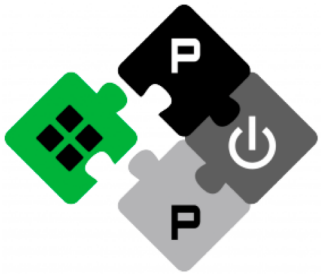


PULP PLATFORM
Open Source Hardware, the way it should be!

What has PULP been up to lately?

Short summary of our activities over the summer of 2019

Frank K. Gürkaynak, ETH Zürich
kgf@ee.ethz.ch

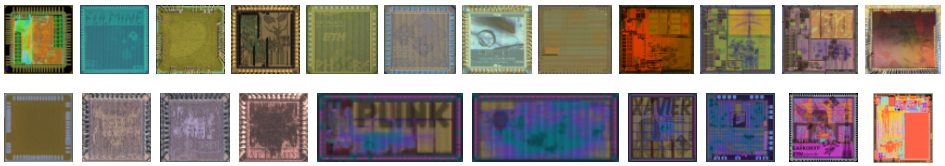
 **http://pulp-platform.org**

 **@pulp_platform**

ETH zürich

PULP started in 2013

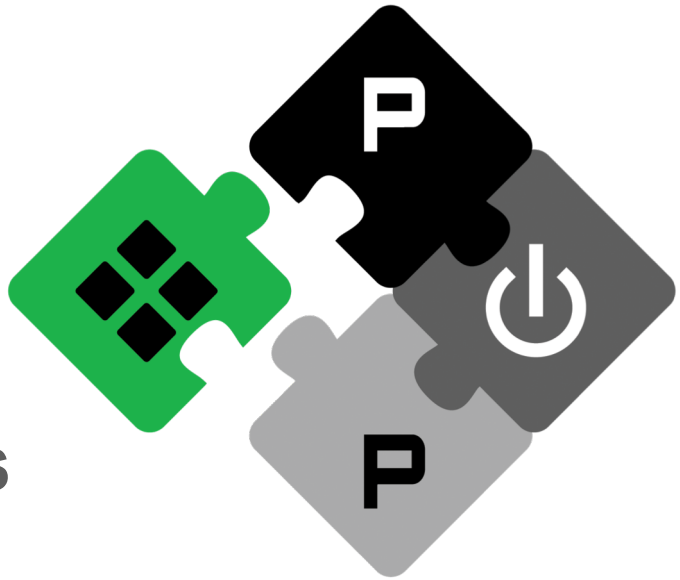
- **Luca wanted to work on NEW energy efficient architectures**
  - Keywords were: parallel processing, near threshold operation, energy efficiency
  - **P**arallel **U**ltra **L**ow-**P**ower platform was born
- **Large group of 60 people in ETH Zurich and University of Bologna**
  - Working on technology, IC design, architecture, programming, and applications.
- **At the moment, we have 36 ASICs taped out**
  - **6x** 22nm, **4x** 28nm, **1x** 40nm, **15x** 65nm, **5x** 130nm, **5x**180nm



+ 1 more without picture (vivosoc3.14)

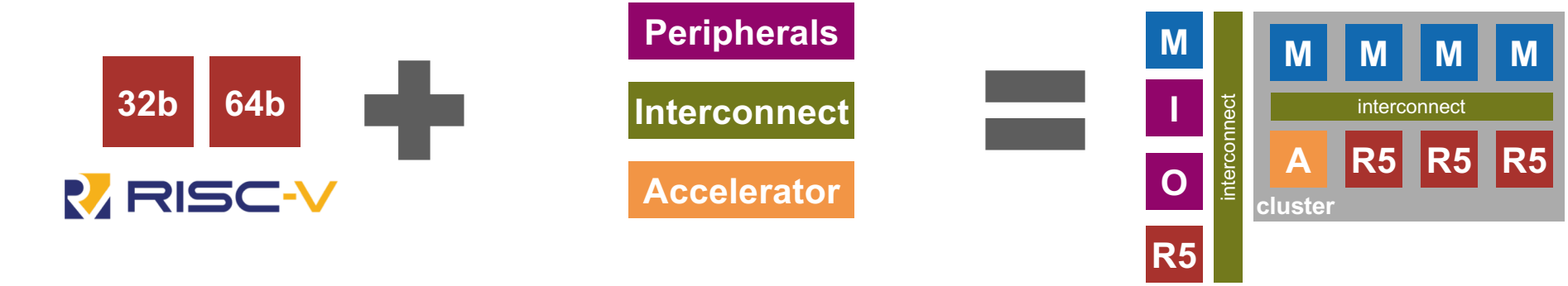
We research energy efficient architectures

- **Near threshold processing**
  - Efficiency is higher at lower operationg voltage
- **Parallel processing as much as possible**
  - Multiple parallel cores at NTV rather than one big core
- **Efficient ways of switching operation modes**
  - Reduce overhead of switching modes
- **Heterogeneous Acceleration**
- **Making use of Technology**

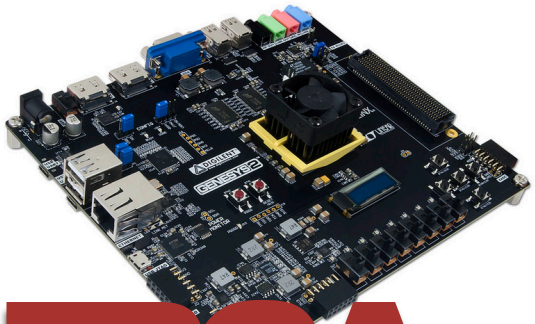


PULP

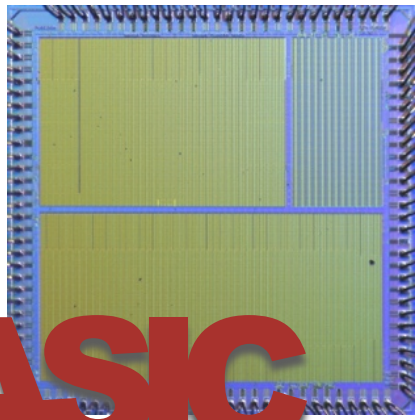
We provide hardware for computing systems



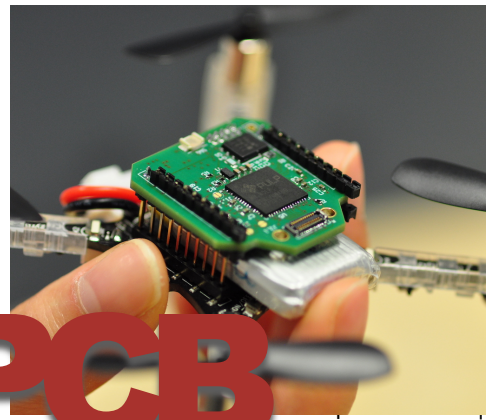
CORES → SYSTEMS



FPGA



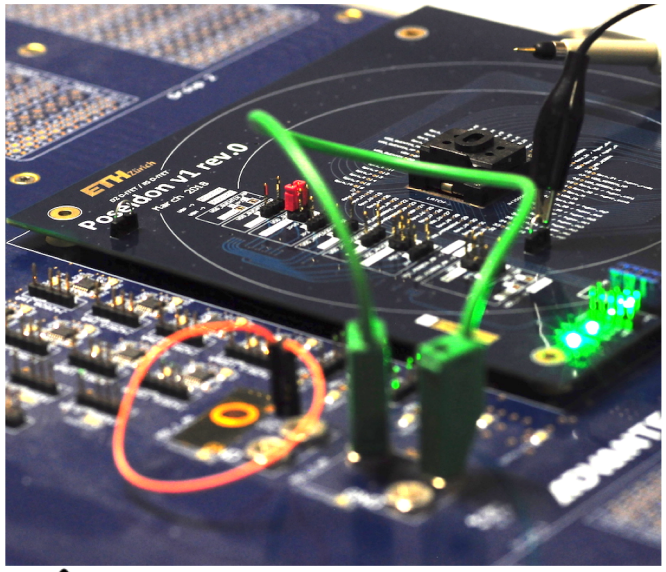
ASIC

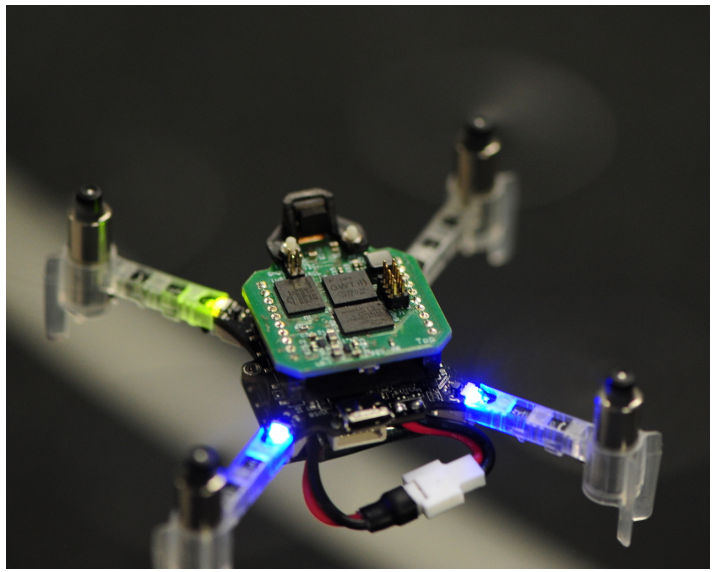


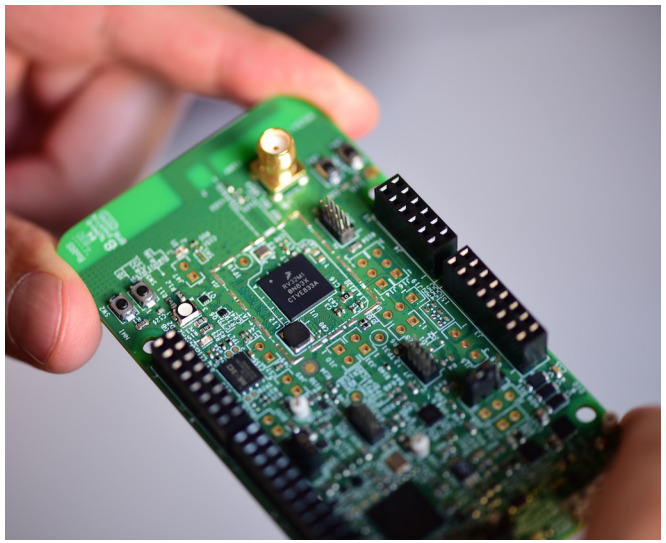
PCB

Our ASICs have different use cases

- **Chips characterized on an IC tester** *(Poseidon 22nm)*
- **Research demonstrators** *(Nano drone with Mr. Wolf/GAP8)*
- **Industrial uses of our cores/peripherals** *(open-isa.org Vega board)*







PULP uses a permissive open source license

- **All our development is on GitHub**
  - HDL source code, testbenches, software development kit, virtual platform

https://github.com/pulp-platform

- **PULP is released under the permissive Solderpad license**
  - Allows anyone to use, change, and make products without restrictions.
- **As of now (2019) we have released:**
  - Single core platforms: PULPino, PULPissimo
  - Cluster-based multi-core platforms: OpenPULP, HERO, Open Piton + Ariane
  - And a range of RISC-V cores, peripherals, accelerators and interconnect solutions

Spanning a large application domain

RISC-V Cores

RI5CY	Ibex	Snitch	Ariane
32b	32b	32b	64b

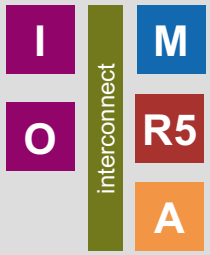
Peripherals

JTAG	SPI
UART	I2S
DMA	GPIO

Interconnect

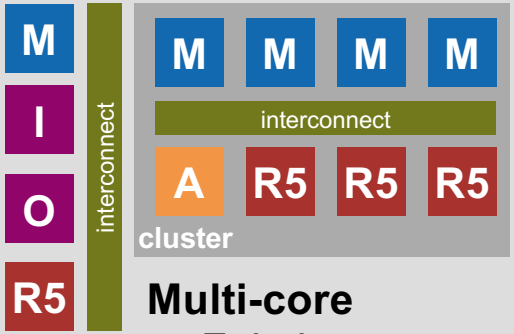
- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

Platforms



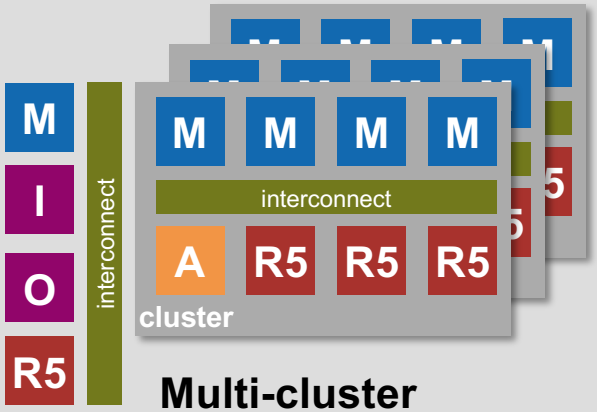
Single Core

- PULPino
- PULPissimo



Multi-core

- Fulmine
- Mr. Wolf



Multi-cluster

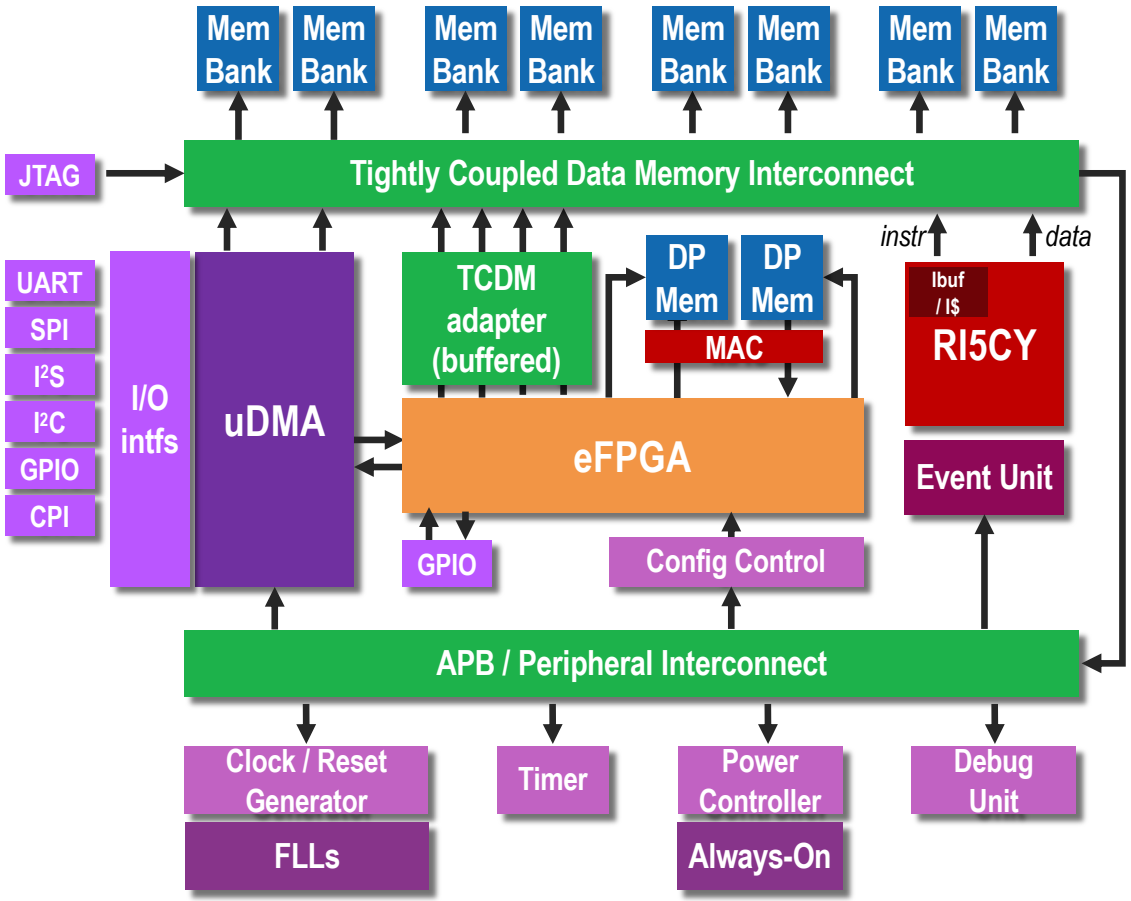
- Hero

IOT → **HPC**

Accelerators

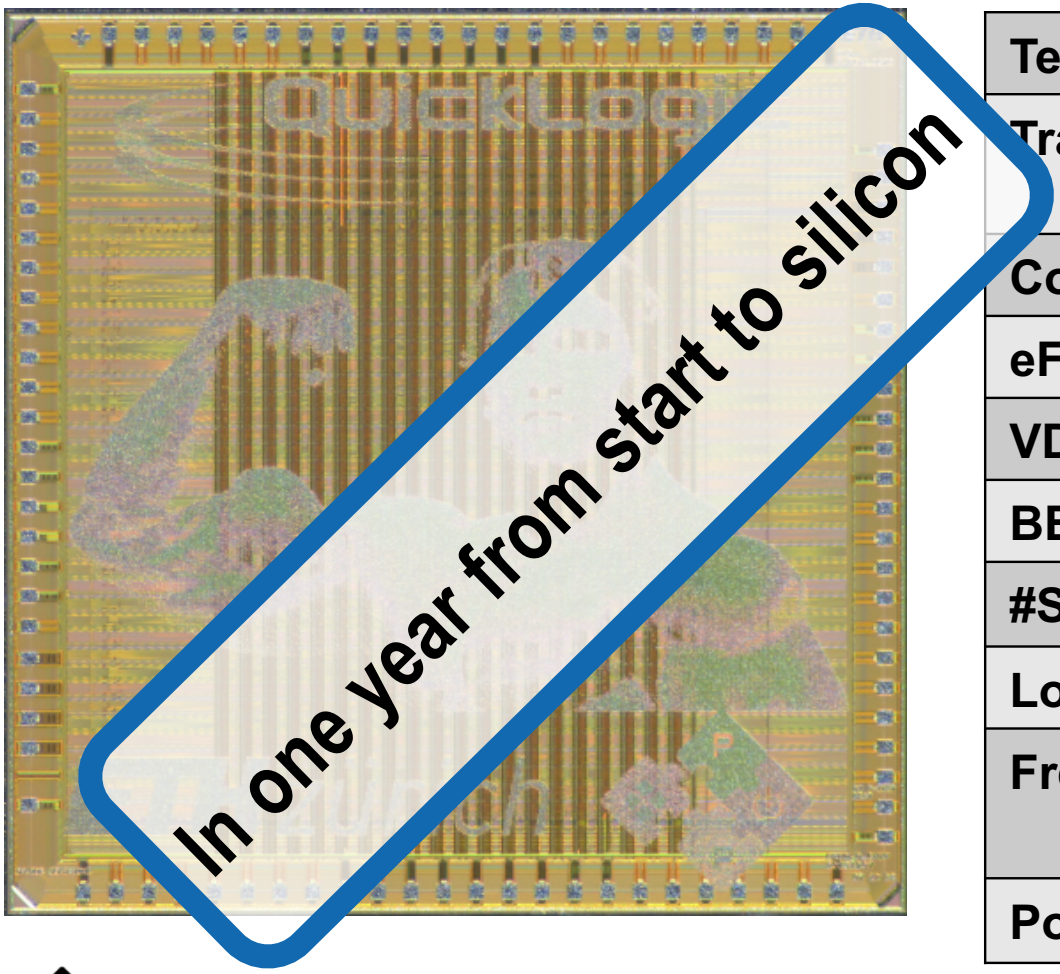
HWCE (convolution)	Neurostream (ML)	HWCrypt (crypto)	PULPO (1st order opt)

Arnold: a Collaboration with Quicklogic



- **Chip in 22nm FDX**
  - Combines e-FPGA (Quicklogic)
  - with PULPissimo (single core uC)
- **Multiple operation modes**
  - Configurable peripheral
  - Accelerator for core
  - Accelerator for independent I/O

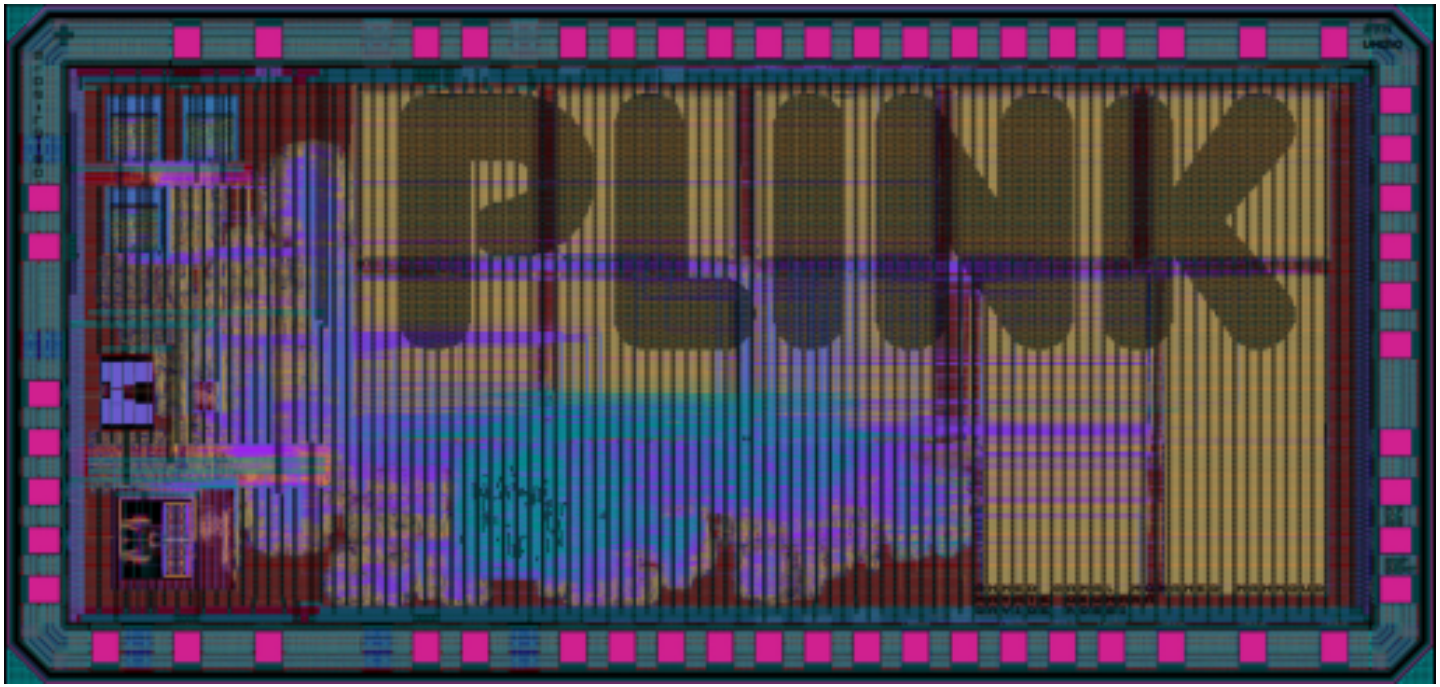
Arnold Measurement Results



Technology	GF FDX 22nm
Transistors	SoC: Flip-well FPGA: Conventional well
Core area	6.86 mm^2
eFPGA area	4 mm^2
VDD range	0.5V - 0.8V
BB range	-1.8V – 0.0V
#SRAM macros	32 x 4096x32 bit
Logic Gates	480 kGE
Frequency range	SoC: 32kHz - 580 MHz FPGA: 0MHz - 116 MHz
Power range	0 – 17mW

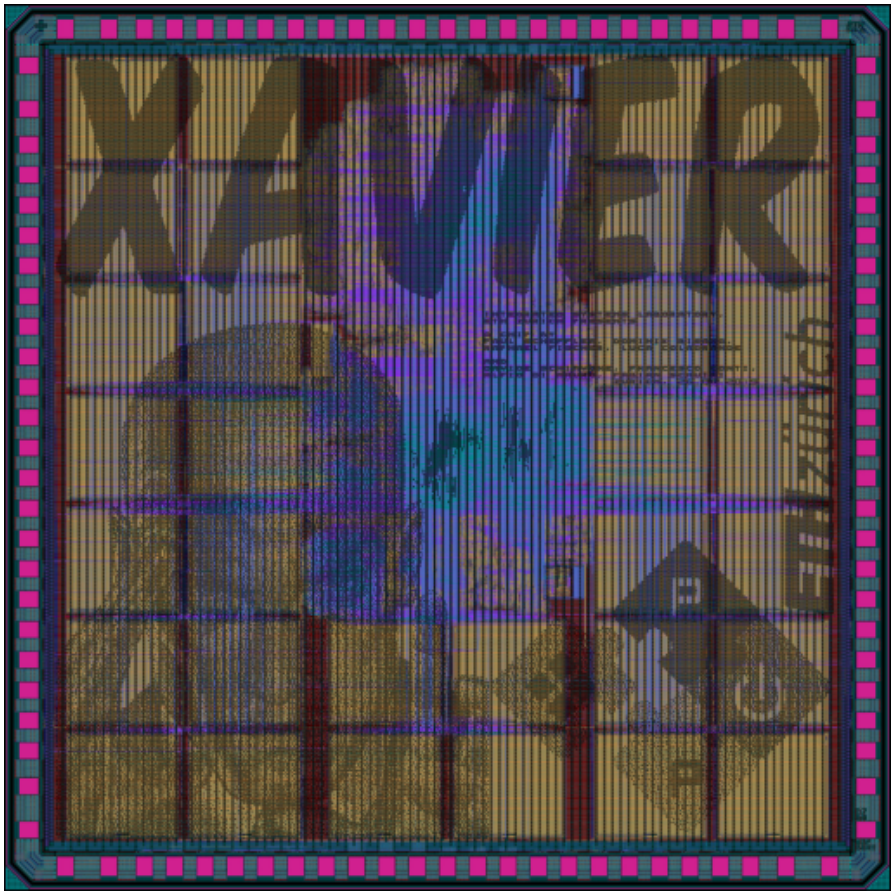
PLINK – Serial communication

- Project to investigate short distance (<2cm) chip to chip communication
- The transceiver is technology specific.
- At the moment we can not open source such designs (NDAs with technology provider and EDA companies prevent this)



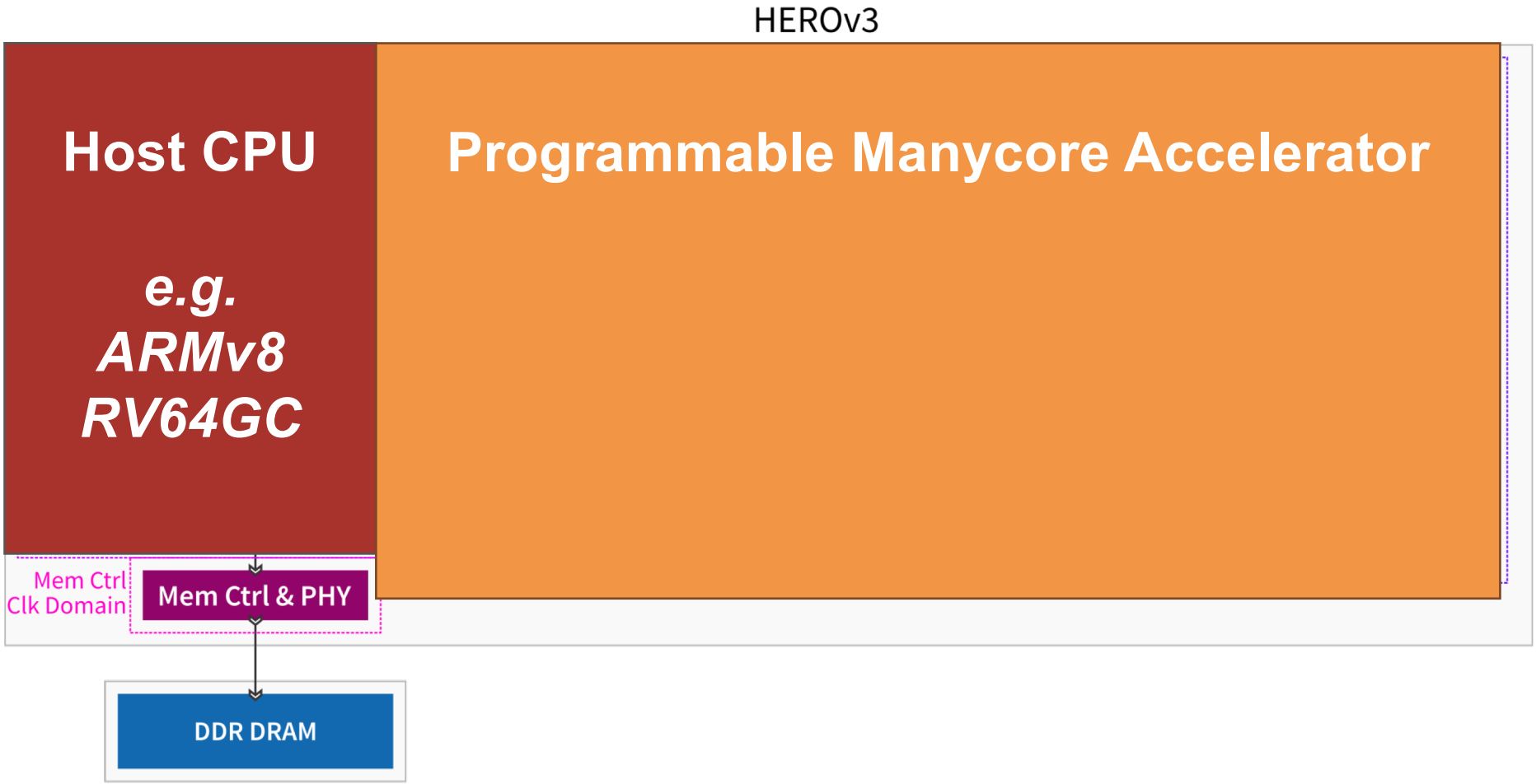
Chip in UMC 65nm, basic PULPissimo system, Serial PHY and AXI adaptor

Xavier – PULPissimo implementation



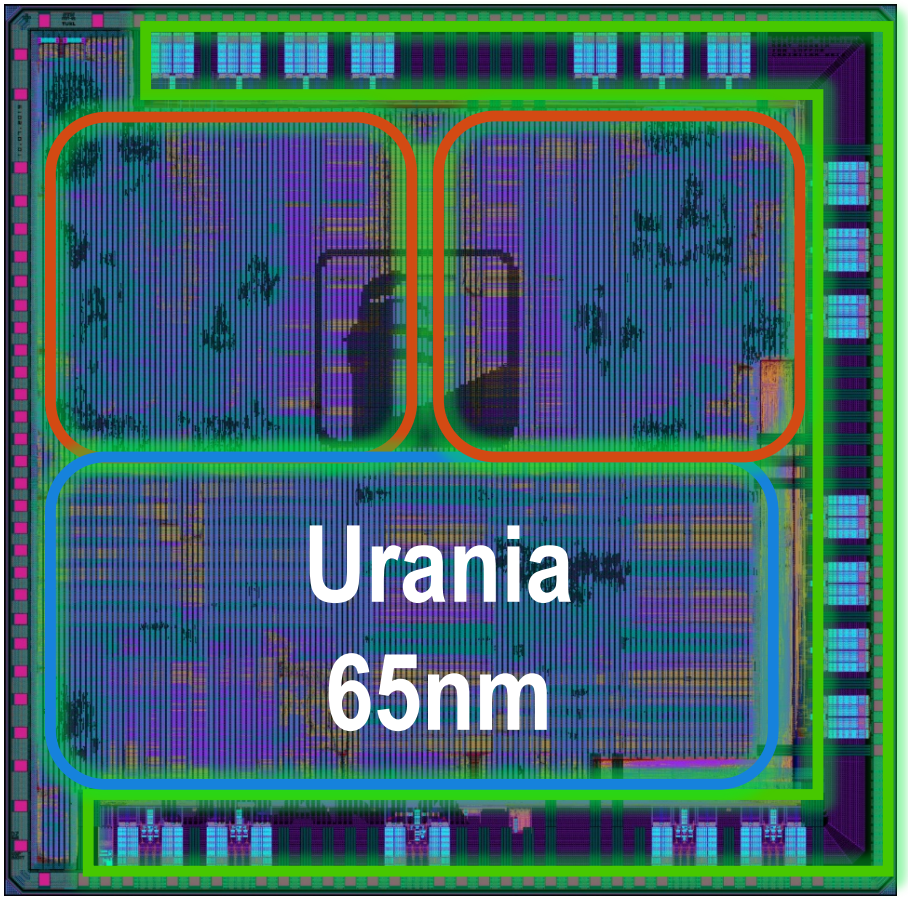
- **Several ideas combined**
  - a RI5CY (RV32ICMF) as main core
  - a uDMA system handling 8 SPI ports
    - Collecting data from independent sources
  - Integrated filtering capabilities inside uDMA
    - IIR, Template matching, and spike detection.
  - Hardware Accelerator for quantized neural networks (4b weights, 4b inputs), 4.81 GMAC/s.
  - a total of 512 kByte memory.
- **Student designs at ETH Zurich**

Cluster as heterogenous accelerator (HERO)



HERO on ASIC (64bit RISC-V + 32bit RISC-V)

- **2 PULP clusters, each with**
  - 4x RV32 RI5CY cores
  - 4x transprecision FPUs
  - 1x PULPO accelerator
  - 64 kB TCDM in 8 banks
- **Ariane RV64 host processor**
  - 128 KiB Shared LLC
  - software-managed IOMMU
- **DDR3 DRAM Controller + PHY**
  - Designed by TU-Kaiserslautern



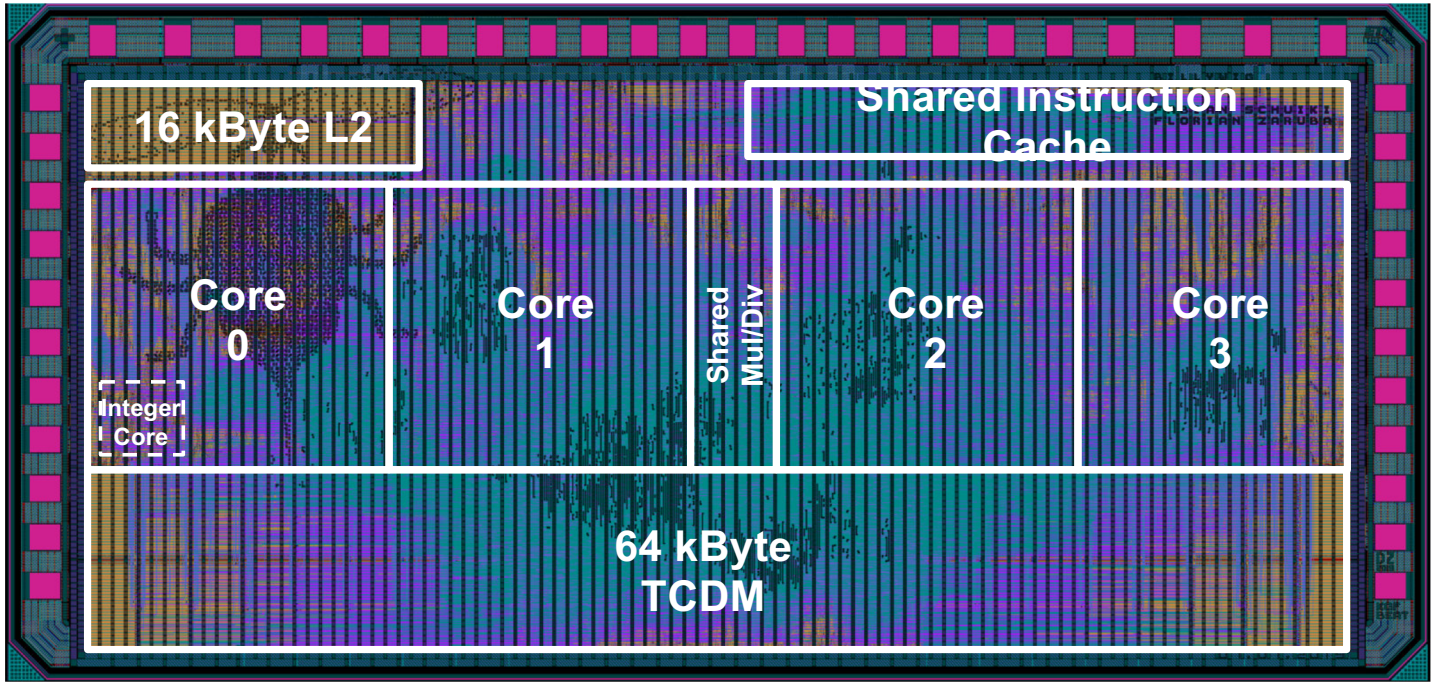
PULP

Baikonur – 22nm Ariane + ML acceleration

- **Resubmission of Kosmodrom**
  - One commercial IP was not working
  - All open source IP worked fine
- **Optimized Ariane (64b) cores**
  - One for high-performance
  - Other one for low power consumption
  - Using different libraries and process corners
- **Additional payload on chip**
  - Total of 25x Snitch cores for ML acceleration

Billywig – A cluster with Snitch (new core)

- Area: 2.4 mm2
- Speed: 350 MHz
- 4 Snitch Cores
  - RV32IMAFD
  - 4 FPUs
    (1x fp64, 2x fp32 ops)
  - 2 SSR lanes per FPU
- 64 kB TCDM
- 16 kB L2



Are these projects open source?

- **In principle our goal is to open source everything**
- **Some of these are still new ideas that we are working on**
  - Not all will prove to be good enough to be open sourced
  - At the moment some of them still need a bit of work
- **Analog design blocks, layouts etc can not yet be open source**
  - Agreements we have signed, prevent us from releasing them
  - They are specific to the technology
- **DDR3 controller and PHY is not from PULP**
  - Our project partner from OPRECOMP, TU-Kaiserslautern has the rights.

Silicon and open source fuel PULP success

Direct research collaborators on PULP

- Politecnico di Torino
- University of Cambridge
- USI Lugano
- TU Kaiserslautern
- University of Cagliari
- IBM Research Zurich
- EPF Lausanne
- CSEM Neuchatel
- Princeton University
- Technische Universität Graz
- CEA-Leti Grenoble
- Fraunhofer-Gesellschaft
- Sapienza Università di Roma

Academic users we are aware of

- Università di Genova
- Politecnico di Milano
- Fondazione Bruno Kessler
- Lund University
- Stanford University
- UC Los Angeles
- UC San Diego
- Columbia University
- Universitat Bar-Ilan
- İstanbul Teknik Üniversitesi
- NCTU Hsinchu
- University of Zagreb, FER
- TUT Tampere
- RWTH Aachen
- IST University of Lisboa
- UFRN Rio Grande do Norte
- TU Darmstadt
- Universität Bremen
- Hongik University Seoul
- IIT Kharagpur
- LIRMM Montpelier

See up to date list at https://pulp-platform.org/pulp_users.html

What is PULP doing for maintaining cores?

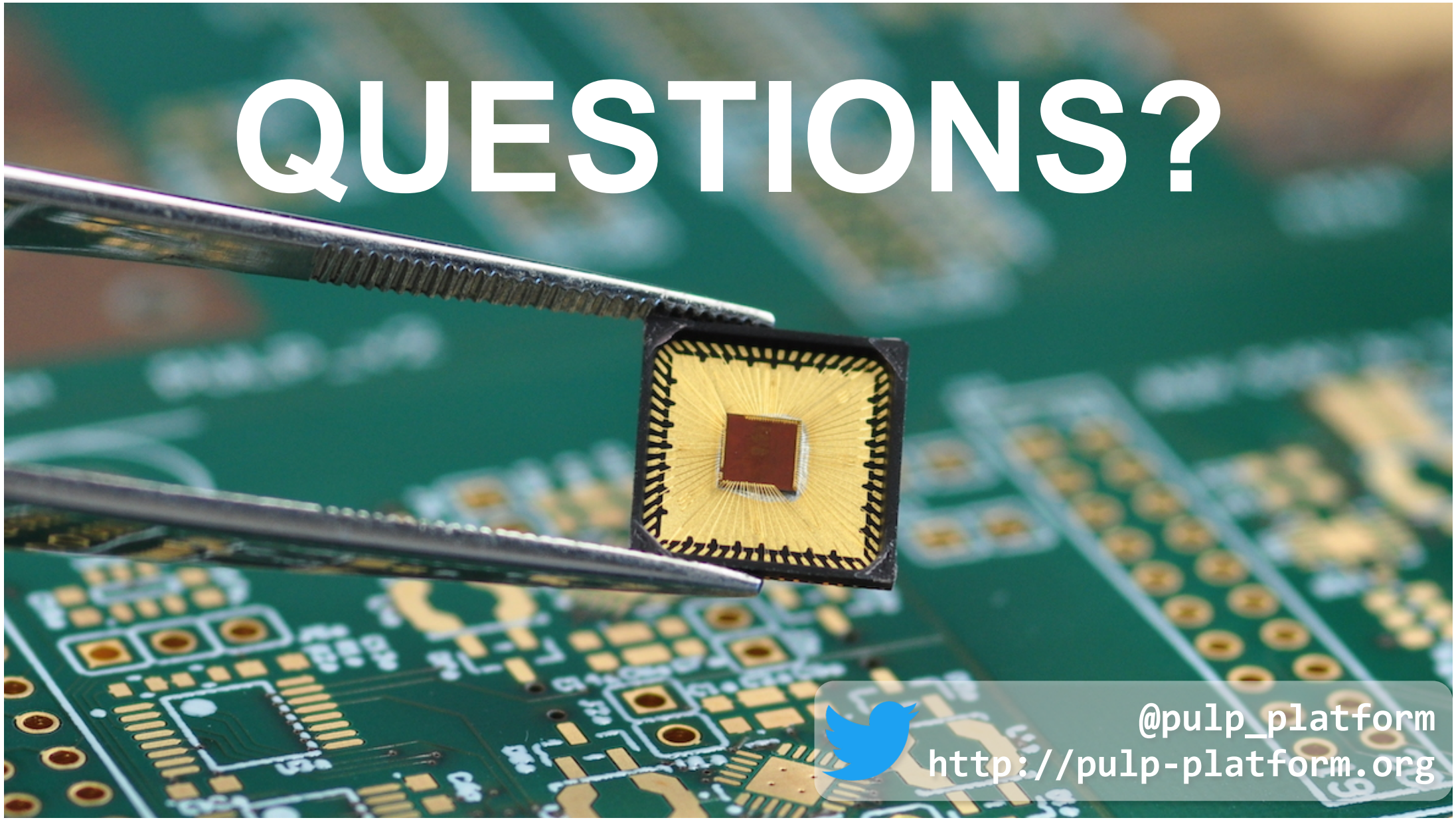
- **We (ETH Zürich and University of Bologna) are research groups**
  - Motivated to develop new architectures and systems
  - We needed efficient RISC-V cores (and peripherals) for our work
  - Not so good (or interested) in providing industrial level support for these cores
- **Goal is to collaborate with groups to maintain our cores/systems**

Next time let's meet in Istanbul

https://fossi-foundation.org/fossistanbul/

Final words

- **PULP provides high quality RISC-V based platforms**
  - Permissive open source license
  - Written in SystemVerilog
  - Available from GitHub: https://github.com/pulp-platform
- **Our research is developing energy-efficient systems**
  - Wide range of applications from IoT to HPC
  - We design complete systems
- **Open to collaborations with industrial and academic partners**
  - We have plenty of collaborations, as PULP allows us to quickly progress with projects


QUESTIONS?
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