ETH zürich ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

PULP within the Open Source Hardware Landscape

Integrated Systems Laboratory (ETH Zürich)

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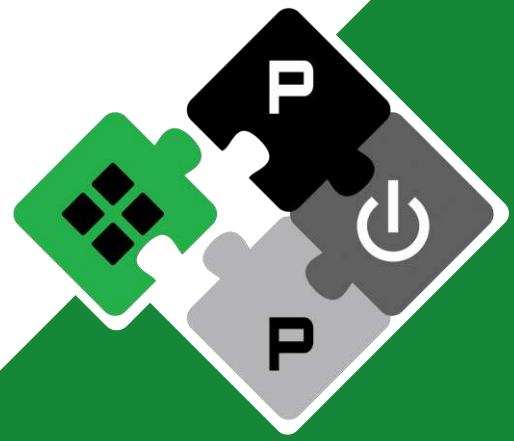


@pulp_platform

pulp-platform.org

youtube.com/pulp_platform

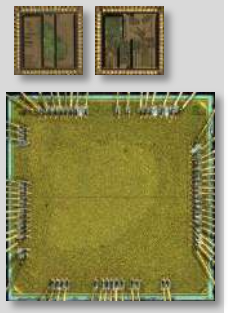
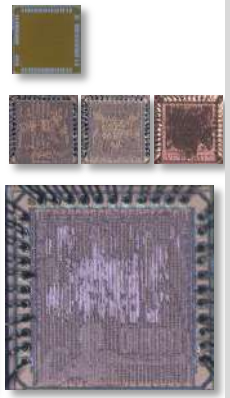
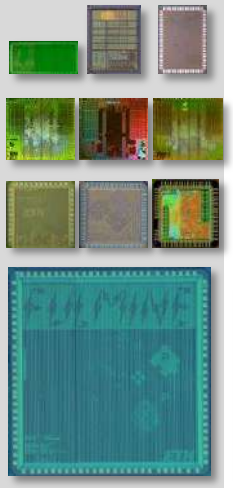
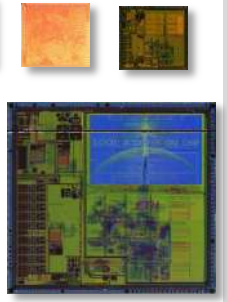
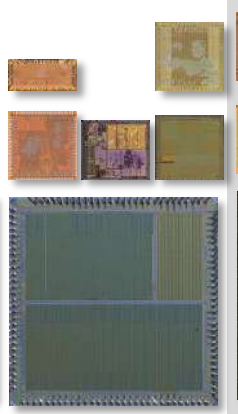
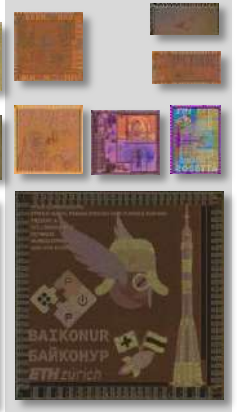
PULP Platform

Open Source Hardware, the way it should be!

Parallel Ultra Low Power (PULP) Platform

- **Research on open-source energy-efficient computing**

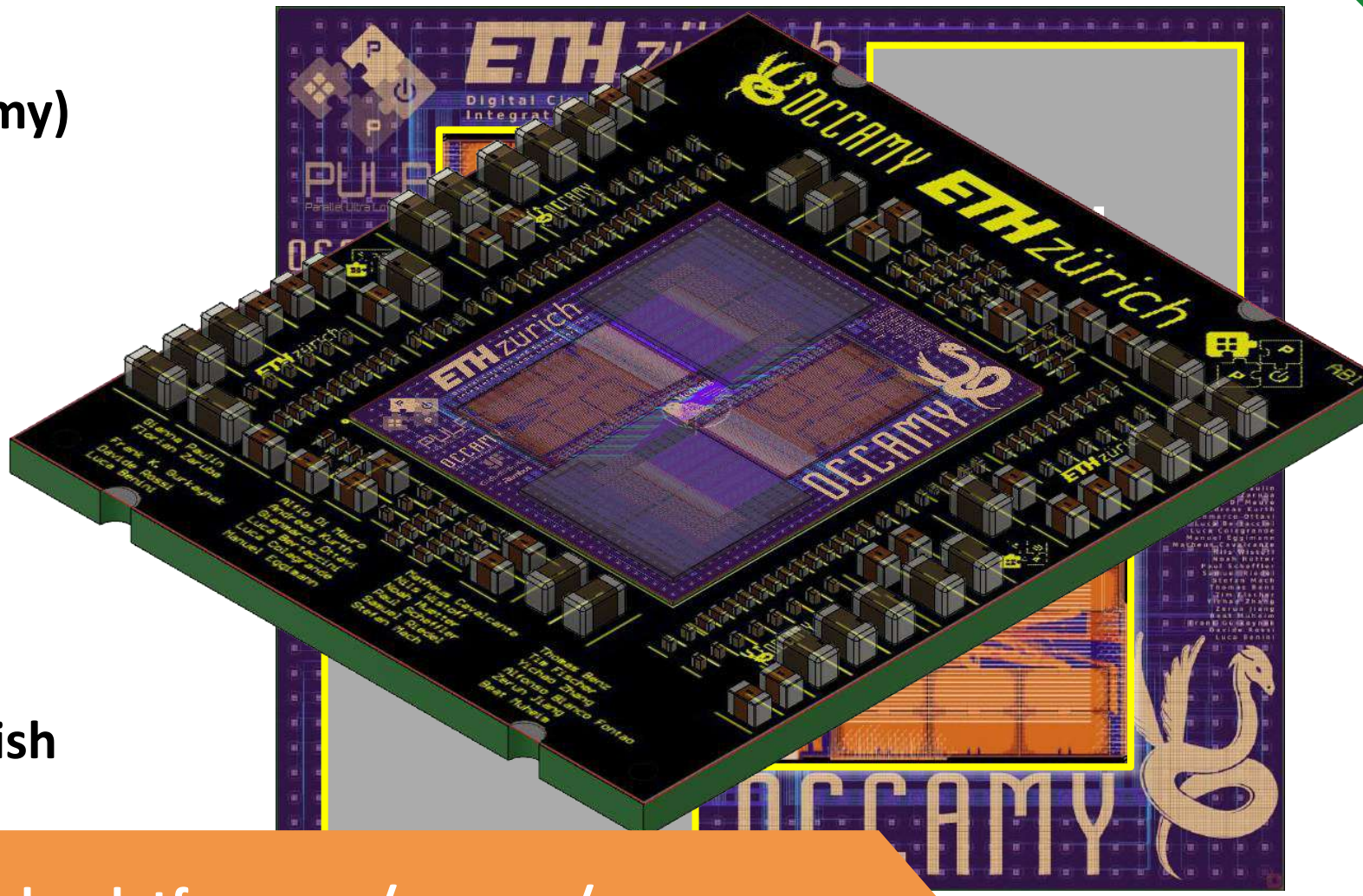
We have designed and tested more than 50 PULP ICs

2013 (3)	2014 (5)	2015 (10)	2016 (3)	2017 (2)	2018 (6)	2019 (7)	2020 (3)	2021 (7)	2022 (9)
									
PULPv1 *STM 28FDSOI* Multi-core processor	**Diana** *UMC 65* 4-core system with approximate FPUs	**Fulmine** *UMC 65* 4-core system with ML and Crypto accelerators	**VivoSoC 2.001** *SMIC 130* Mixed signal system for biosignal acquisiton	**Mr. Wolf** *TSMC 40* 8+1 core IoT processor	**Poseidon** *GF 22FDX* 64bit RISC-V core, 32bit Microcontroller system, ML rator	**Baikonur** *GF 22FDX* Dual 64bit RISC-V core, 3x 8core snitch clusters, Body biasing test vehicle	**Dustin** *TSMC 65* IoT processor with 16 cores and QNN enhancements	**Kraken** *GF 22FDX* IoT processor with Spiking Neural and Ternary Inference Engines	**Occamy** *GF 12LPP* ML accelerator with 216 + 1 cores and HBM interface

Check http://asic.ethz.ch for all our chips

Including some very complex designs like Occamy

- **Chiplet based design**
- **2x Compute chiplets (Occamy)**
  - 216+1 RISC-V cores
  - 0.75 TFLOP/s for the system
  - GF12LPP
  - Running at 1 GHz
- **2x 16GB HBM DRAMs**
- **Silicon Interposer**
  - GF 65nm 26mm x 23mm
- **Waiting for assembly to finish**



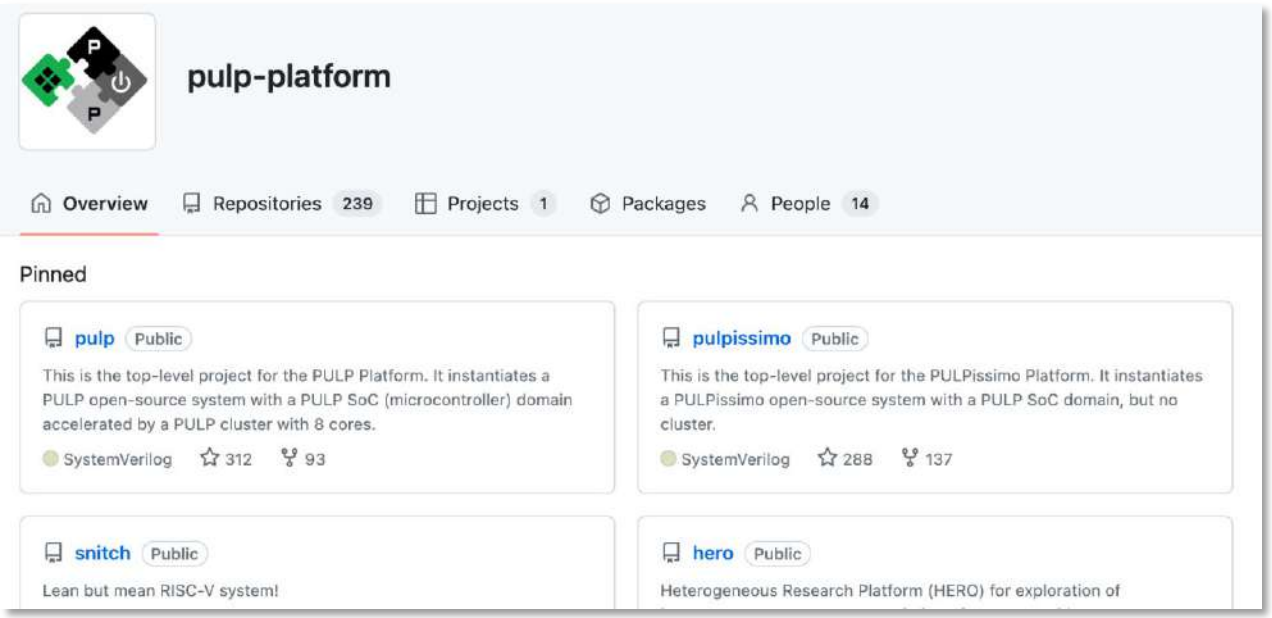
More on Occamy – https://pulp-platform.org/occamy/

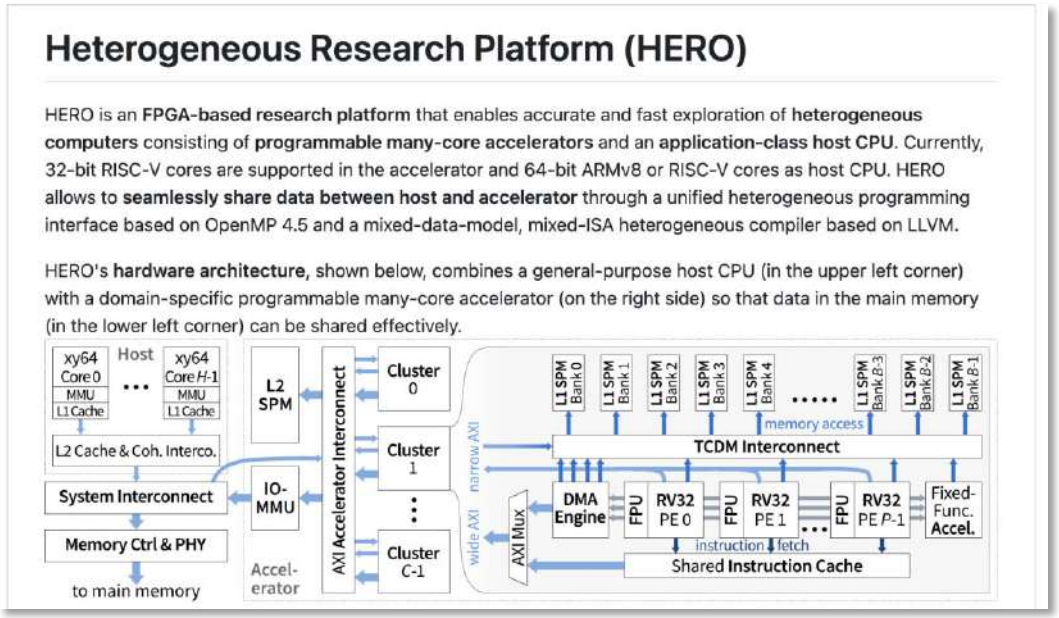
All of our designs are open source hardware

- **All our development is on GitHub using a permissive license**
  - HDL source code, testbenches, software development kit, virtual platform

https://github.com/pulp-platform

- Allows anyone to use, change, and make products without restrictions.





What PULP provides is a box of building blocks

RISC-V Cores

RI5CY	Ibex	Snitch	Ariane
32b	32b	32b	64b

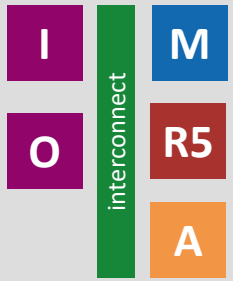
Peripherals

JTAG	SPI
UART	I2S
DMA	GPIO

Interconnect

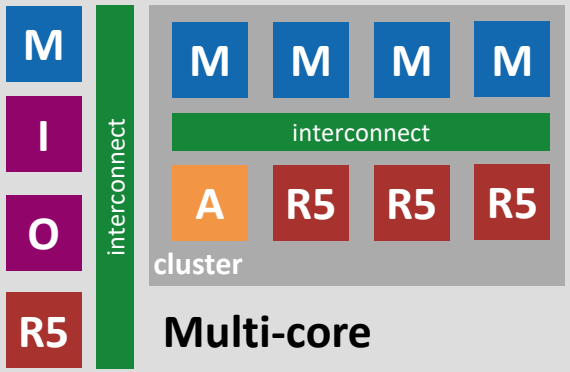
- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

Platforms



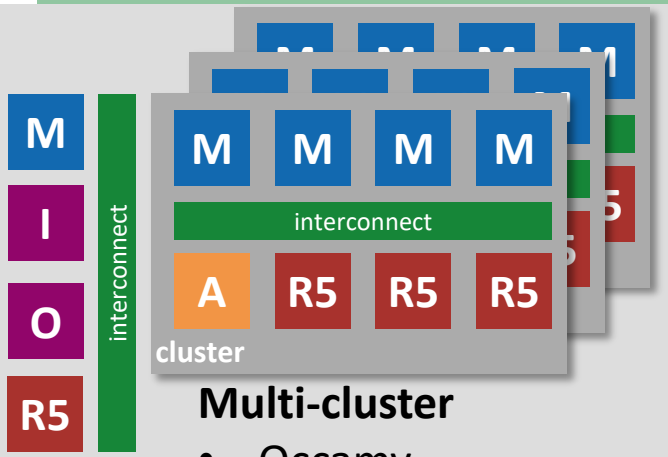
Single Core

- PULPino
- PULPissimo



Multi-core

- OpenPULP
- Mr. Wolf



Multi-cluster

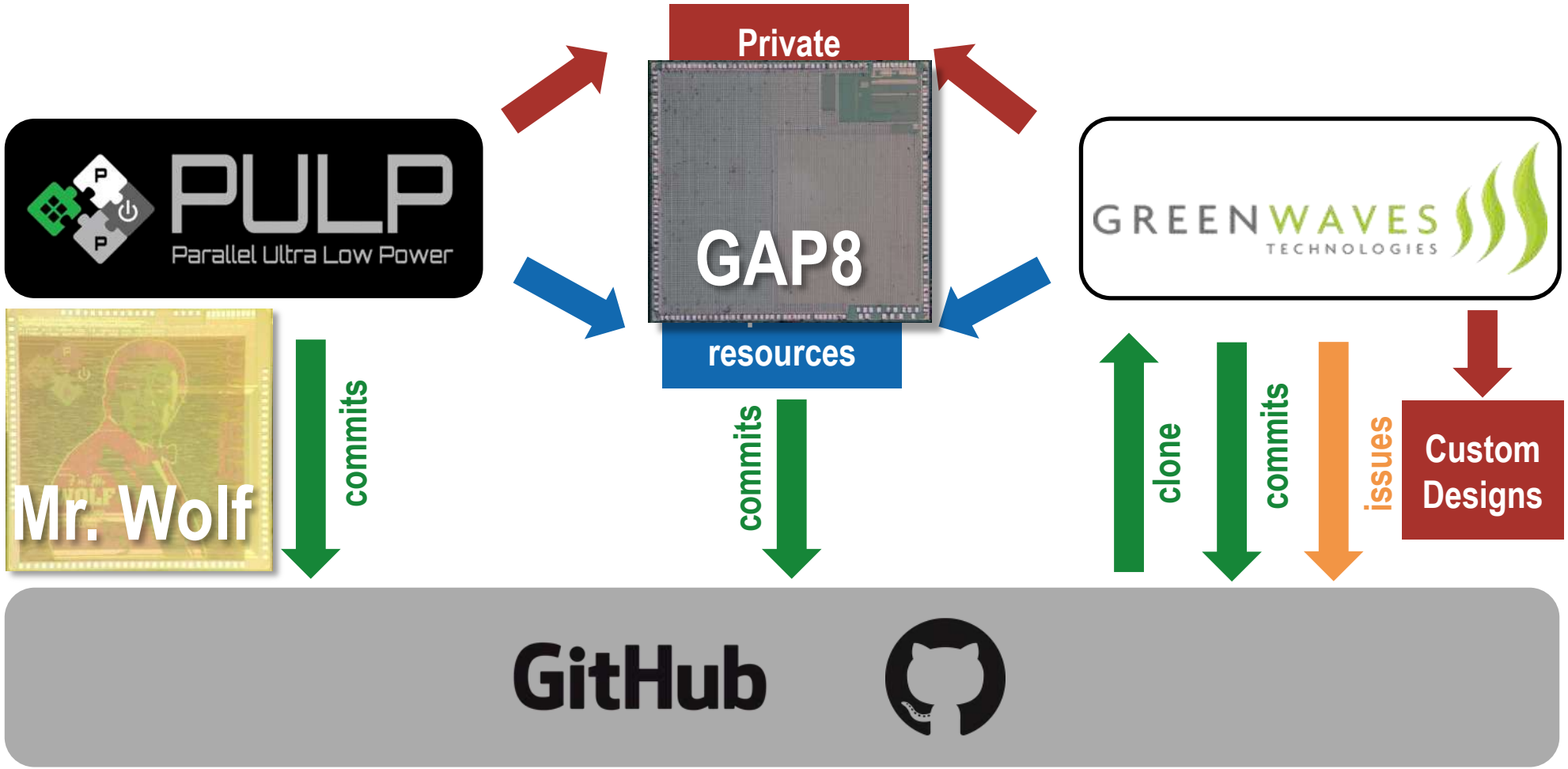
- Occamy
- Hero

IOT → **HPC**

Accelerators

HWCE (convolution)	Neurostream (ML)	HWCrypt (crypto)	PULPO (1st order opt)

How does PULP collaborate with 3rd parties?

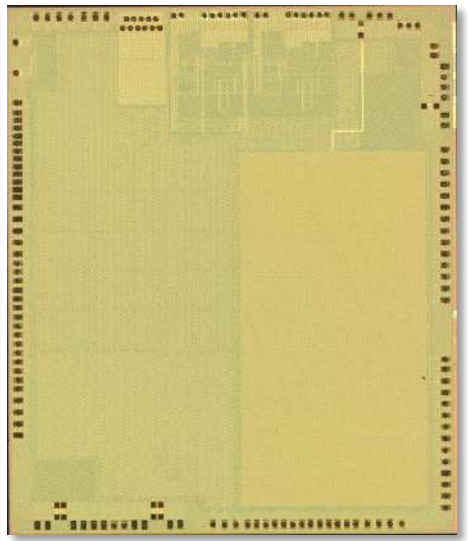


The open model led to successful industry collaborations

QuickLogic®

Arnold (GF22)

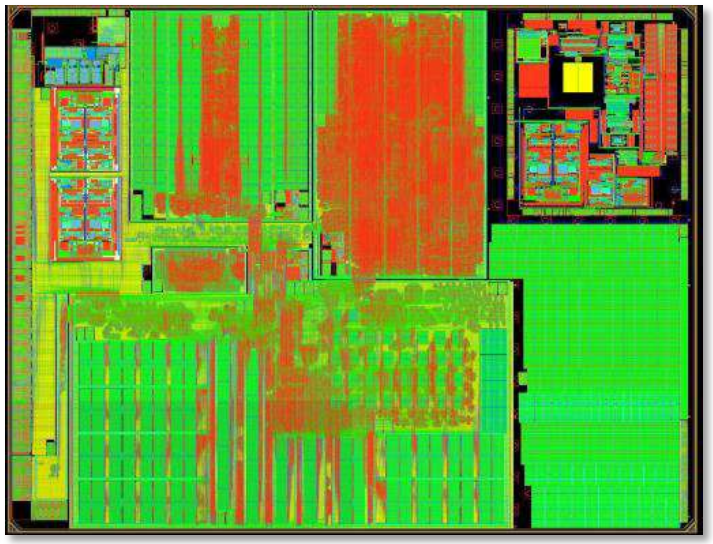
eFPGA with RISC-V core



GREENWAVES TECHNOLOGIES

Vega (GF22)

IoT Processor with ML acceleration



DOLPHIN INTEGRATION

The enabler of low-power Systems-on-Chip

Marsellus (GF22)

IoT Processor with low power modes and event based computing

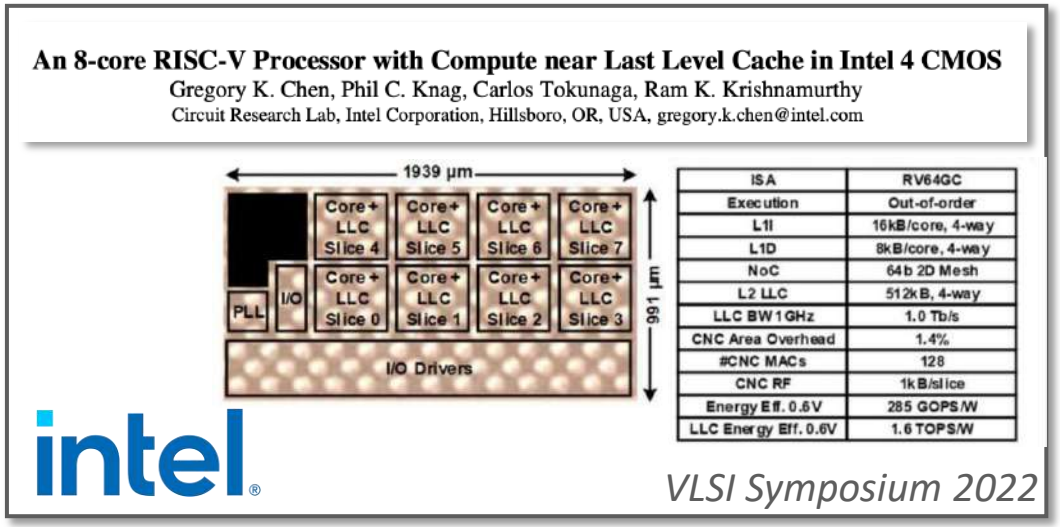
Meta numem

Siracusa (TSMC16)

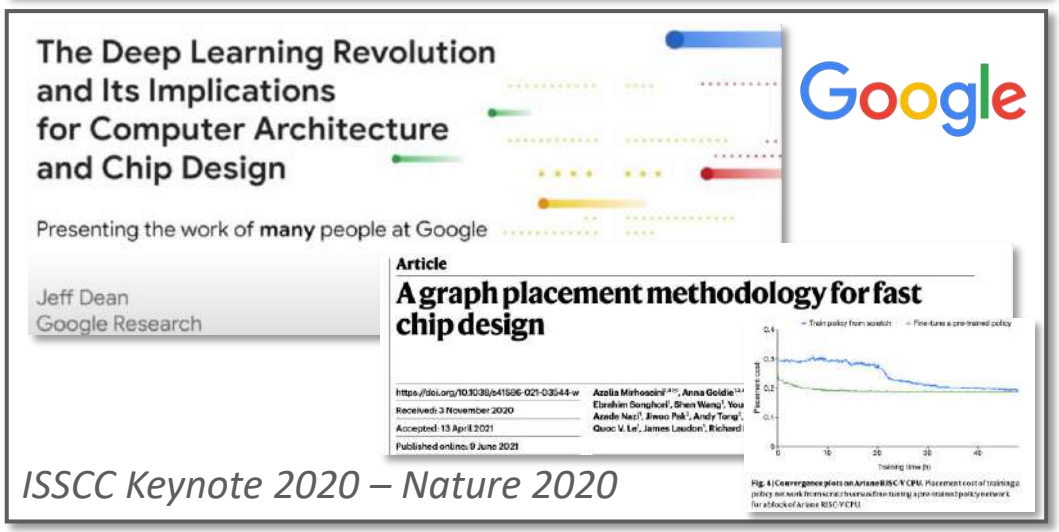
IoT Processor with NVM technology

And many have used our work for their research

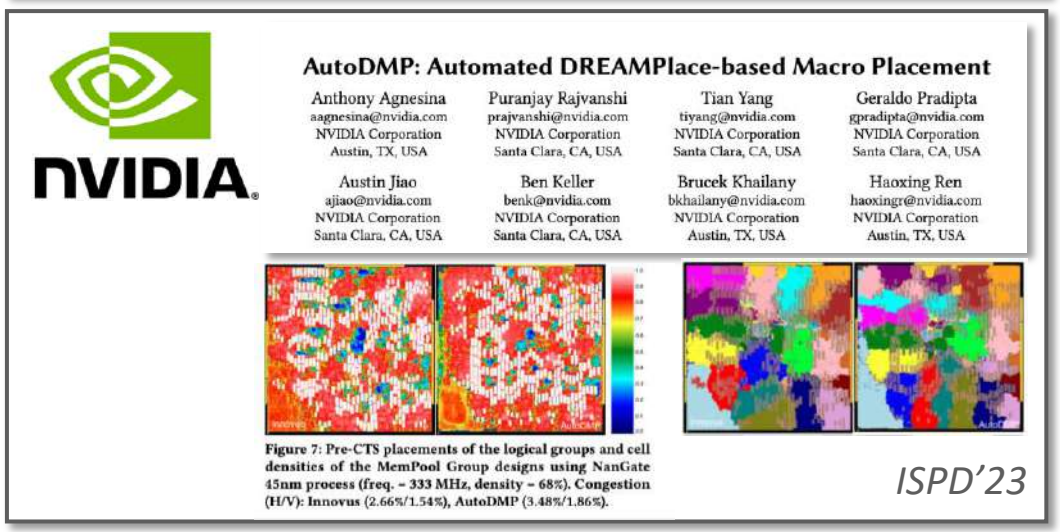
RISC-V week Barcelona 2018



VLSI Symposium 2022

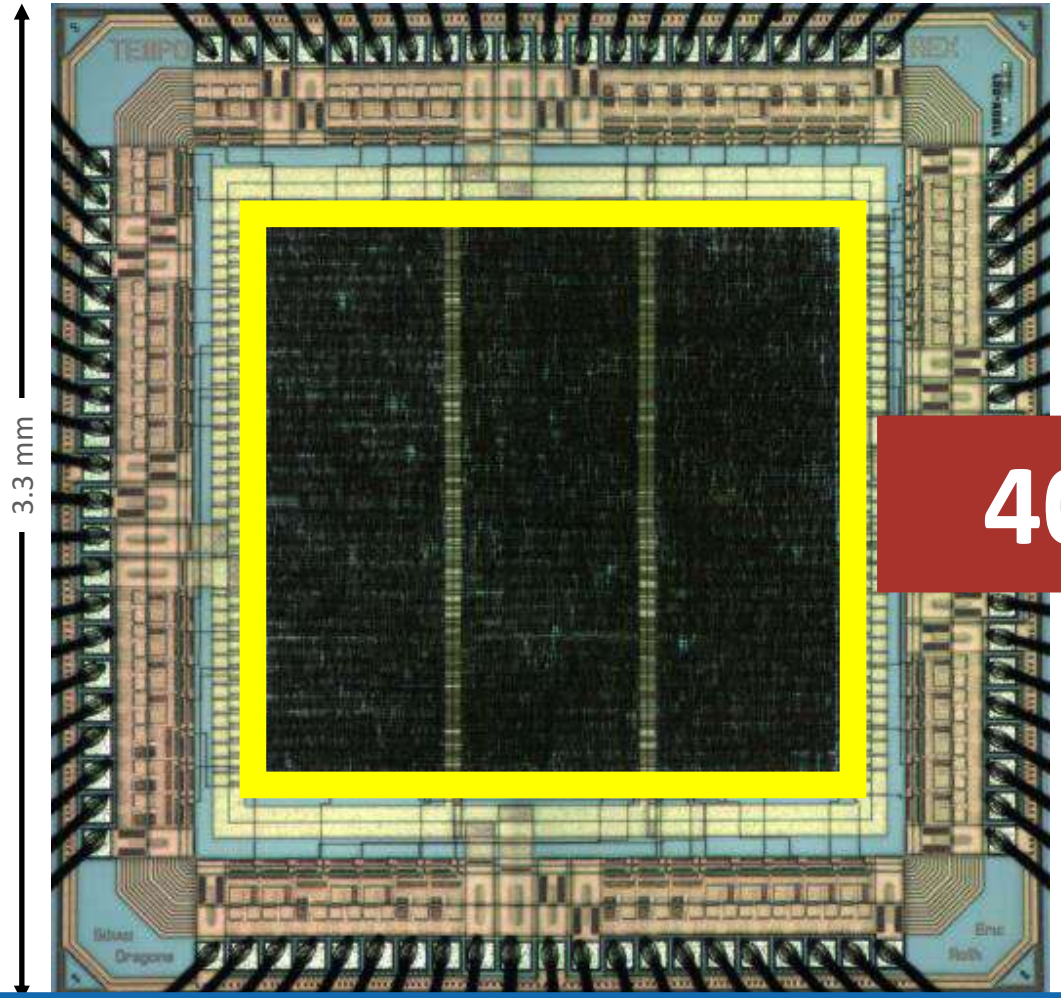


ISSCC Keynote 2020 – Nature 2020



ISPD'23

In the last 20 years IC Design has changed a lot

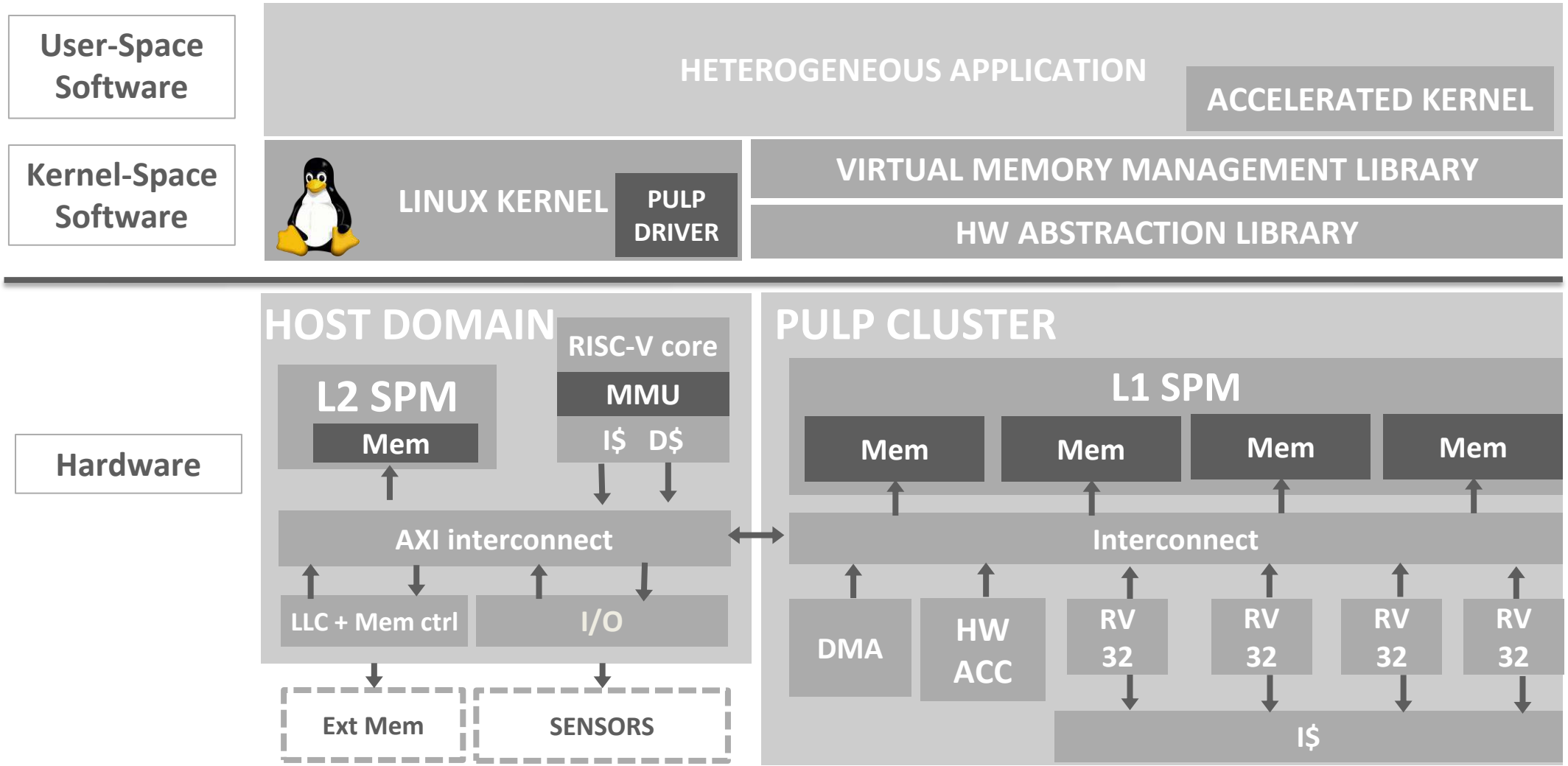


4000 x

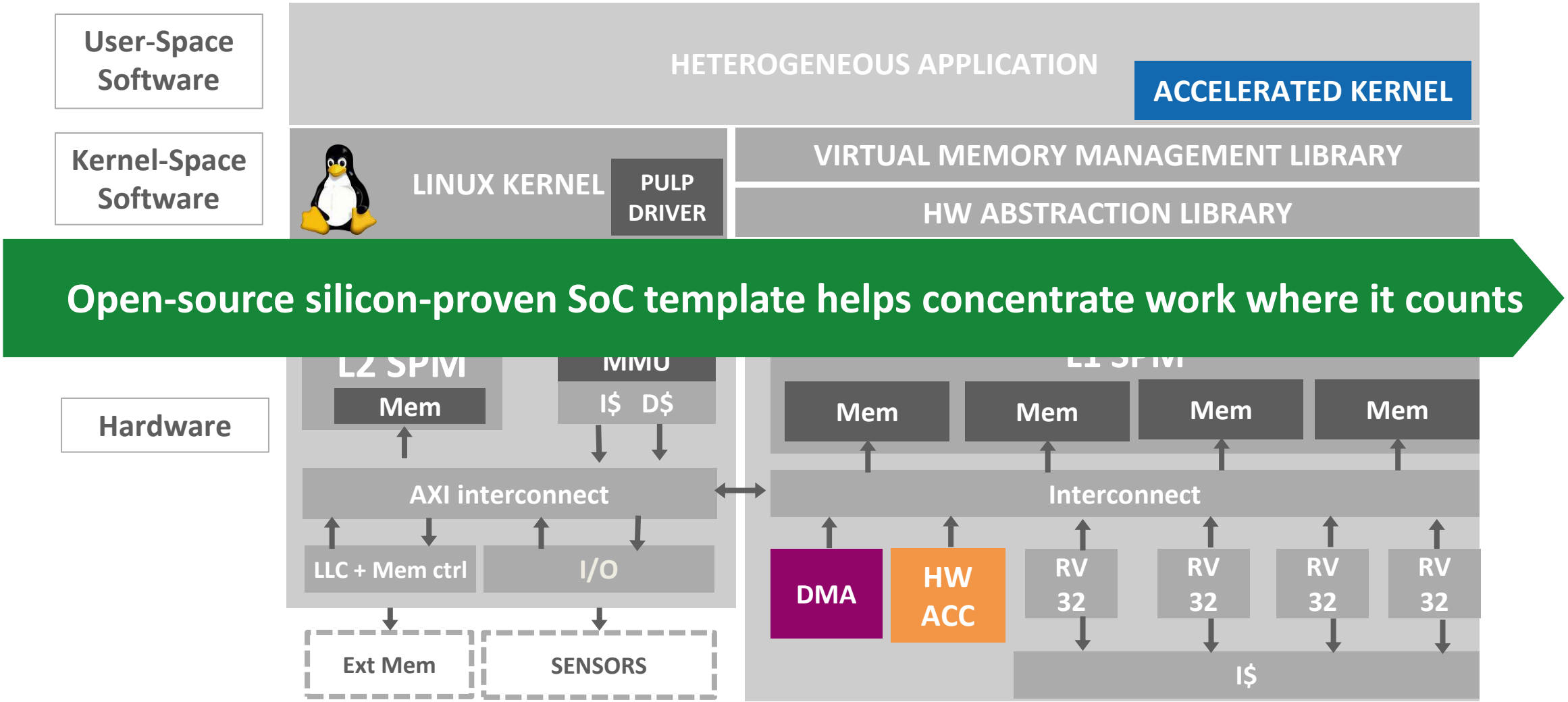
80 MGE

What used to be a complete chip is now a small part of a SoC !

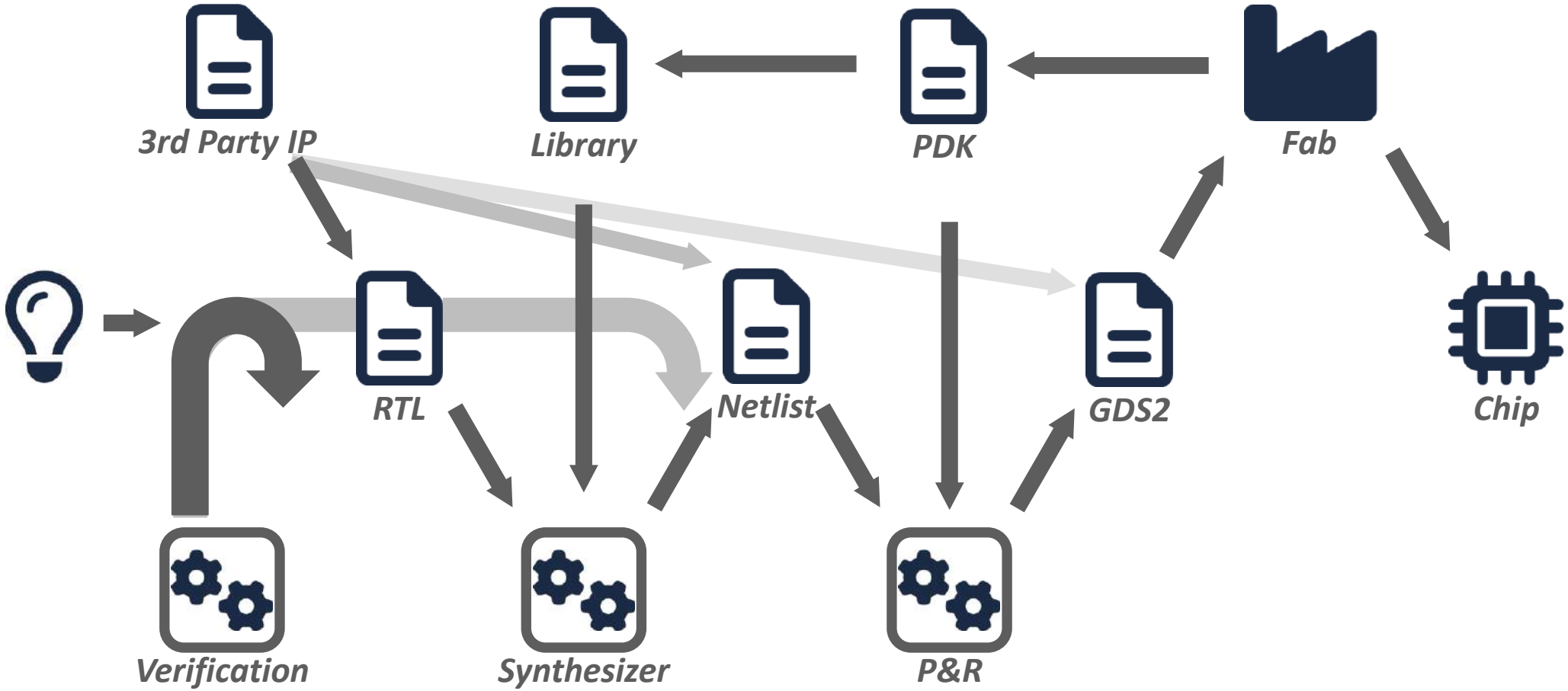
There is so much that makes up a modern SoC



In a typical design, innovation is only in a limited scope

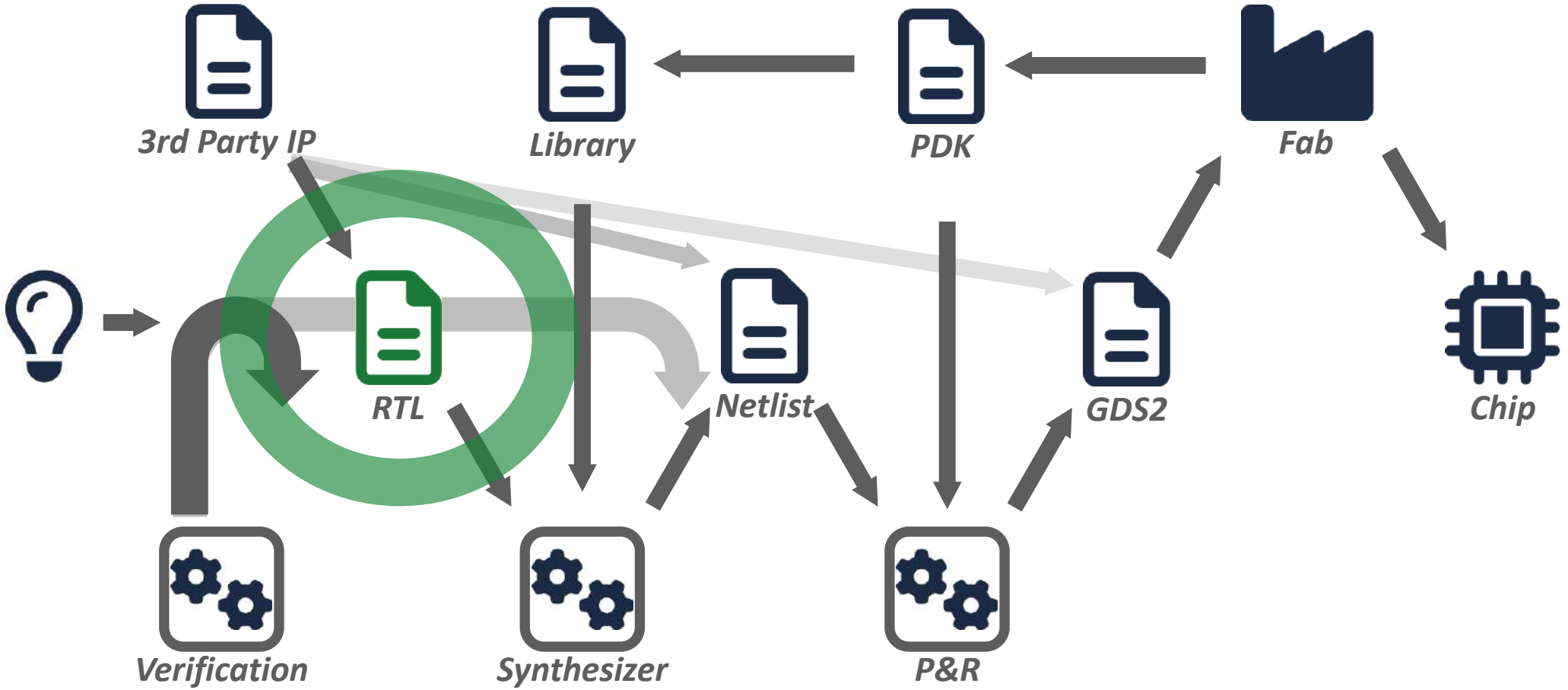


Simplified IC design flow



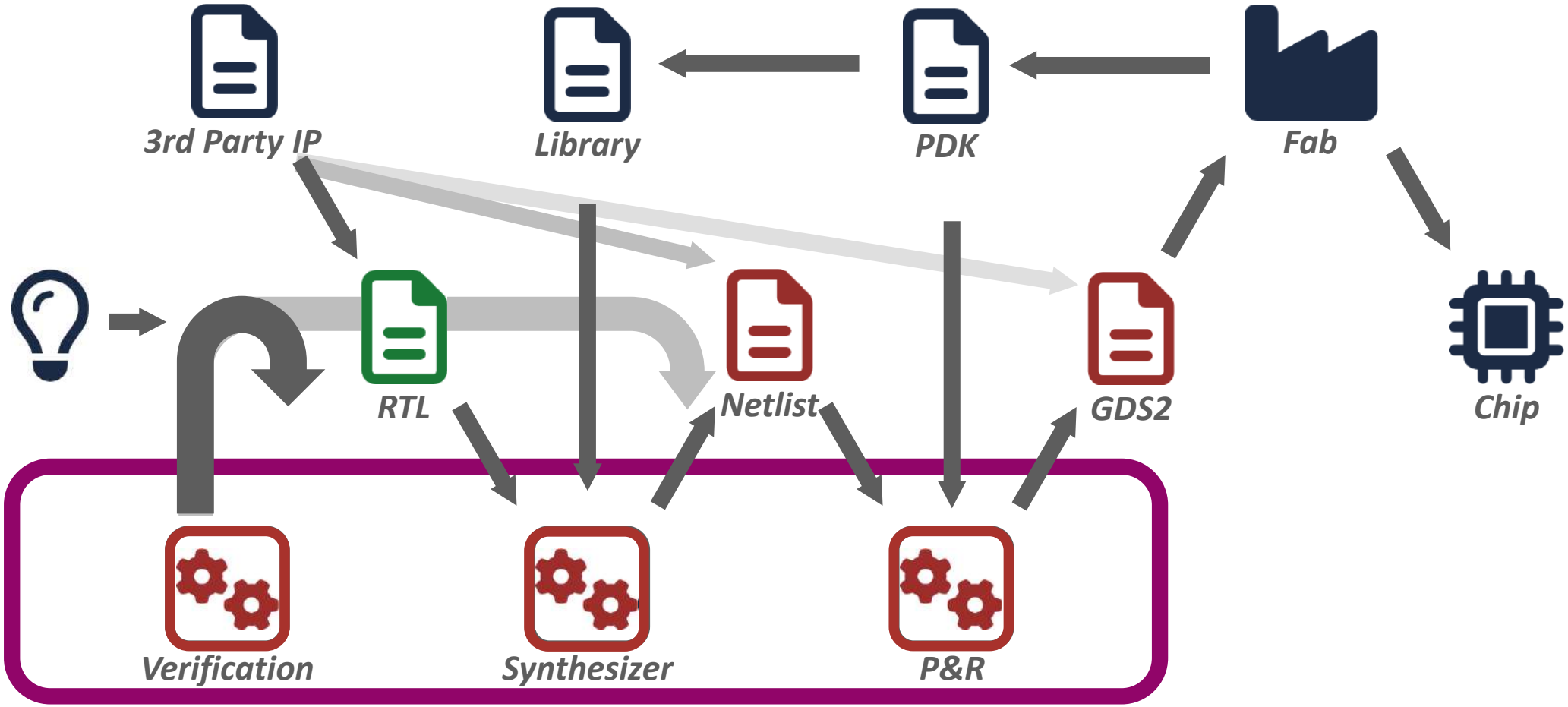
Icons taken from free icons from fontawesome.com

Simplified IC design flow: at the moment only RTL



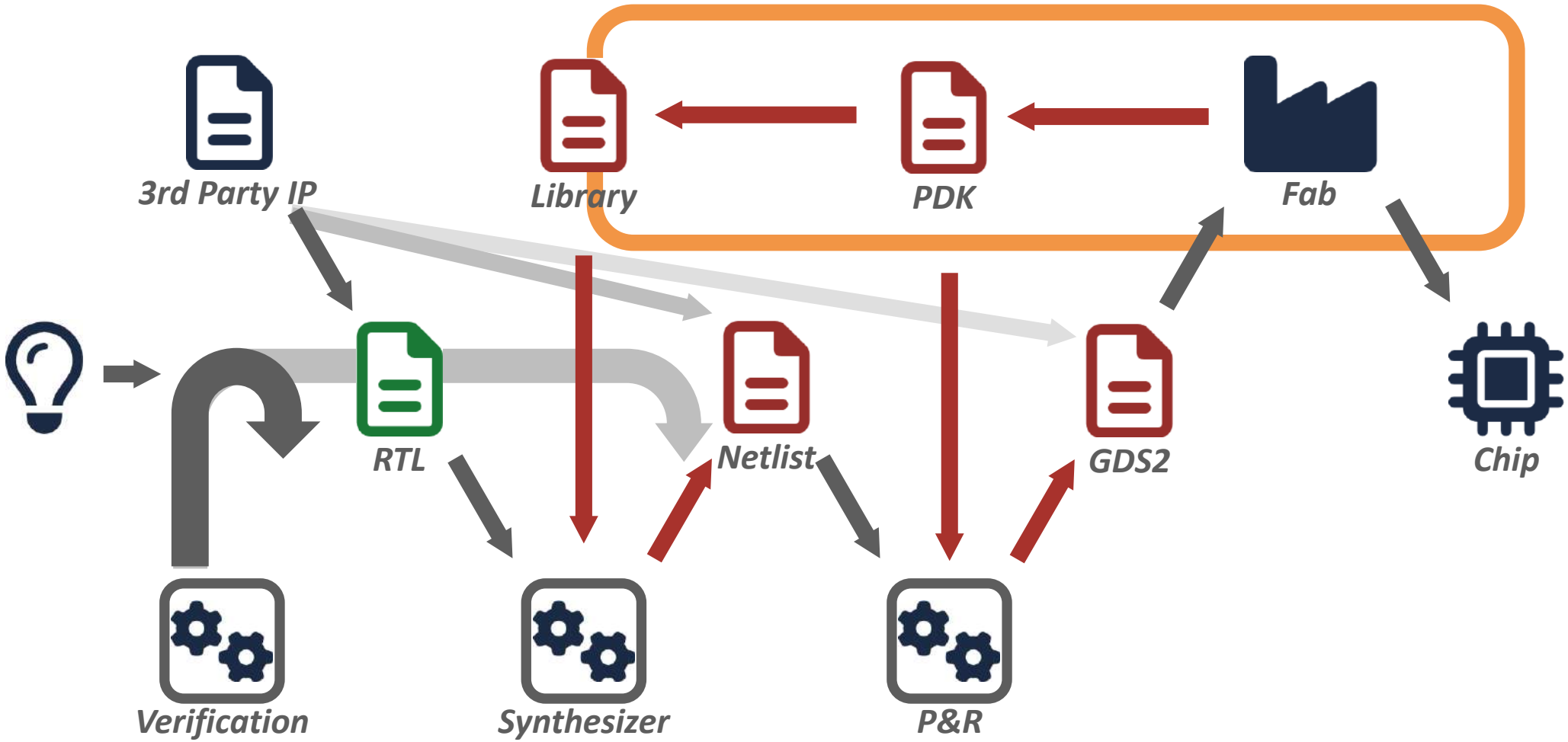
Icons taken from free icons from fontawesome.com

Simplified IC design flow: proprietary tools



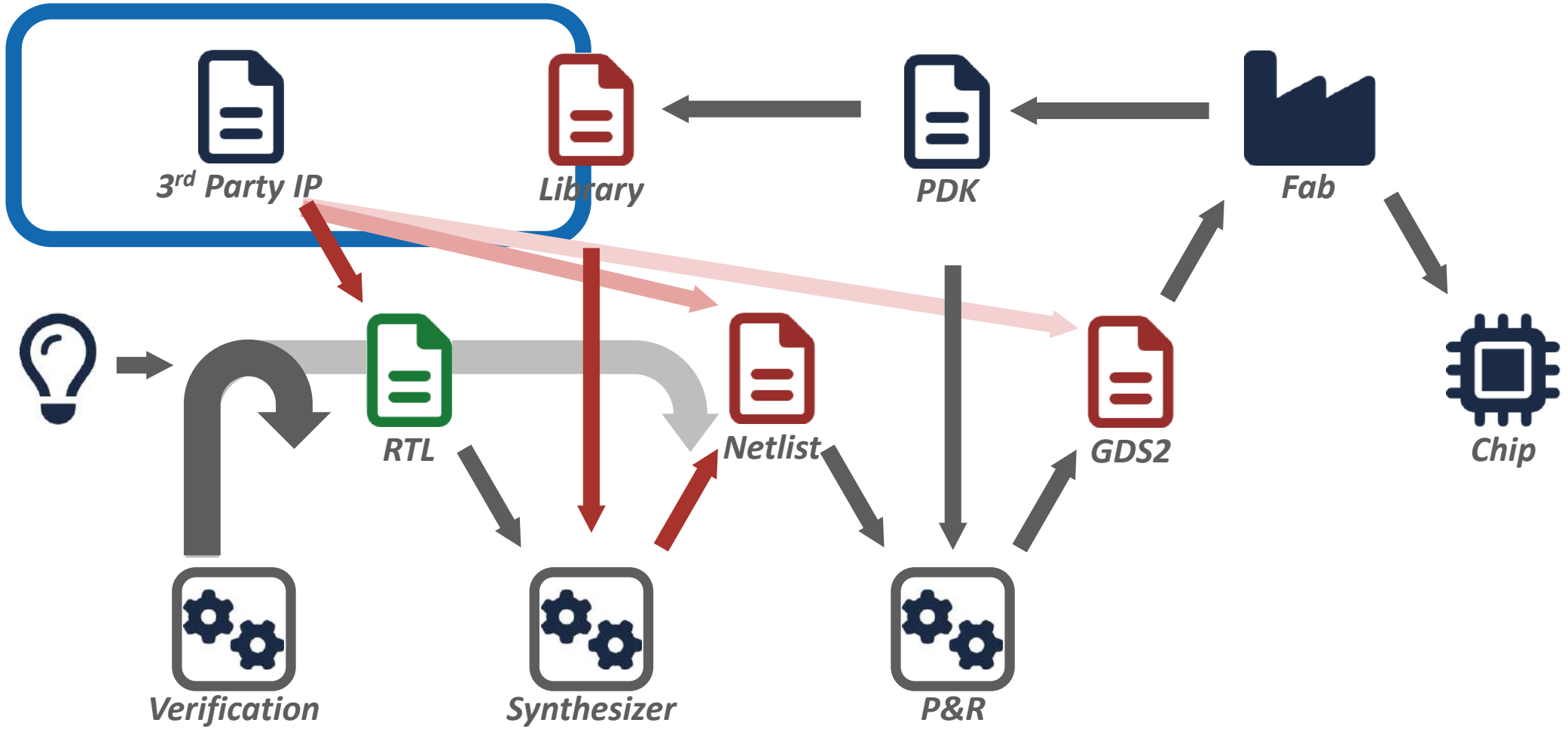
EDA vendors limit the output of their tools

Simplified IC design flow: technology provider



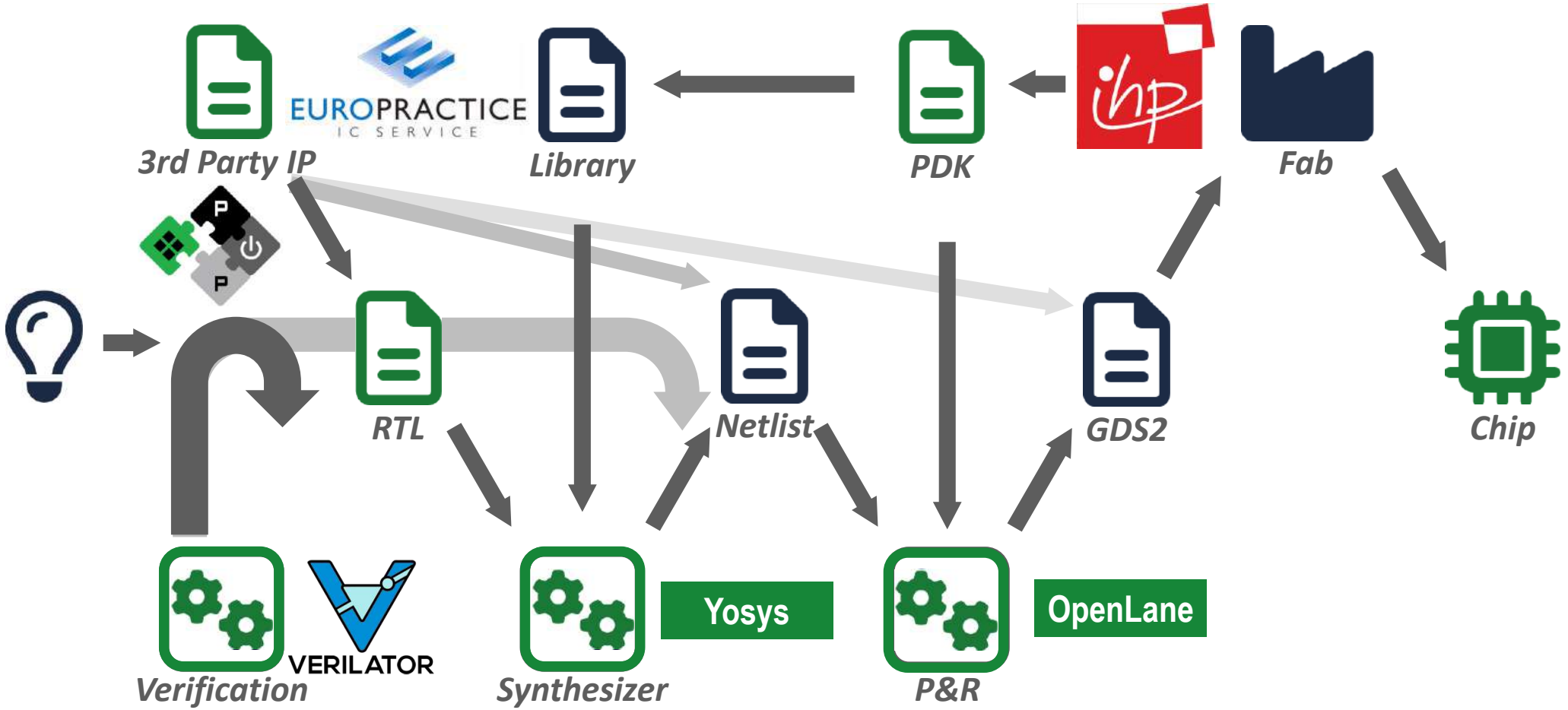
Fabs do not make PDK information accessible

Simplified IC design flow: 3rd party IP



3rd party IP when included can limit what can be open sourced

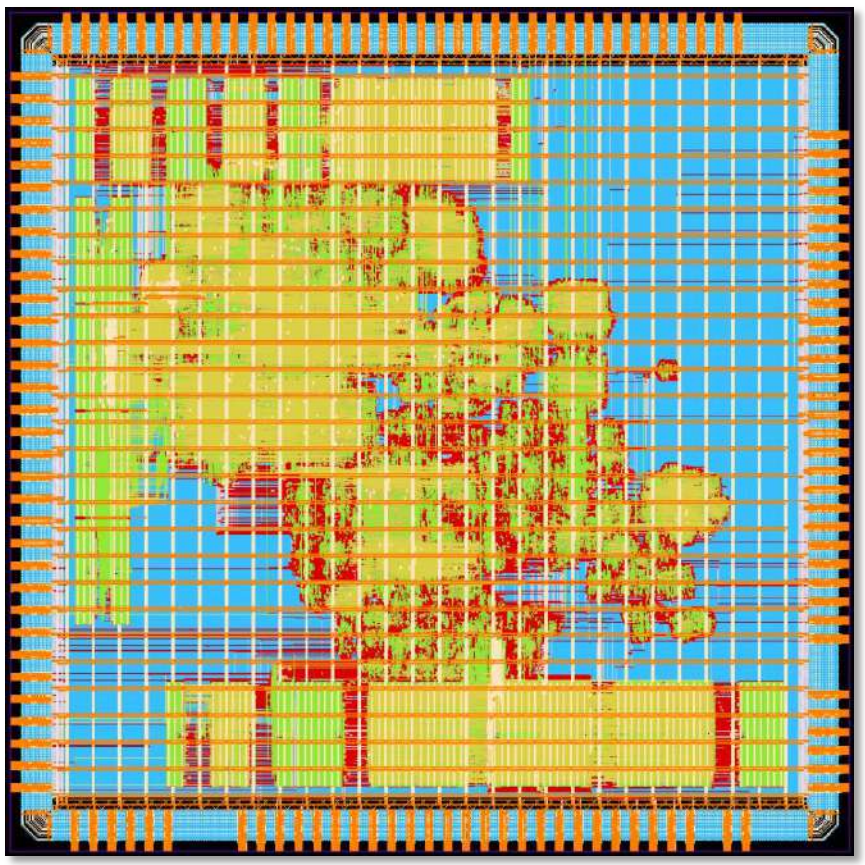
Simplified IC design flow: road to opennes



We are getting there, first fully open chips are underway

Iguana, Linux capable fully-open RISC-V processor.

- **Designed using IHP 130nm**
  - European Open PDK
  - Tape-out July 2023
- **Mostly open flow**
  - Some parts still rely on proprietary tools/IP
  - Next version 4Q23 fully open



What is PULP doing to maintain our cores?

- **We (ETHZ and University of Bologna) are research groups**
  - Motivated to develop new architectures and systems
  - We needed efficient RISC-V cores (and peripherals) for our work
  - Not so good (or interested) in providing industrial level support for these cores
- **We need help to**
  - Provide support
  - Develop industrial verification
  - Governance of open source repositories
- **Happy to receive this help from**
  - Open HW group (Ariane -> CVA6, RI5CY -> CV32E40P)
  - LowRISC (ZeroRiscy -> Ibex)
  - EU projects (Tristan/Isolde), Europractice

Open source HW is making great strides

- **RTL level open source hardware is quite established**
  - (among others) PULP based solutions are widely used in Industry and Academia
- **More openness requires solutions for Technology, EDA, 3rd party IP providers**
  - Open PDKs (slowly on the way)
  - Open source EDA and/or more support from existing EDA vendors
  - Lack of IP to make it harder to design impactful systems
- **Efforts underway to support Open HW**
  - Non-profit organizations (OpenHW, RISC-V), EU projects (TRISTAN/ISOLDE), Supporting groups (Europractice)
- **IC Design is an expensive business, there will always be a financial aspect**
  - Open source HW is an enabler, lowers costs and access, but does not make IC Design free

More work and support is needed to make open source HW viable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