PULP within the Open Source Hardware Landscape

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PULP Platform
Open Source Hardware, the way it should be!
Parallel Ultra Low Power (PULP) Platform

- Research on open-source energy-efficient computing

Led by Luca Benini

Involves ETH Zürich (Switzerland) and University of Bologna (Italy)

Large group of almost 100 people
We have designed and tested more than 50 PULP ICs

<table>
<thead>
<tr>
<th>Year</th>
<th>Number</th>
<th>Chip Name</th>
<th>Technology</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2013</td>
<td>(3)</td>
<td>PULPv1</td>
<td>STM 28FDSOI</td>
<td>Multi-core processor</td>
</tr>
<tr>
<td>2014</td>
<td>(5)</td>
<td>Diana</td>
<td>UMC 65</td>
<td>4-core system with approximate FPUs</td>
</tr>
<tr>
<td>2015</td>
<td>(10)</td>
<td>Fulmine</td>
<td>UMC 65</td>
<td>4-core system with ML and Crypto accelerators</td>
</tr>
<tr>
<td>2016</td>
<td>(3)</td>
<td>VivoSoC 2.001</td>
<td>SMIC 130</td>
<td>Mixed signal system for biosignal acquisition</td>
</tr>
<tr>
<td>2017</td>
<td>(2)</td>
<td>Mr. Wolf</td>
<td>TSMC 40</td>
<td>8+1 core IoT processor</td>
</tr>
<tr>
<td>2018</td>
<td>(6)</td>
<td>Poseidon</td>
<td>GF 22FDX</td>
<td>Dual 64bit RISC-V core, 32bit Microcontroller system, ML accelerator</td>
</tr>
<tr>
<td>2019</td>
<td>(7)</td>
<td>Baikonur</td>
<td>GF 22FDX</td>
<td>Dual 64bit RISC-V core, 3x 8-core snitch clusters, Body biasing test vehicle</td>
</tr>
<tr>
<td>2020</td>
<td>(3)</td>
<td>Dustin</td>
<td>TSMC 65</td>
<td>IoT processor with 16 cores and QNN enhancements</td>
</tr>
<tr>
<td>2021</td>
<td>(7)</td>
<td>Kraken</td>
<td>GF 22FDX</td>
<td>IoT processor with Spiking Neural and Ternary Inference Engines</td>
</tr>
<tr>
<td>2022</td>
<td>(9)</td>
<td>Occamy</td>
<td>GF 12LPP</td>
<td>ML accelerator with 216 + 1 cores and HBM interface</td>
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</tbody>
</table>

Check [http://asic.ethz.ch](http://asic.ethz.ch) for all our chips
Including some very complex designs like Occamy

- Chiplet based design
- 2x Compute chiplets (Occamy)
  - 216+1 RISC-V cores
  - 0.75 TFLOP/s for the system
  - GF12LPP
  - Running at 1 GHz
- 2x 16GB HBM DRAMs
- Silicon Interposer
  - GF 65nm 26mm x 23mm
- Waiting for assembly to finish

More on Occamy – https://pulp-platform.org/occamy/
All of our designs are open source hardware

- All our development is on GitHub using a permissive license
  - HDL source code, testbenches, software development kit, virtual platform
  
https://github.com/pulp-platform

- Allows anyone to use, change, and make products without restrictions.

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What PULP provides is a box of building blocks.

<table>
<thead>
<tr>
<th>RISC-V Cores</th>
<th>Platforms</th>
<th>Interconnect</th>
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</thead>
<tbody>
<tr>
<td>RI5CY 32b</td>
<td>Single Core</td>
<td>Logarithmic interconnect</td>
</tr>
<tr>
<td>Ibex 32b</td>
<td>• PULPino</td>
<td>APB – Peripheral Bus</td>
</tr>
<tr>
<td>Snitch 32b</td>
<td>• PULPissimo</td>
<td>AXI4 – Interconnect</td>
</tr>
<tr>
<td>Ariane 64b</td>
<td>Multi-core</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• OpenPULP</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Mr. Wolf</td>
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<tr>
<th>Accelerators</th>
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<td>HWCE (convolution)</td>
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Source Hardware Landscape
How does PULP collaborate with 3rd parties?
The open model led to successful industry collaborations

**Arnold (GF22)**
eFPGA with RISC-V core

**Vega (GF22)**
IoT Processor with ML acceleration

**Marsellus (GF22)**
IoT Processor with low power modes and event based computing

**Siracusa (TSMC16)**
IoT Processor with NVM technology
And many have used our work for their research.
In the last 20 years IC Design has changed a lot

What used to be a complete chip is now a small part of a SoC!
There is so much that makes up a modern SoC
In a typical design, innovation is only in a limited scope

Open-source silicon-proven SoC template helps concentrate work where it counts

User-Space Software

Kernel-Space Software

Hardware

HETEROGENEOUS APPLICATION

ACCELERATED KERNEL

LINUX KERNEL

PULP DRIVER

VIRTUAL MEMORY MANAGEMENT LIBRARY

HW ABSTRACTION LIBRARY

User-Space Software

Kernel-Space Software

Hardware

Open-source silicon-proven SoC template helps concentrate work where it counts

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Simplified IC design flow

3rd Party IP -> Library

RTL -> Netlist

Synthesizer

P&R

Verification

GDS2 -> Chip

PDK

Fab

Icons taken from free icons from fontawesome.com
Simplified IC design flow: at the moment only RTL

- RTL
- 3rd Party IP
- Library
- PDK
- Fab
- Chip
- Synthesizer
- Netlist
- P&R
- Verification

Icons taken from free icons from fontawesome.com
Simplified IC design flow: proprietary tools

EDA vendors limit the output of their tools
Simplified IC design flow: technology provider

3rd Party IP

Library

PDK

Fab

Veriﬁcation

RTL

Synthesizer

Netlist

P&R

GDS2

Chip

Fabs do not make PDK information accessible
3rd party IP when included can limit what can be open sourced
We are getting there, first fully open chips are underway
Iguana, Linux capable fully-open RISC-V processor.

• Designed using IHP 130nm
  • European Open PDK
  • Tape-out July 2023

• Mostly open flow
  • Some parts still rely on proprietary tools/IP
  • Next version 4Q23 fully open
What is PULP doing to maintain our cores?

• **We (ETHZ and University of Bologna) are research groups**
  • Motivated to develop new architectures and systems
  • We needed efficient RISC-V cores (and peripherals) for our work
  • Not so good (or interested) in providing industrial level support for these cores

• **We need help to**
  • Provide support
  • Develop industrial verification
  • Governance of open source repositories

• **Happy to receive this help from**
  • Open HW group (Ariane -> CVA6, RI5CY -> CV32E40P)
  • LowRISC (ZeroRiscy -> Ibex)
  • EU projects (Tristan/Isolde), Europractice
Open source HW is making great strides

- RTL level open source hardware is quite established
  - (among others) PULP based solutions are widely used in Industry and Academia

- More openness requires solutions for Technology, EDA, 3rd party IP providers
  - Open PDKs (slowly on the way)
  - Open source EDA and/or more support from existing EDA vendors
  - Lack of IP to make it harder to design impactful systems

- Efforts underway to support Open HW
  - Non-profit organizations (OpenHW, RISC-V), EU projects (TRISTAN/ISOLDE), Supporting groups (Europractice)

- IC Design is an expensive business, there will always be a financial aspect
  - Open source HW is an enabler, lowers costs and access, but does not make IC Design free

More work and support is needed to make open source HW viable