Spatzformer – Reconfigurable Dual-Core RVV Cluster for Mixed Workloads

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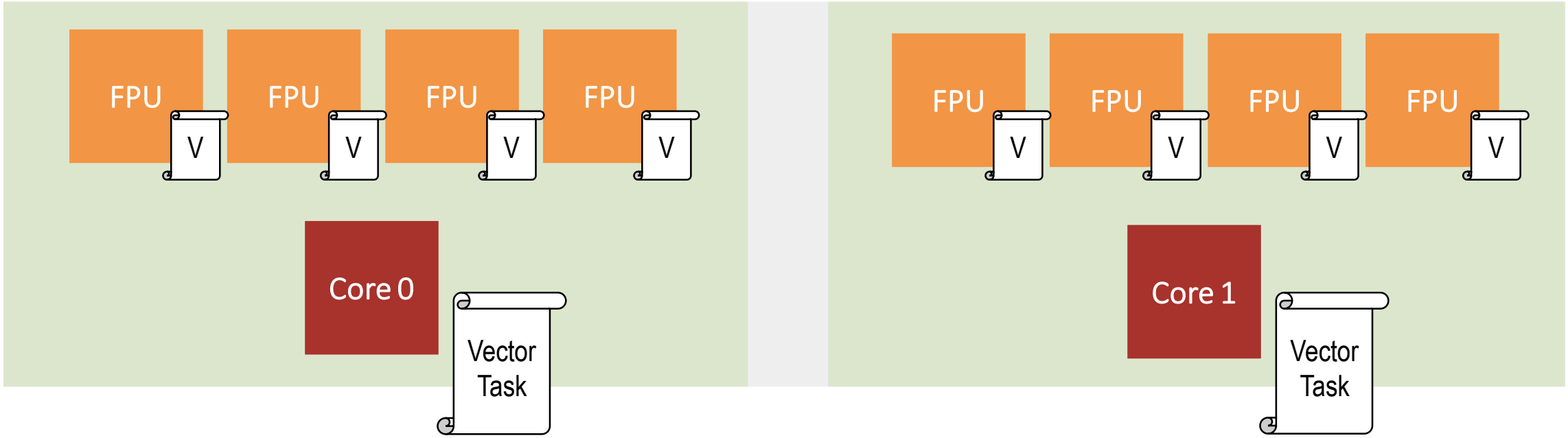
Open Source Hardware, the way it should be!

The problem – **Mixed scalar-vector workload**

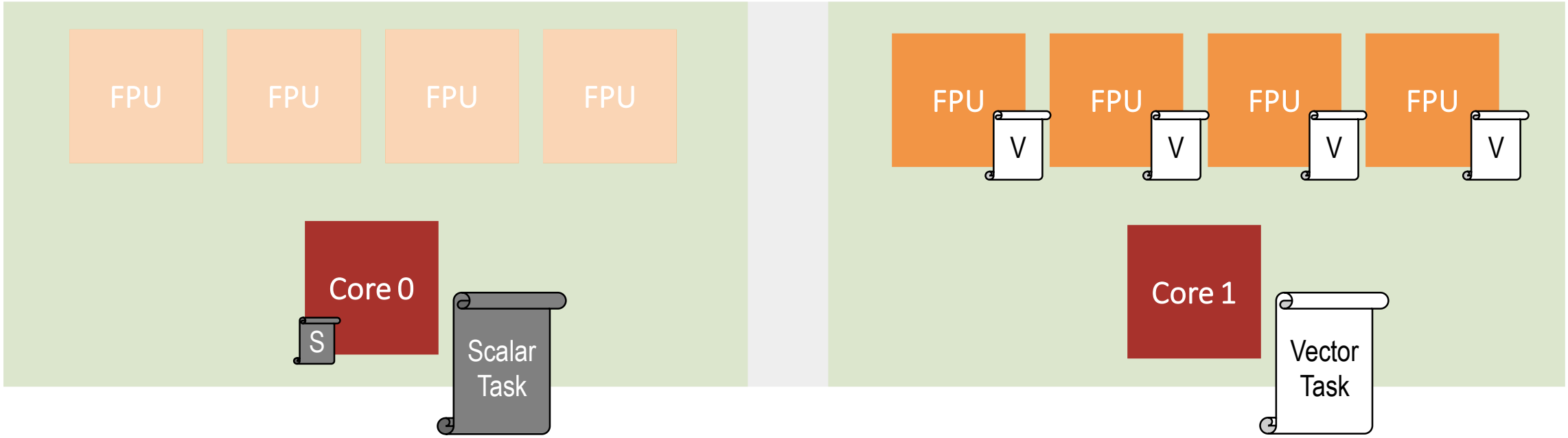
Dual-core vector architecture



Each core runs a **vector task** – We can reach **100% FPU utilization**!

The problem – **Mixed scalar-vector workload**

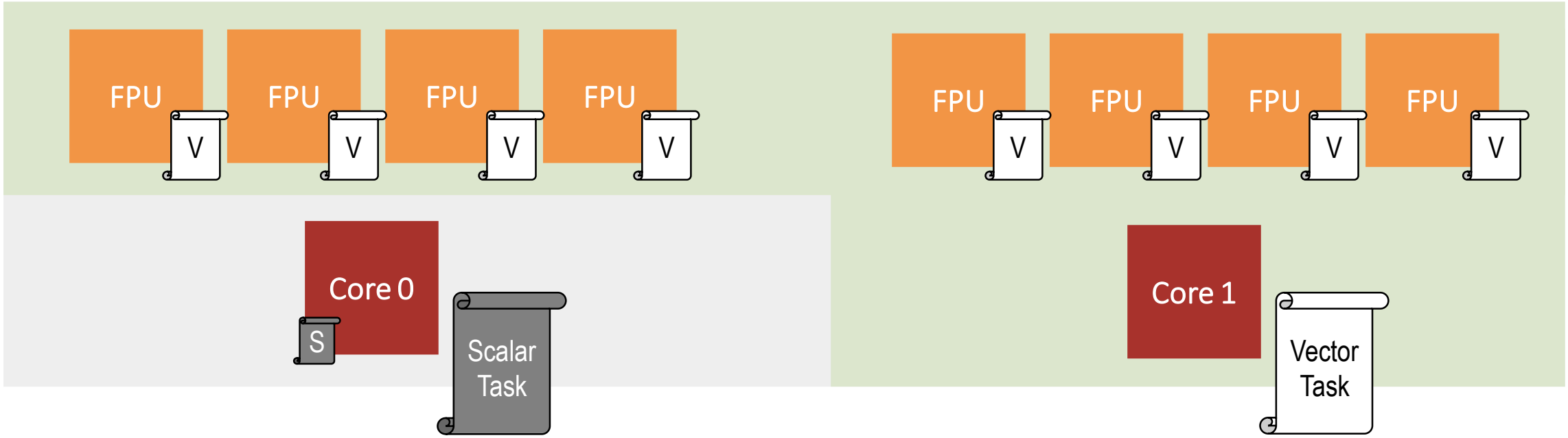
Dual-core vector architecture



Mixed scalar-vector workload – Half of the resources are not used!

Two small vector processors... **Or a larger one**?

Reconfigurable vector architecture



- **Core 1** can **exploit all** the vector **FPUs**
- **Core 0** is free to run **scalar tasks**
- The **architecture** can be **reconfigured** at **runtime**

Want to know more?

We added the **reconfigurability** support to a highly-optimized **RISC-V V dual-core cluster**

We **implemented** the architecture
In **12-nm** technology

- Does this work?
- How to change configuration?
- What is the cost of this feature?
- Power, performance?

Check out our poster stand ☺