ETH zürich

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

Open-source EDA for chip design: Where are we now, what is next?

Open Source at CERN in 2026/2027

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pulp-platform.org

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company/pulp-platform

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PULP Platform

Open Source Hardware, the way it should be!

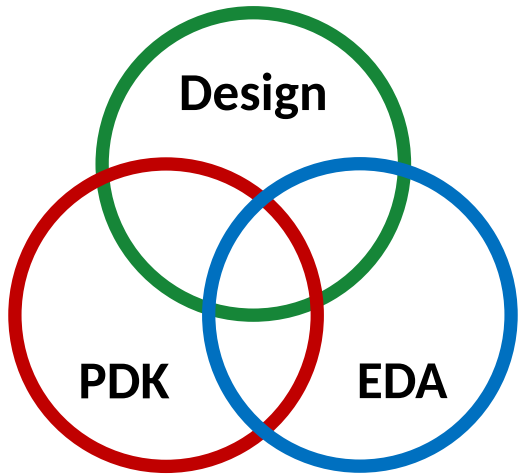
Open IC Design has three different components

Design

- RTL / HDL descriptions (quite common)
- Schematics / Physical Design (may have dependencies to technology information)

Tools (EDA)

- Front-end tools (Synthesis)
- Back-end tools (Placement and Routing)
- Verification tools (Simulation)



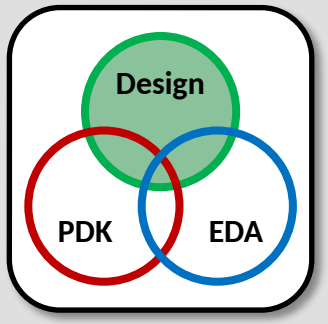
Manufacturing (PDK)

- Design rules for manufacturing (separation, minimum width of metals)
- Layer stack information for parasitics (thickness, dielectric constants..)
- Device models (SPICE parameters) for simulation

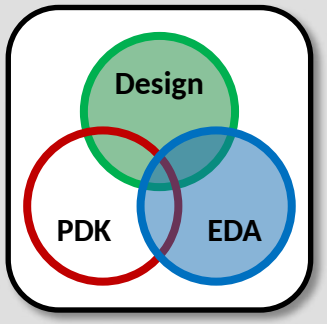
This makes open IC design a bit different from FPGA and PCB design

Notice that open parts in IC flow are independent

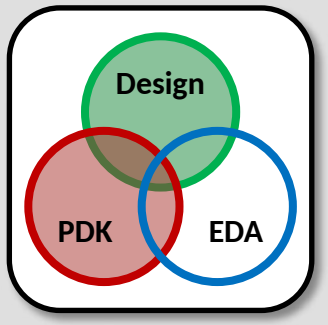
It is possible to use **open design** with closed EDA and closed PDK *(Picobello, Flamingo)*



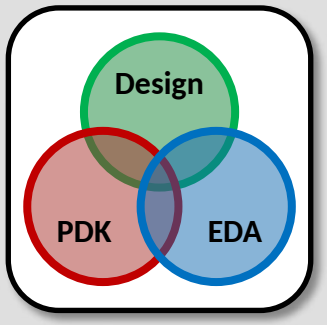
Or have **open designs** using **open EDA** on a closed PDK *(Torik)*



As well as having **open designs** using commercial EDA with **open PDKs** *(EZ Library)*



But end goal is to allow **open designs** using **open EDA** and **open PDKs** *(Basilisk, Mlem, Thomy)*



On our journey at PULP we experienced all combinations

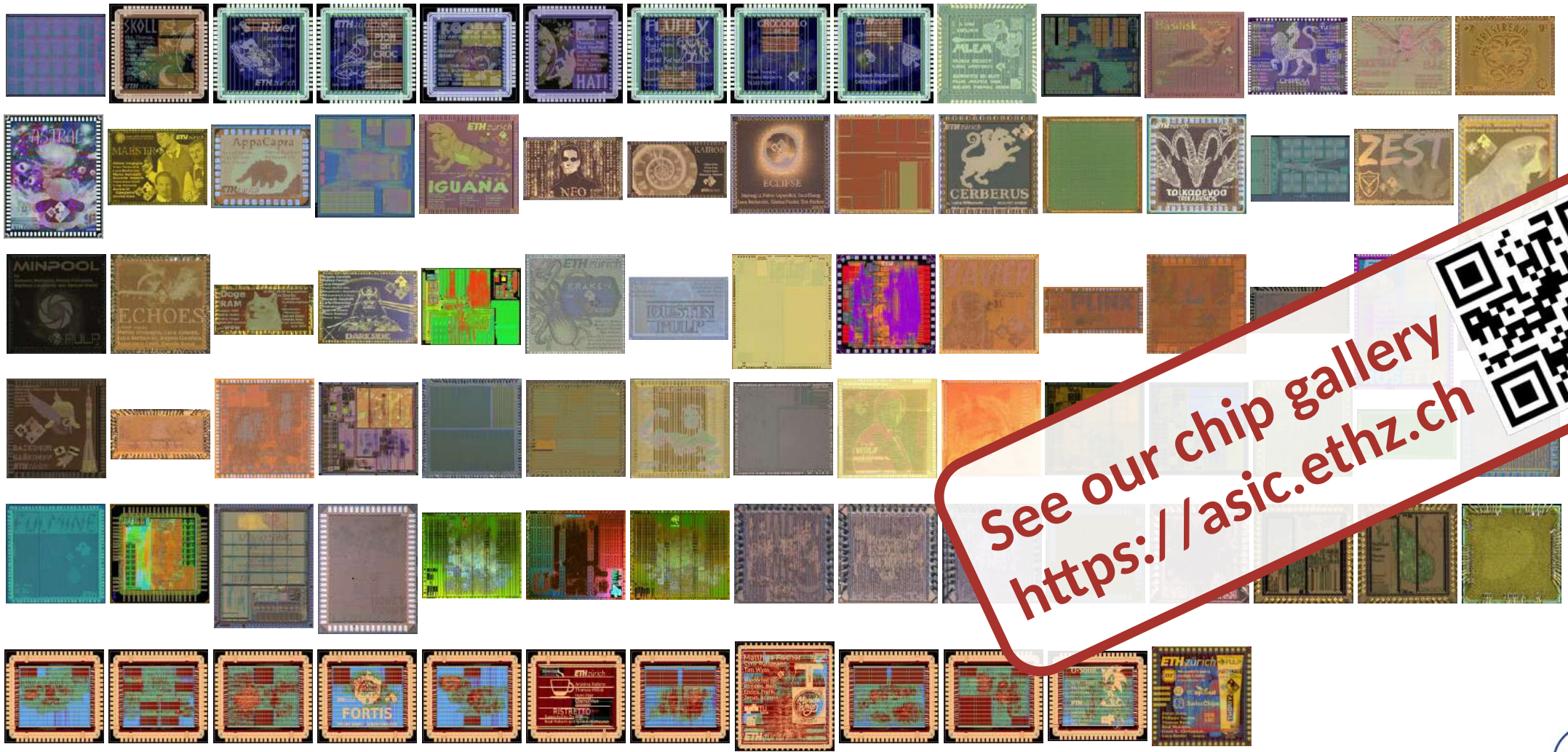
PULP platform has a long history in open source HW

- **PULP (Parallel Ultra Low Power) Platform started in 2013**
  - With the appointment of Luca Benini as professor to ETH Zurich while keeping his professorship at University of Bologna
- **From the beginning the group was active in open source hardware**
  - First open source project was PULPino, released in 2016
- **Starting in 2015 group started developing RISC-V based systems**
  - CVA6, CVE32E40P, Ibex/CVE2 all started their life as PULP platform projects



The PULP team is about 100 people Both in CH and IT

As PULP group we have designed more than 85 ASICs



Several of these are end-to-end open-source designs



We can make larger end-to-end open-source chips

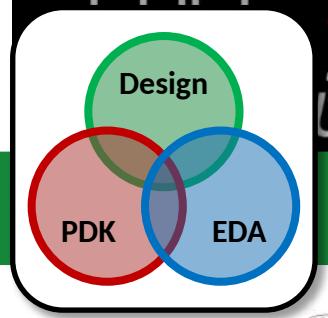
Booting Linux on

Basilisk

an end-to-end open-source
64-bit RISC-V SoC
in IHP 130nm BiCMOS

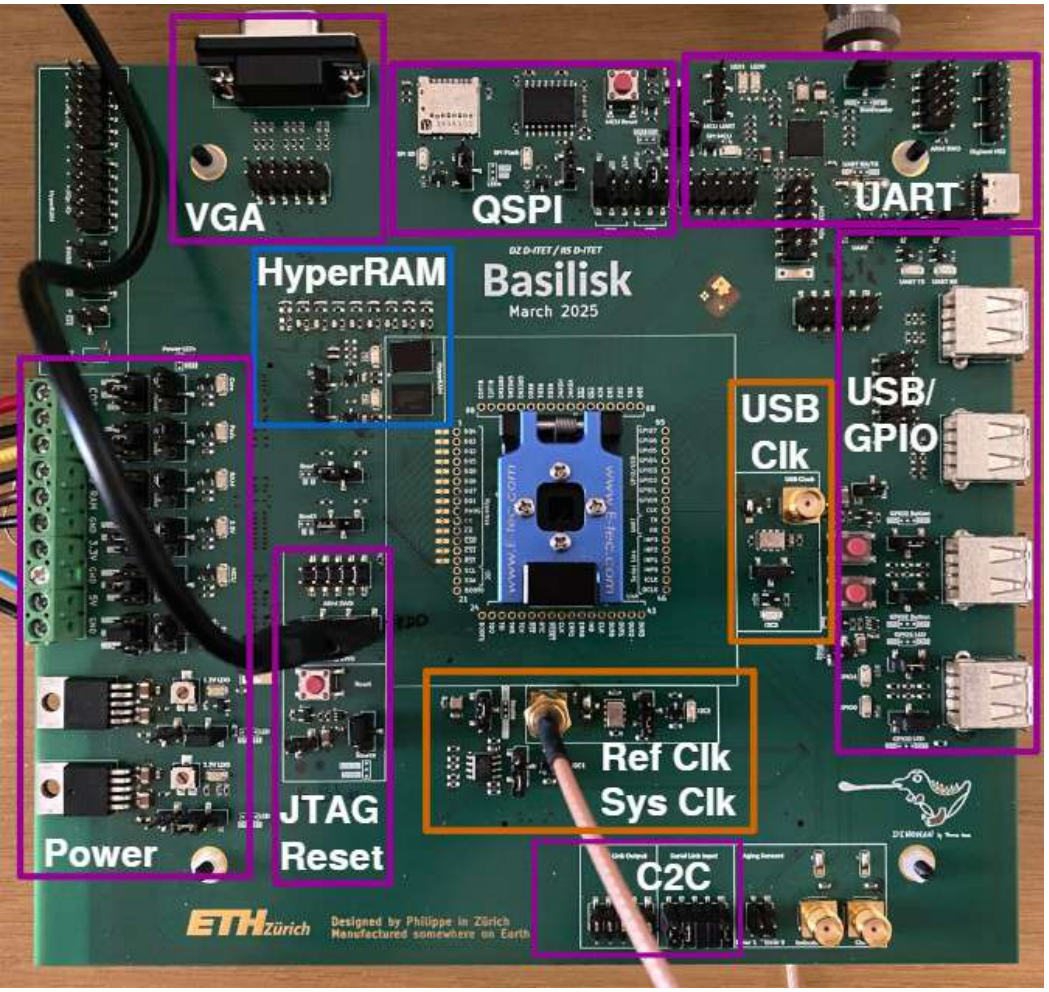


- **Open Design**
  - Cheshire with CVA6
- **Open EDA**
  - Yosys (with –slang)
  - OpenROAD
  - KiCAD (for board)
- **Open PDK**
  - IHP 130
  - Open standard cells
  - Memory macros



github.com/pulp-platform/cheshire-

Basilisk is proof that we can already make large(r) designs



Designed in IHP 130nm OpenPDK
- **34mm²** (6.25mm x 5.50mm)
- **~5× larger** than previous end-to-end OS designs
- 2.7 MGE total, 1.14MGE logic
- 24 SRAM macros (114 KiB)
- **62MHz** at nominal voltage (1.2V)

RV64GC design runs Linux

Active collaboration with

arxiv.org/pdf/2505.10060

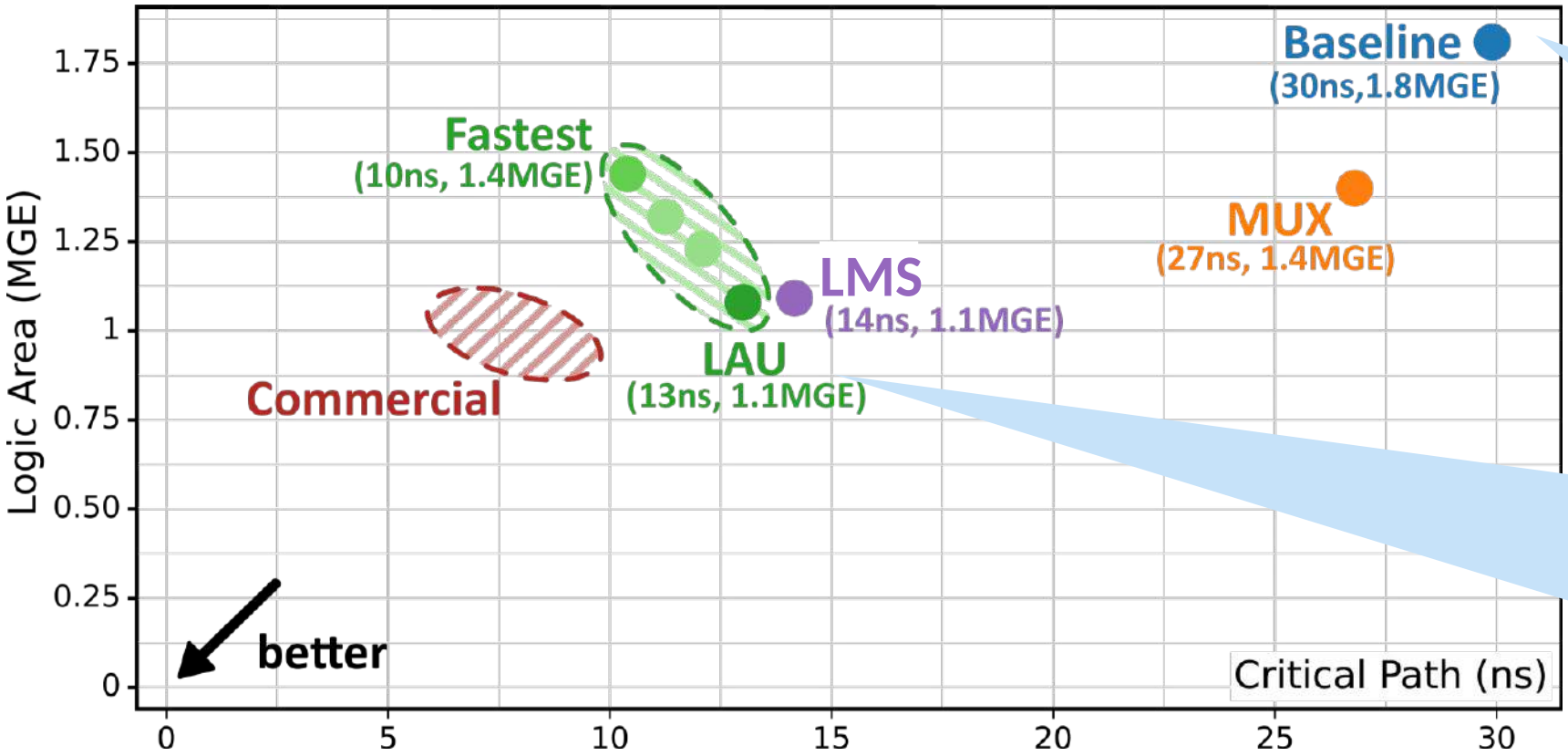
Just how good are the Open-EDA tools?



- **Main Open-EDA tools are definitely usable**
  - Yosys, ABC, OpenRoad, Klayout, ngspice, xschem, verilator, gtkwaves, openSTA… work like their commercial counterparts. Complete designs are possible
  - In mature nodes the PPA difference is within 10-15%,
    It gets better as we have more experience with the process node
  - We use them for teaching and also in a number of projects
- **There are gaps (and bugs)**
  - Open source developers usually do not design larger chips in more modern nodes
    - Some simplifications that work well in 130nm do not work that well in 22nm
    - Color aware routing for example is not yet available
  - Some ‘features’ are not so popular for open-source developers (Scan insertion..)

But tools will only improve and the gaps will continue to close

Closing the PPA gap to commercial EDA





We can get there!

(timing-aware synth., elaboration+optimizations, pre-optimized blocks libs, physically aware synthesis…)

Open-source EDA is not a all or nothing decision



- **You can mix and match open-source EDA tools with proprietary tools**
  - Some configuration is required, but both flows rely on the same information
  - Flows that contain a mix of tools are easy to realize
- **Not being limited by license costs but by available CPUs gives opportunities**
  - Makes public (or cross partner) CI flows much easier
  - Being able to run many iterations (with small variations) opens new possibilities
  - Early evaluations of technical choices do not require signoff accuracy
- **Open source EDA is also not the enemy of commercial companies**
  - Open-source EDA allows developing skills needed for EDA companies
  - Allows EDA companies to concentrate their efforts on differentiating features
- **Lowering barriers: OS EDA allows you to experiment before investing**
  - You can see if your company can venture into IC Design by experimenting at your own pace

Reliable collection of open source tools is essential!

- **Most open source developers have their own idea about the environment**
  - Getting several independent tools to work at the same time is very demanding work
  - Preparing/sharing lectures require you to be able to point to a reliable image

`https://github.com/iic-jku/IIC-OSIC-TOOLS` to the

README Apache-2.0 license

IIC-OSIC-TOOLS

DOI 10.5281/zenodo.15044726

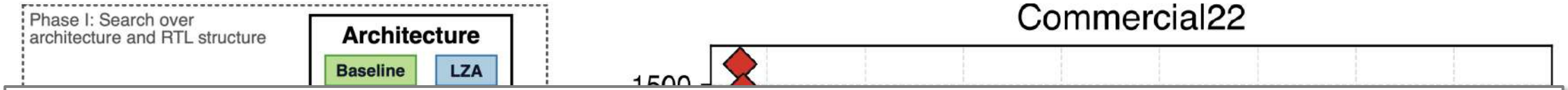
This environment is based on the efabless.com FOSS-ASIC-TOOLS.

IIC-OSIC-TOOLS (Integrated Infrastructure for Collaborative Open Source IC Tools) is an all-in-one Docker container for open-source-based integrated circuit designs for analog and digital circuit flows. The CPU architectures `x86_64/amd64` and `aarch64/arm64` are natively supported based on Ubuntu 24.04 LTS (since release `2025.01`). This collection of tools is curated by the Department for Integrated Circuits (DIC), Johannes Kepler University (JKU).

Thanks Harald ☺

The more exciting opportunity, making EDA tools better

- **FP32 adders optimized with ABC and Synopsys Design Compiler**



Constraint	Adder design	Synthesis flow	IHP130		ASAP7		Commercial22	
			Area [μm^2]	Delay [ns]	Area [μm^2]	Delay [ns]	Area [μm^2]	Delay [ns]
Fastest	BASELINE-OPT	Baseline	13'824	3.46	136	0.516	939	0.576
	LZA-OPT	Baseline	17'760	3.10	181	0.458	1'145	0.525
	LZA-OPT	LMS-assisted	18'326	2.98	220	0.422	1'298	0.502
	LZA-ABC balanced	Proposed	22'614	2.40	224	0.359	1'294	0.421
	LZA-ABC fast	Proposed	27'912	**2.15**	303	**0.322**	1'481	**0.375**
Area ≤ LZA-OPT	LZA-ABC balanced	Proposed	17'421	**2.70**	180	**0.400**	1'016	0.440
	LZA-ABC fast	Proposed	–	–	–	–	1'041	**0.420**
Delay ≤ LZA-OPT	LZA-ABC balanced	Proposed	**15'736**	3.00	**159**	0.440	**652**	0.520
	LZA-ABC fast	Proposed	21'519	3.00	212	0.440	735	0.520

Better designs achieved by combining open + proprietary EDA tools

End-to-end open-source flows **REQUIRE** open PDKs

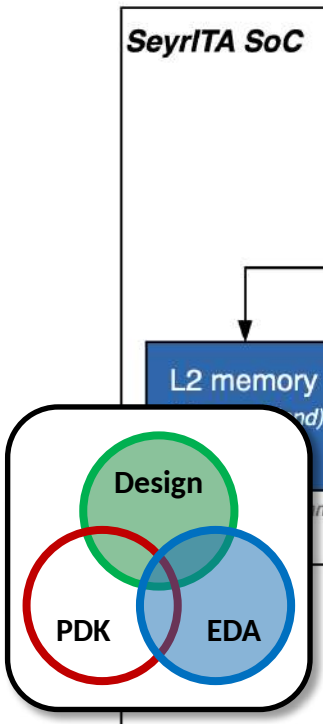
- **At the moment, the choice is limited**
  - Skywater 130nm
  - IHP 130nm
  - Globalfoundries 180MCU (will be abandoned soon)
- **Some are sort of available**
  - IC Sprout 55nm (taped out our first chip)
- **We need more open PDKs to design more relevant designs**
  - Something in the 65nm – 28nm range would be a **game changer**
  - **And we will soon have alternatives (to be announced in 2027, this is a done deal!)**

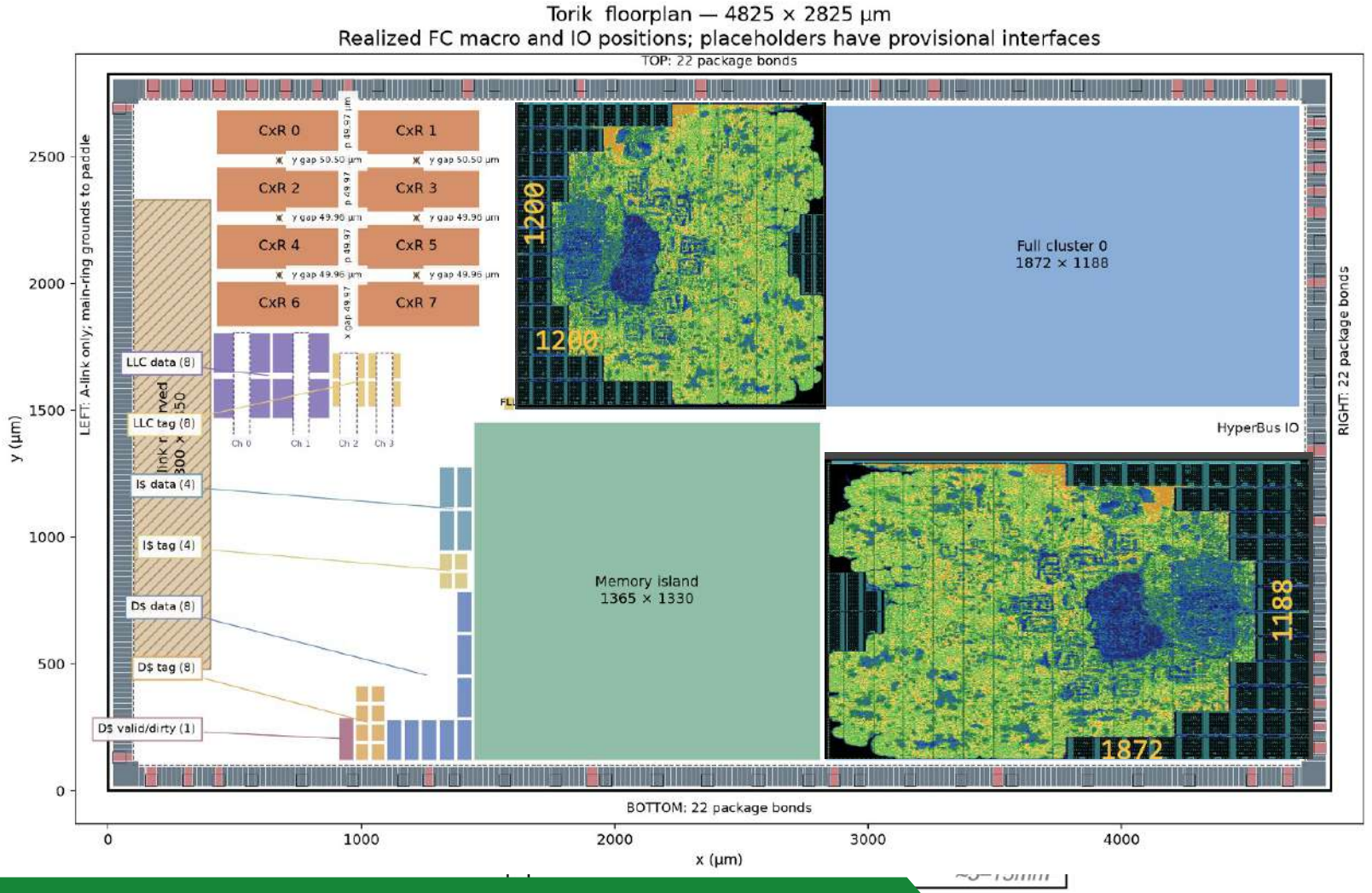


What do we do until we have open PDKs in scaled technologies?

Torik: our most ambitious project for embodied AI

- **Designi**
  - State of
- **Collabo**





(ITA)

ng work

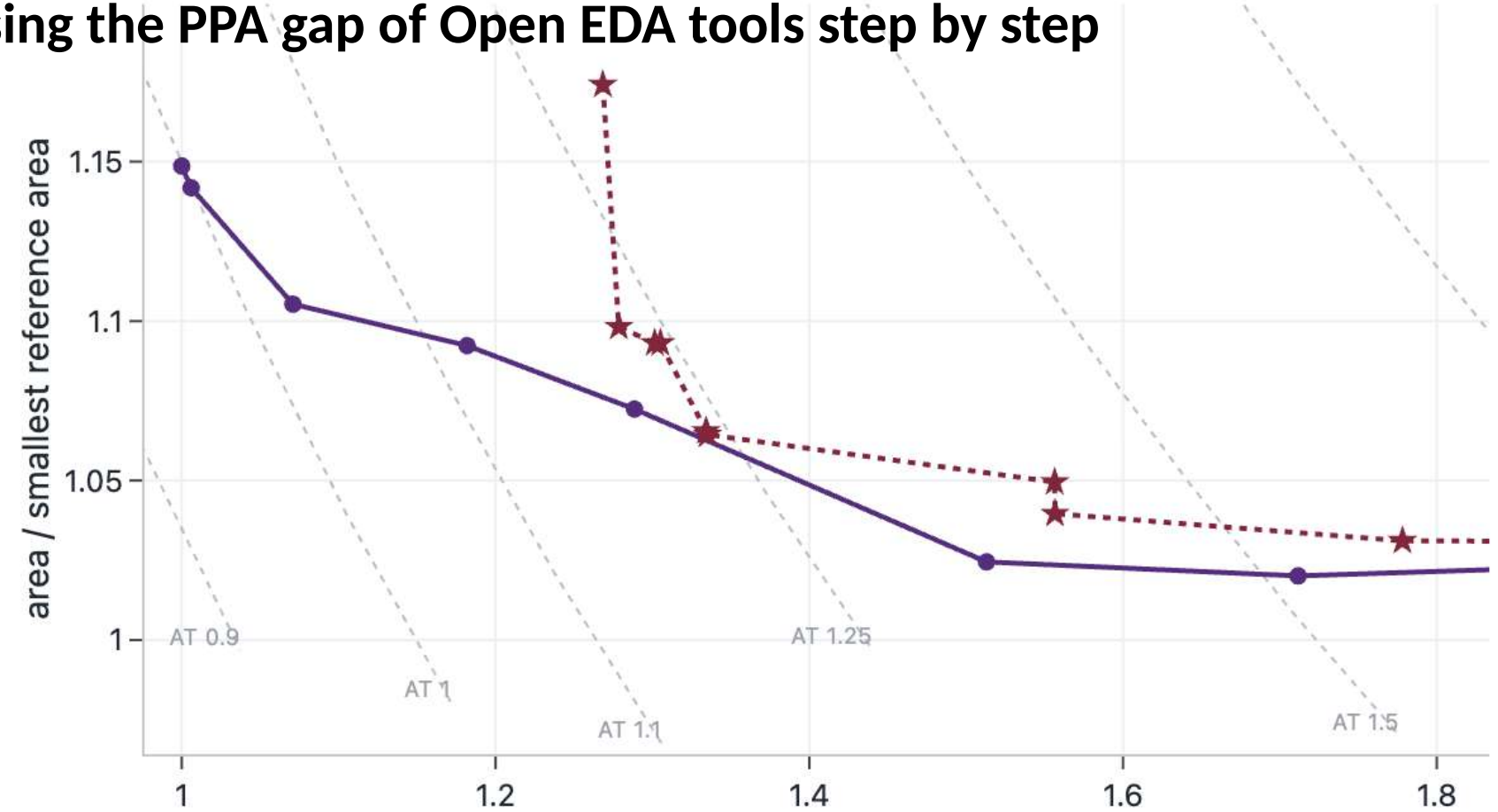
gn,
echnology
nter problems daily
solve them
em at a time
we will get it done

e-out

https://github.com/pulp-platform/

Using open source EDA with modern technologies

- **Closing the PPA gap of Open EDA tools step by step**



Achieving synthesis results that come close to proprietary tools

There is much more work to be done

- **Problems can only be solved once you encounter them**
  - Current 180-130nm PDKs do not allow designs beyond certain complexity
  - Issues that appear in larger designs are not (yet) encountered by community
  - Open PDKs in more advanced nodes will help the community to design more complex chips
- **Exchanging experience/information is key to go forward with EDA tools**
  - Not practical with closed PDKs, needs multi-party NDAs (like the CERN one)
  - We also need more open PDKs to be able to communicate issues quickly

Help is on the way, we will be getting new PDKs in 65-28nm range soon!

- **More designs results in more experience and helps fix more problems**
  - Bugs, issues are being uncovered when people try different things
    - Chips wth different aspect ratios uncovered a global placement issue recently
  - We are getting more designs and better results every day

Funding for Open Source EDA for Europe: **ODE4EC**

- **HORIZON-JU-CHIPS-2025-IA-EDA-two-stage**
  - 20MEUR funding from EU, total project **50MEUR**
  - Organized in three sub projects: Digital, Analog, Productivity
  - 3-year project, started in June 2026
- **Large consortium**
  - 24 partners (DIG), 27 partners (AMS), 24 partners (PIV)
  - From 14 Countries (AT, DK, FI, FR, DE, GR, HU, IT, LT, PT, SI, ES, SE, SE, CH, UK)
  - Includes broad participation from most open source contributors in EU
- **Great opportunity to close the gap**

`https://ode4ec.eu/`



The five lessons from our experience



- **Open source is needed to share designs and ideas efficiently**
  - And we can not build everything ourselves, modern SoCs are way to complex
- **Sharing beyond RTL level requires both open EDA, and open PDKs**
  - There are several roadblocks that prevent sharing in IC Design
  - These can only be addressed once there are PDKs that allow sharing
- **End-to-end open-source flows can already deliver complex working chips**
  - There is a gap to commercial EDA, but it is less than what people think
- **End-to-end open-source flows are great for training and teaching**
  - Being able to share all aspects of the flow allows us to make materials available to everyone
- **There are many interesting opportunities for open EDA**
  - There is more to do than just replicate what commercial EDA has been doing
  - Opportunities for disruptive developments that will push performance beyond current levels

EFCL SUMMER SCHOOL

on Open Source IC and system design

The Nicolaus Hotel, Bari (Puglia), Italy

July 5th - 9th, 2027

REGISTER NOW

Featuring a special event:

PULP Platform



http://pulp-platform.org @pulp_platform

Open source HW has a bright future



Sharing our **FLL** with others that need it

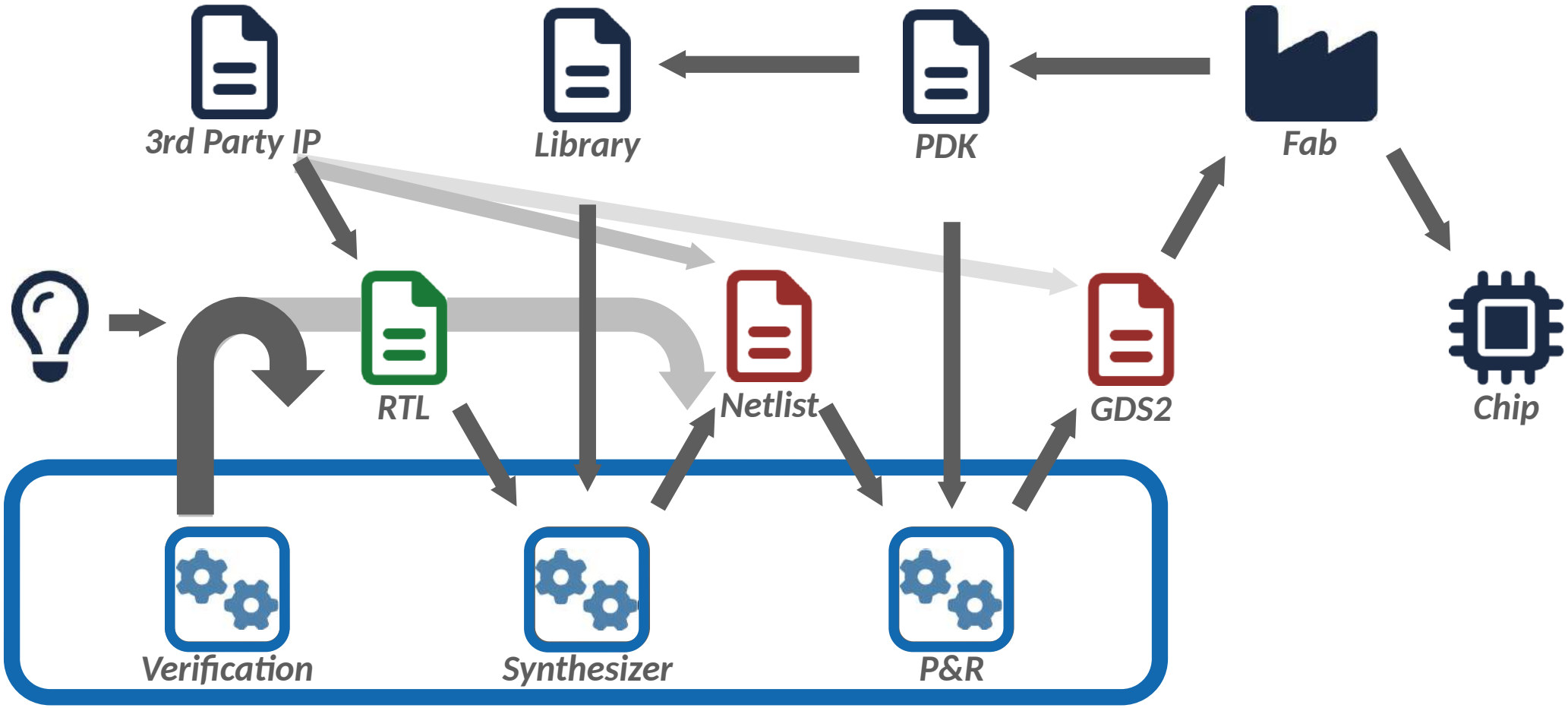


- **When you start designing in more modern technologies clock rates increase**
  - For 28nm and less clock rates of 500MHz – 2GHz are easily possible
  - It is difficult to bring such clocks externally, an internal clock generator could help
  - Good luck getting access to a low-cost clocking IP ☺
- **We designed an FLL (Frequency Locked Loop) back in 2016**
  - D. E. Bellasi and L. Benini, "Smart Energy-Efficient Clock Synthesizer for Duty-Cycled Sensor SoCs in 65 nm/28nm CMOS," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2322-2333, Sept. 2017, doi: 10.1109/TCSI.2017.2694322.
  - Ported and taped-out in many technologies: UMC65, TSCM65, GF22, GF12, TSMC7…

People have asked us repeatedly if we could share our FLL

.. and we really want to share our FLL, we know how much it helped us

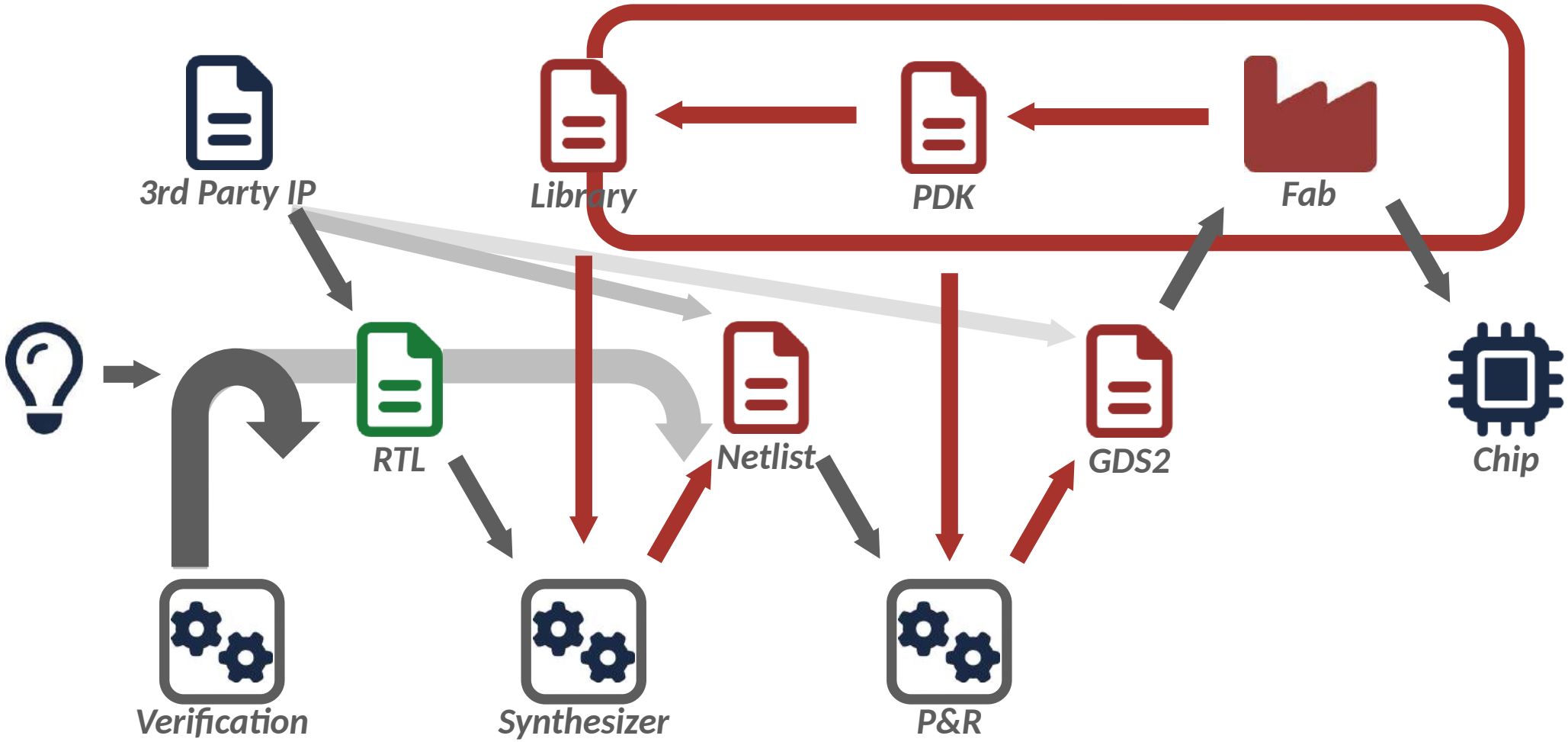
The output (and even scripts) of EDA vendors are closed



EDA vendors limit the output of their tools

Icons taken from free icons from fontawesome.com

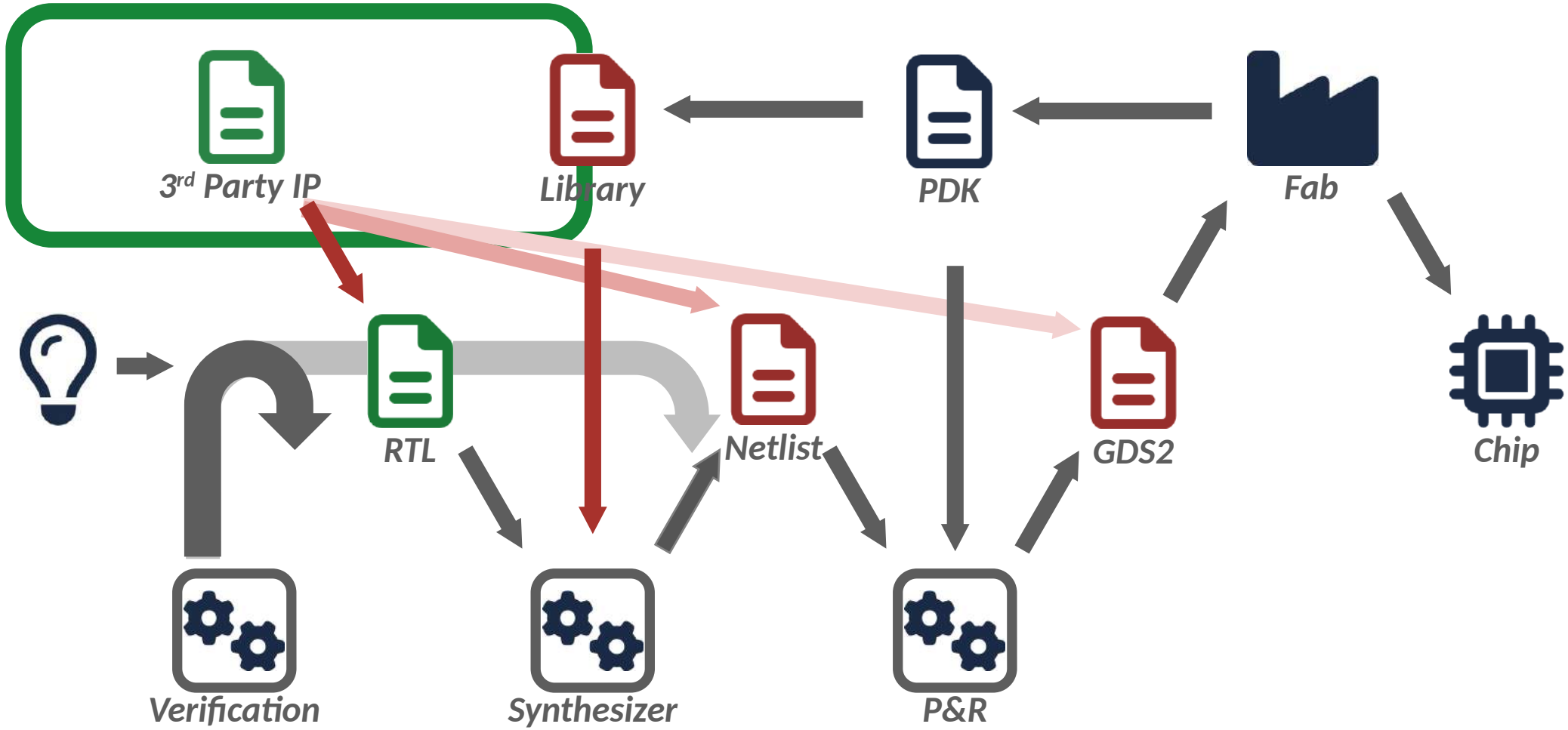
The chip will contain information from the PDK of the Fab



Fabs do not make PDK information accessible

Icons taken from free icons from fontawesome.com

Most designs will include some 3rd party IP



3rd party IP when included can limit what can be open sourced

Icons taken from free icons from fontawesome.com

Issues of sharing technology specific IP (like our FLL)



- **Assuming you have no objections from your own institution to share your IP**

The design requires technology data that is under NDA

- You can not share anything without getting permission from the technology provider
- Usually this requires a multi-party NDA

Your design may contain standard cells that come from a different provider

- You will have to contact the IP provider to ask for permission
- Our FLL for GF22 uses INVECAS standard cell libraries now owned by Synopsys
- In theory you can send a design WITHOUT the cells only references, and add the cells locally

You have used EDA tools with academic licenses for your design

- Most academic license agreements would not allow you to transfer the output to others
- You need to contact the EDA vendor and ask for their permission to share

Issues of sharing technology specific IP (like our FLL)

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This is a long and tedious process

On average it takes 6 months

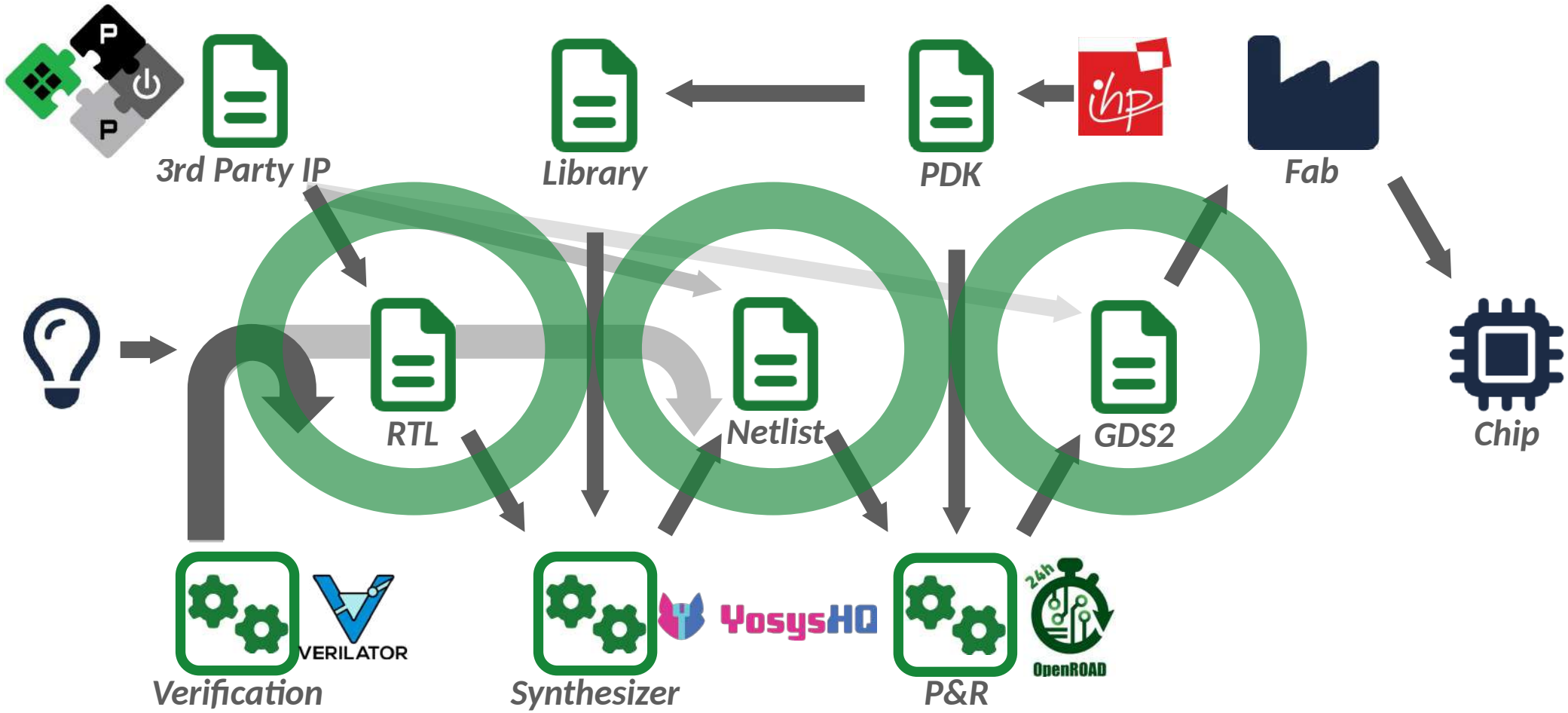
even with great support form everyone involved

Even worse this effort is

needed by the donor every single time

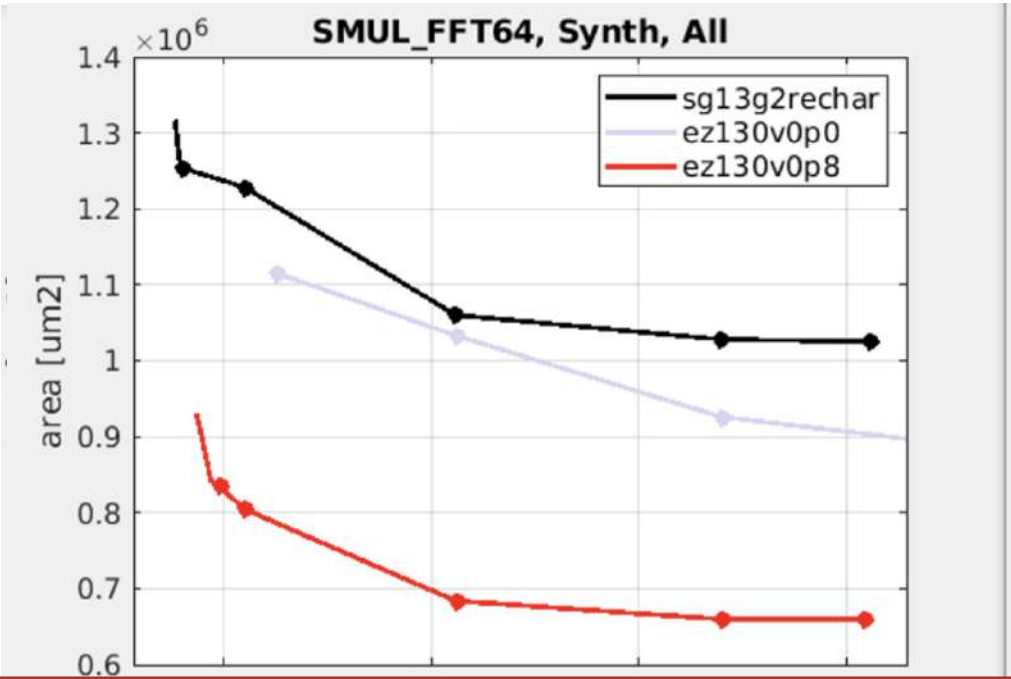
someone wants to use your IP

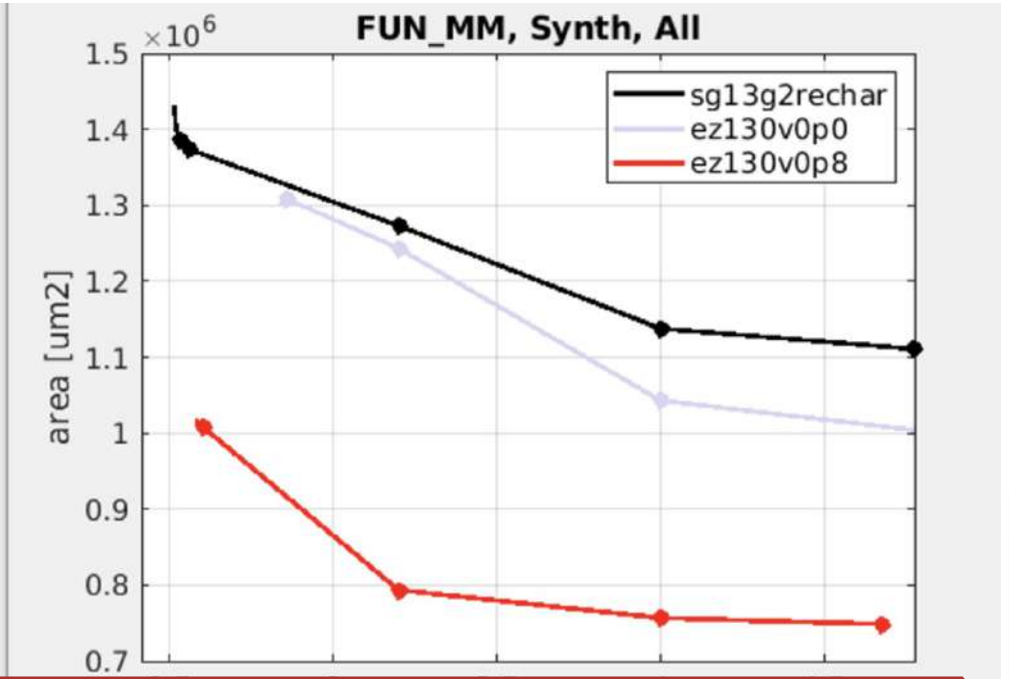
End-to-end Open-Source flow would help share IP

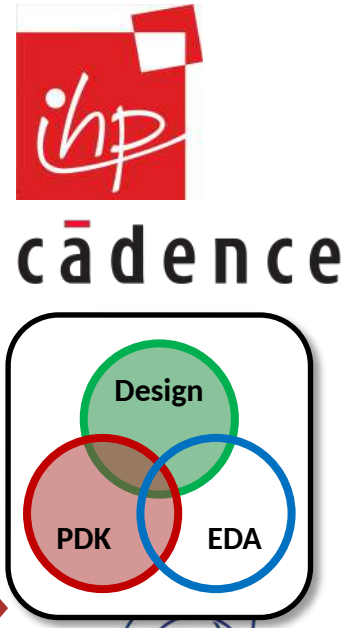


EZ Library: new standard cells for IHP130

- **VLSI 5 lecture by the Integrated Information Processing group at ETH Zürich**
  - By Oscar Castañeda Fernández, Christoph Studer and a bit of support from me
- **In one semester, 18 students re-designed a standard cell library for IHP130**







Needed additional negotiation with EDA tool vendor for release (granted)