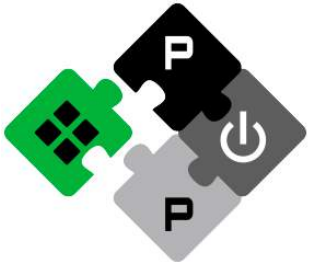


PULP PLATFORM

Open Source Hardware, the way it should be!

Moore's Law is In trouble... More Jobs in IC Design!

Luca Benini <luca.Benini@unibo.it, lbenini@iis.ee.ethz.ch>

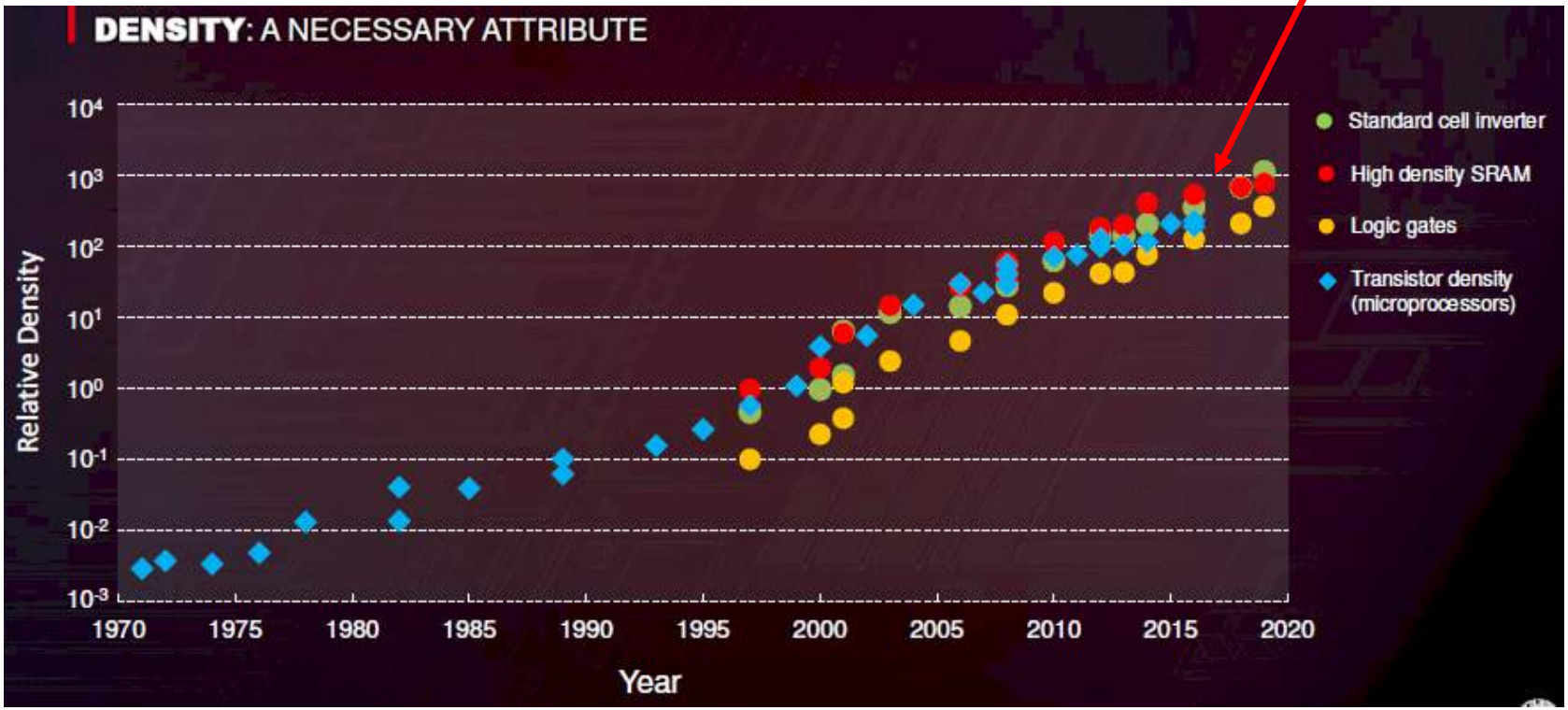
 http://pulp-platform.org  @pulp_platform

ETH zürich

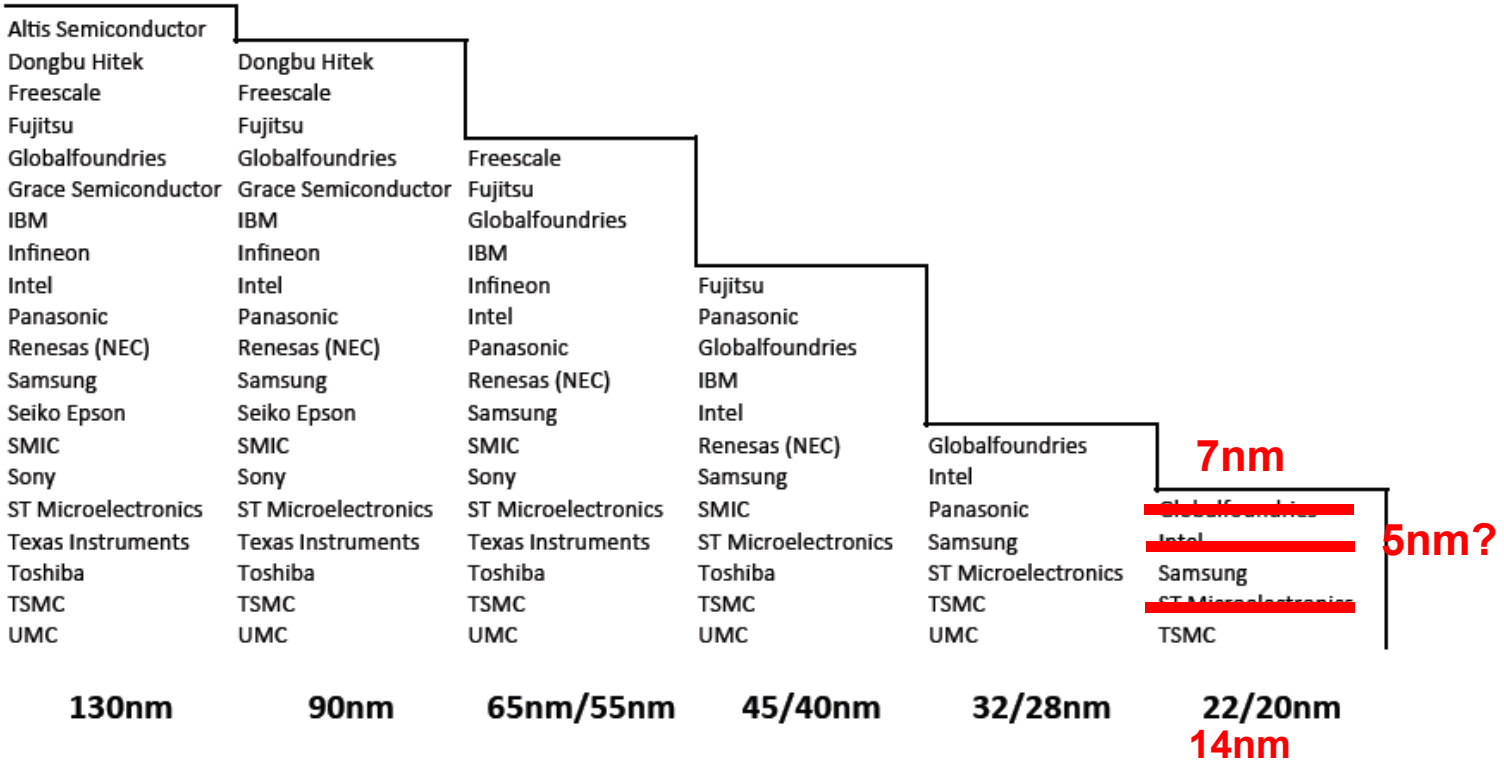
Moore's Law is well and alive?

Density scaling is **slowing down slightly**

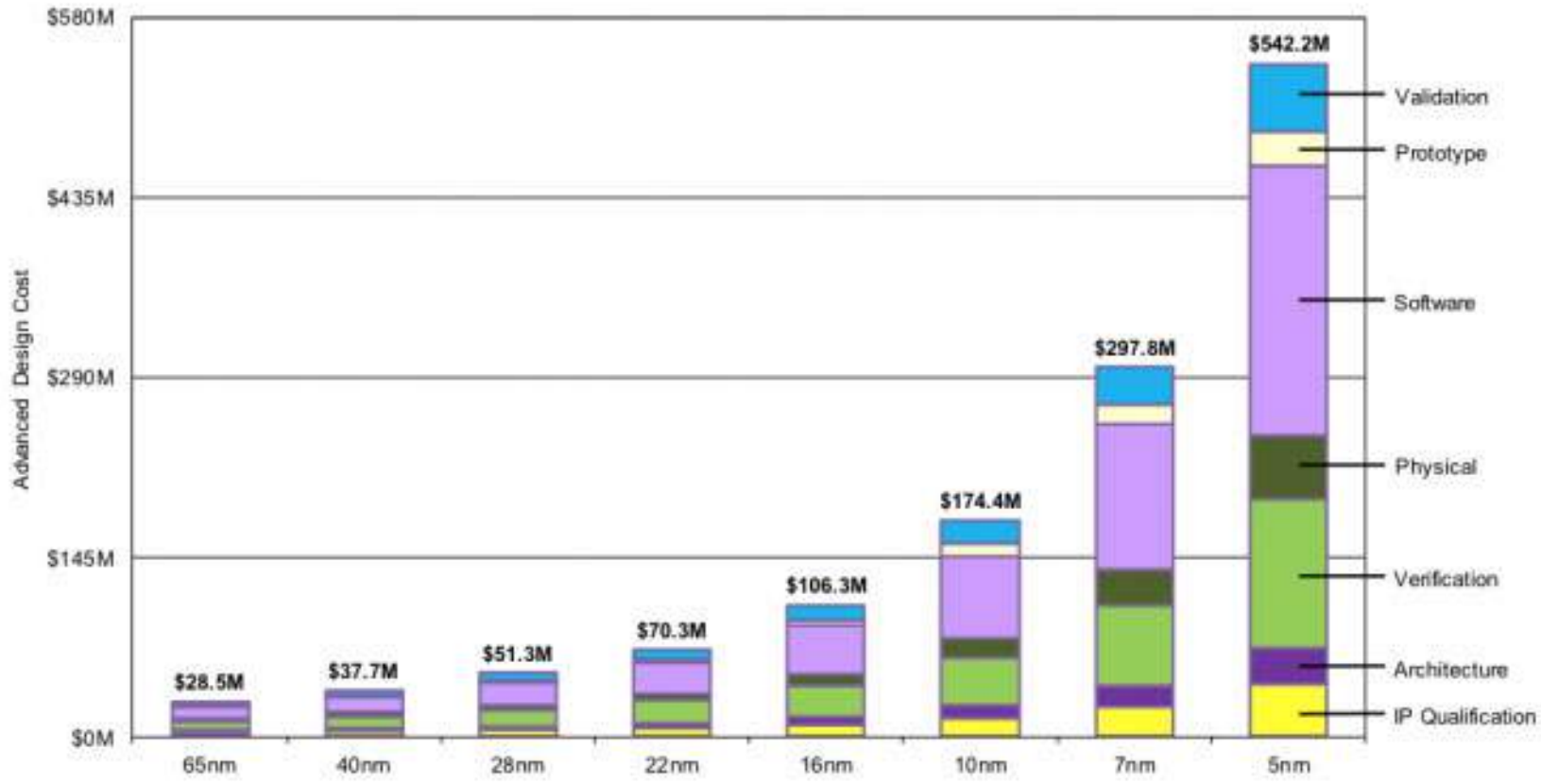
TSMC19



But it's a super-tough game!



And even if you do not build fabs…



Source: IBS

Prospects are dire…

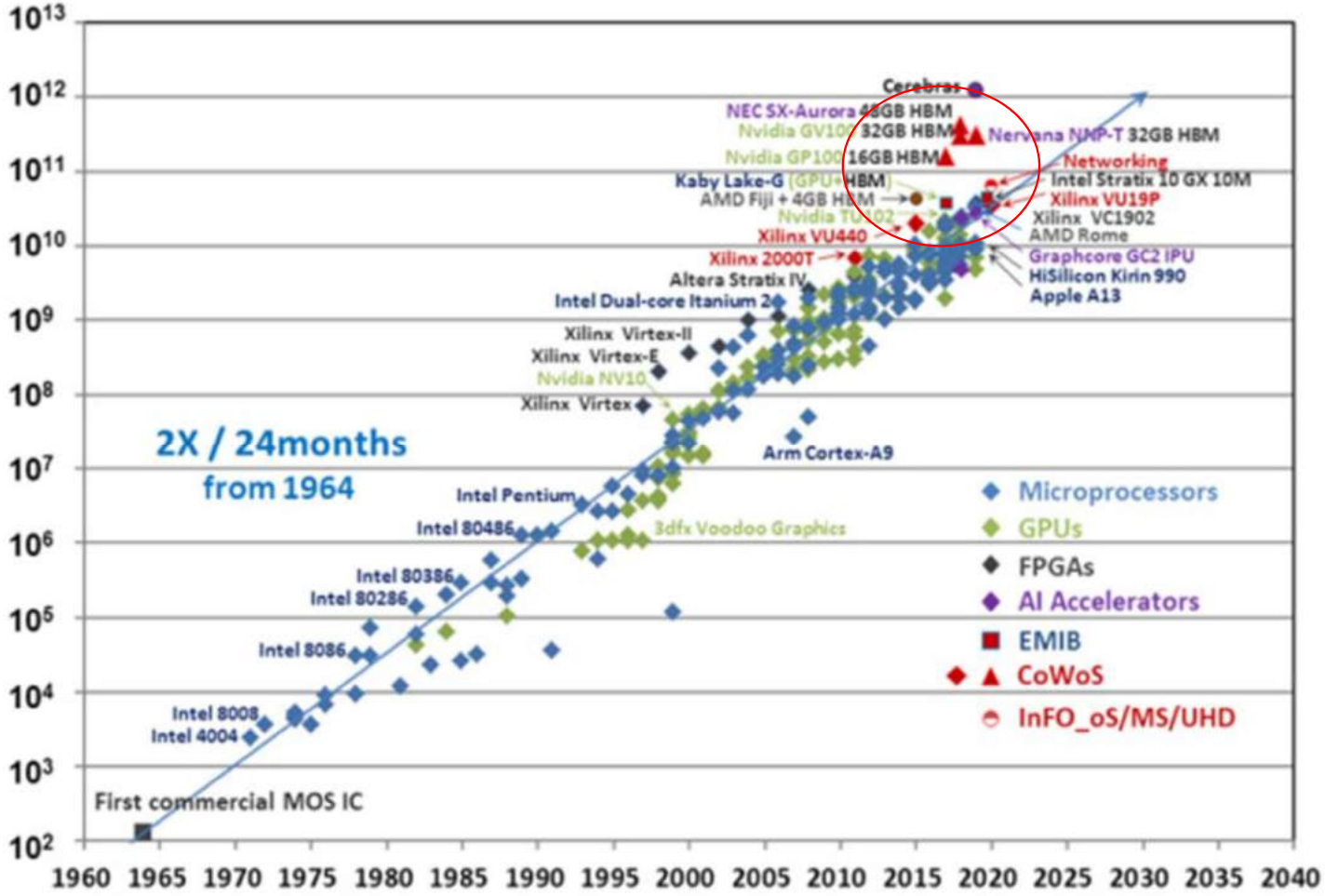
Technology is super-expensive to develop

Design cost is ballooning

IC jobs only in a few places in USA, Asia?

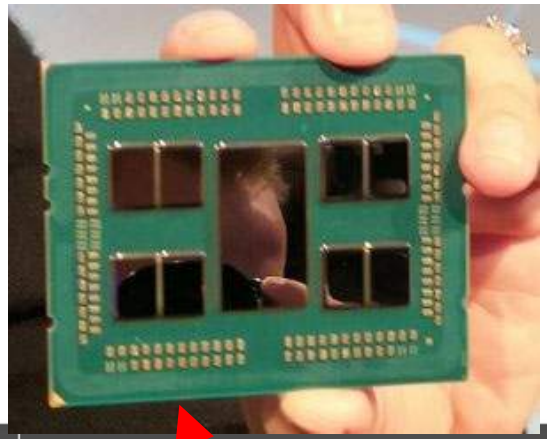
Think again!

Why? Another take on Moore's law

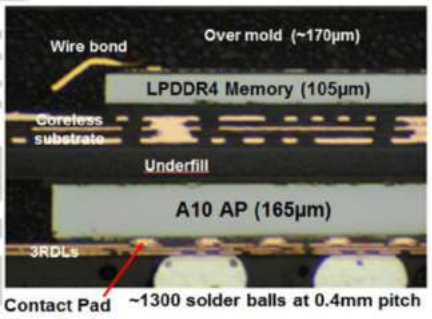


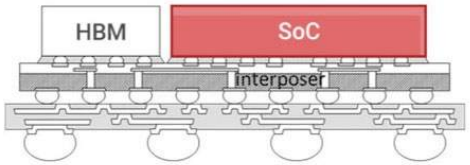
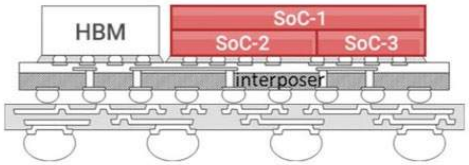
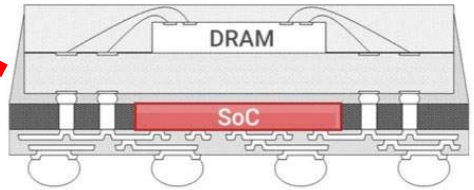
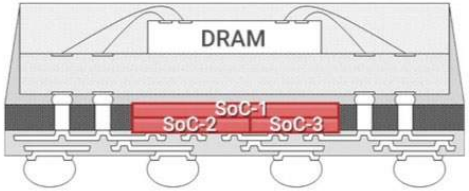
Chen et. Al. (TSMC) Ultra High Density SoIC with Sub-micron Bond Pitch, ECETC20

How? 3D IC

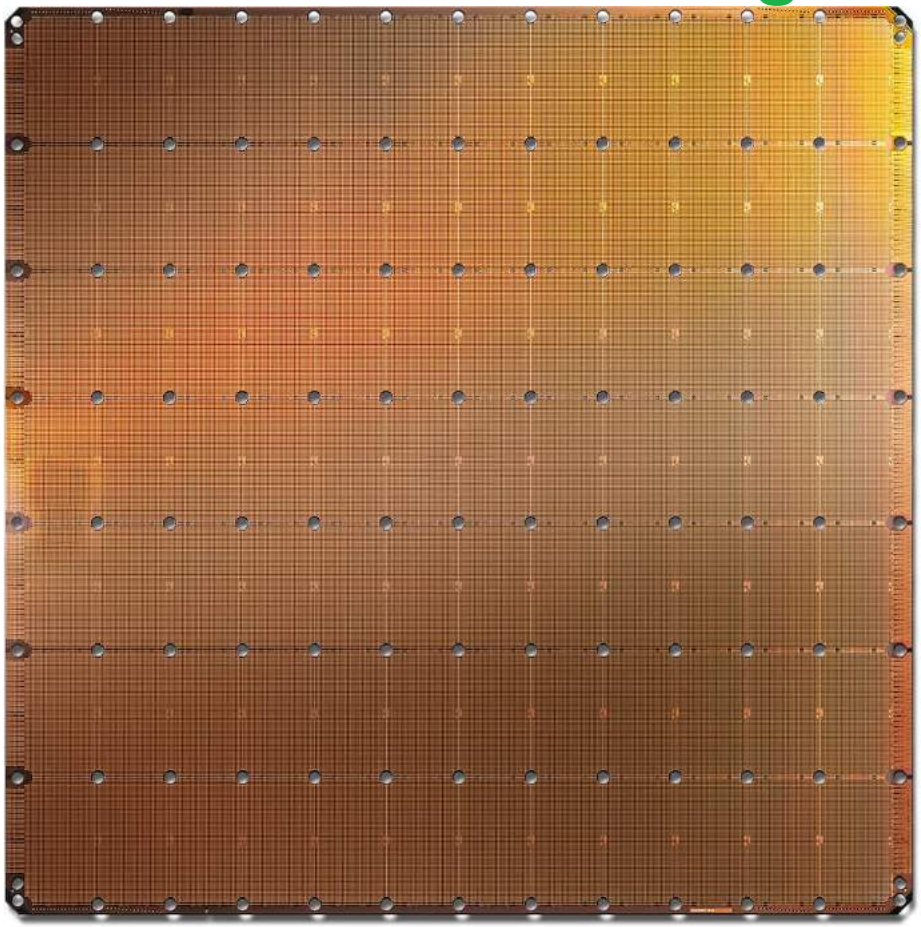


AMD



	SoC	TSMC-SoIC
CoWoS®		
InFO_PoP		

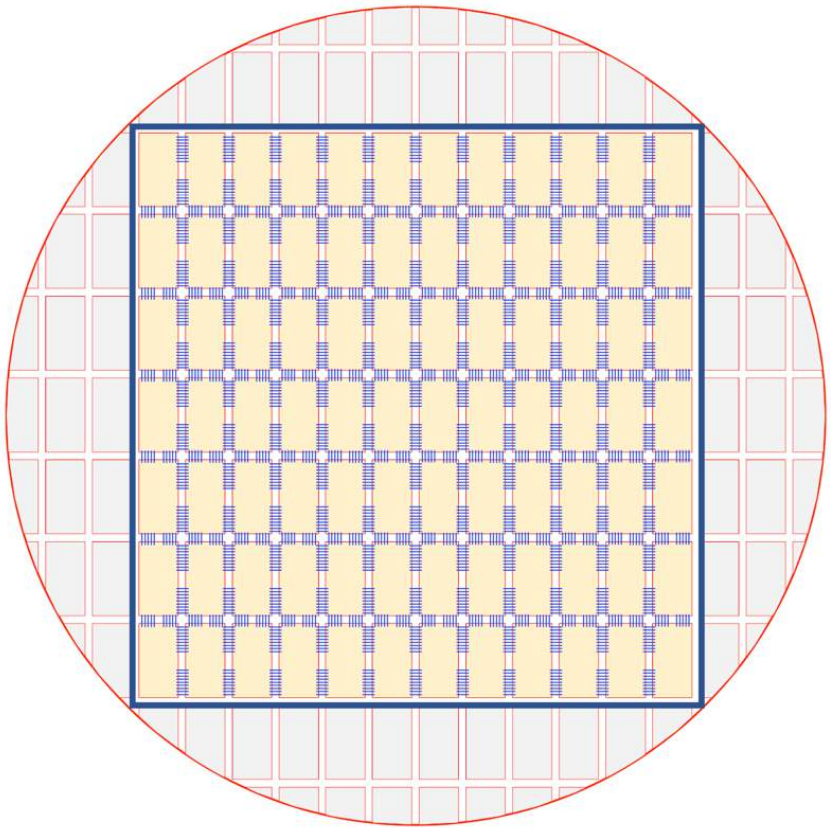
How? Wafer Scale Processing

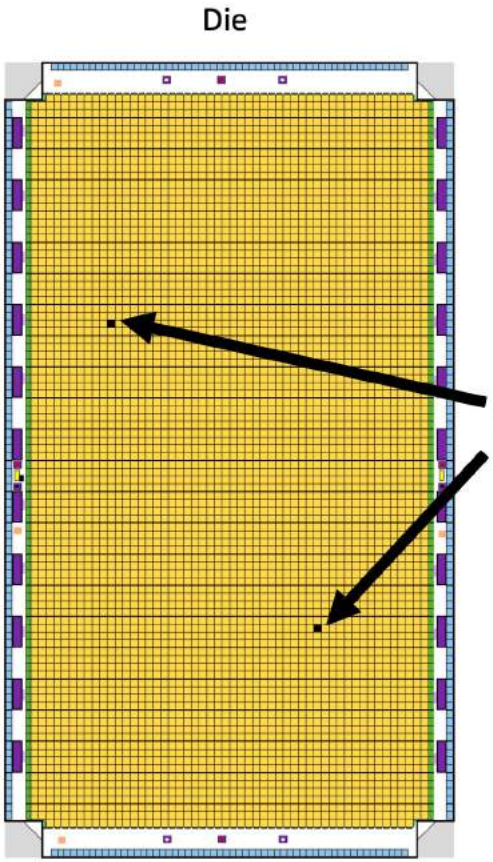


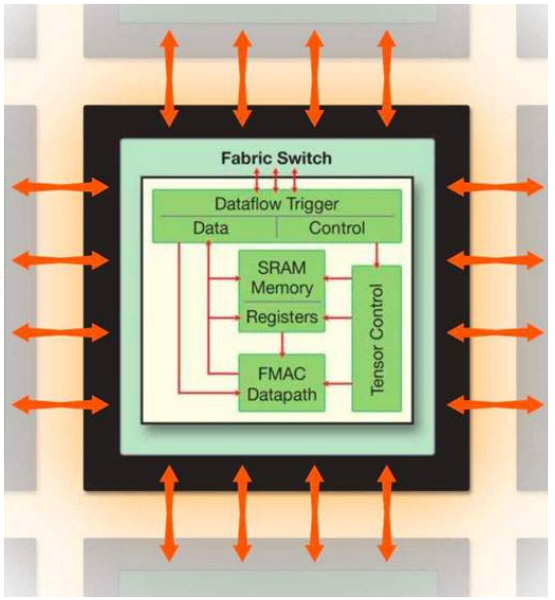
Cerebras WSE
46’225 mm2 silicon
1.2 Trillion Transistors

GPU
815 mm2 silicon
21.1 Billion Transistors

Cerebras: Vast array of flexible cores

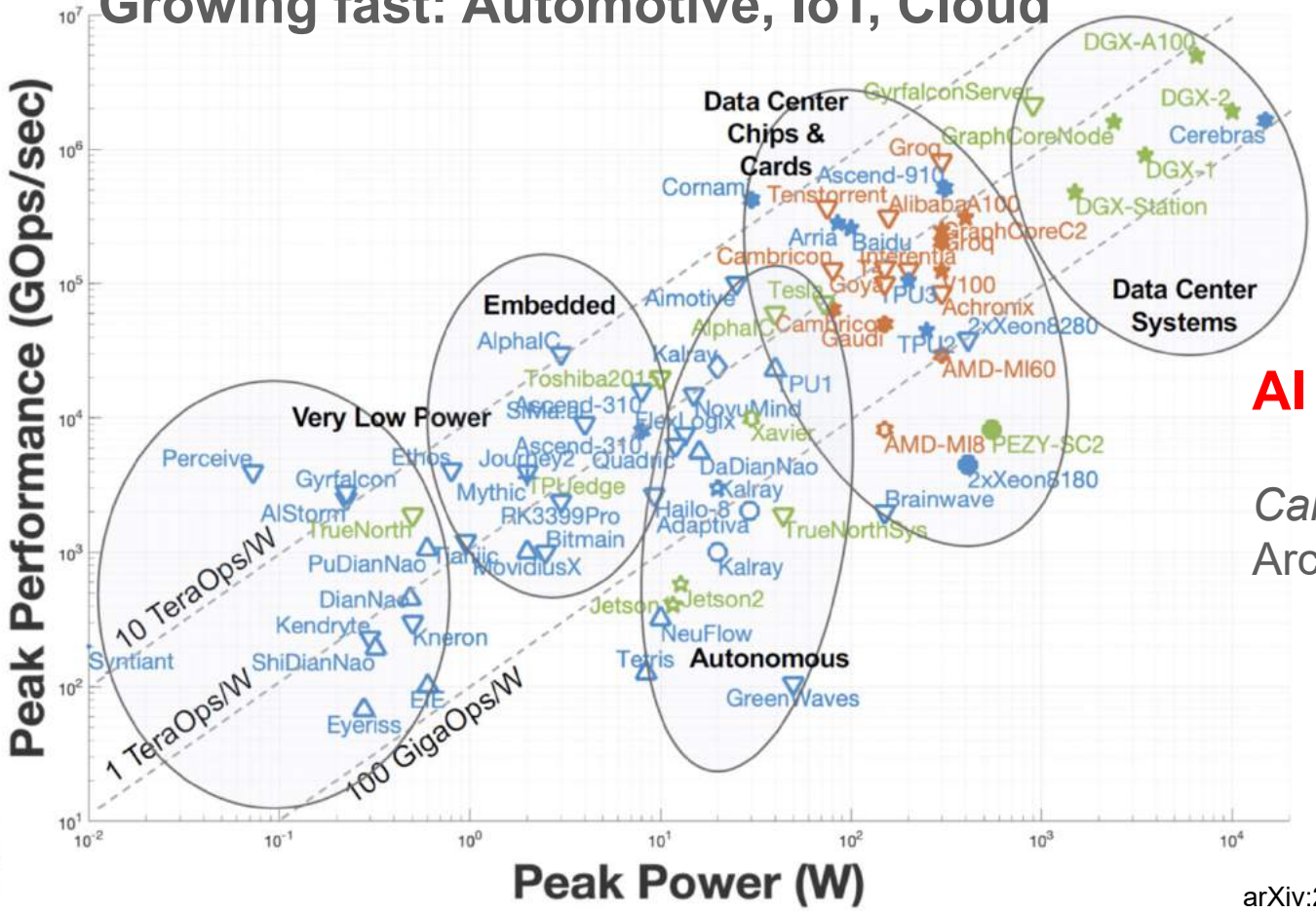






Why? More IC demand!

Growing fast: Automotive, IoT, Cloud



Semiconductor Shortage Could Cost Automakers $61B in Lost Sales

By Joel Hruska on February 1, 2021 at 8:16 am | 3 Comments

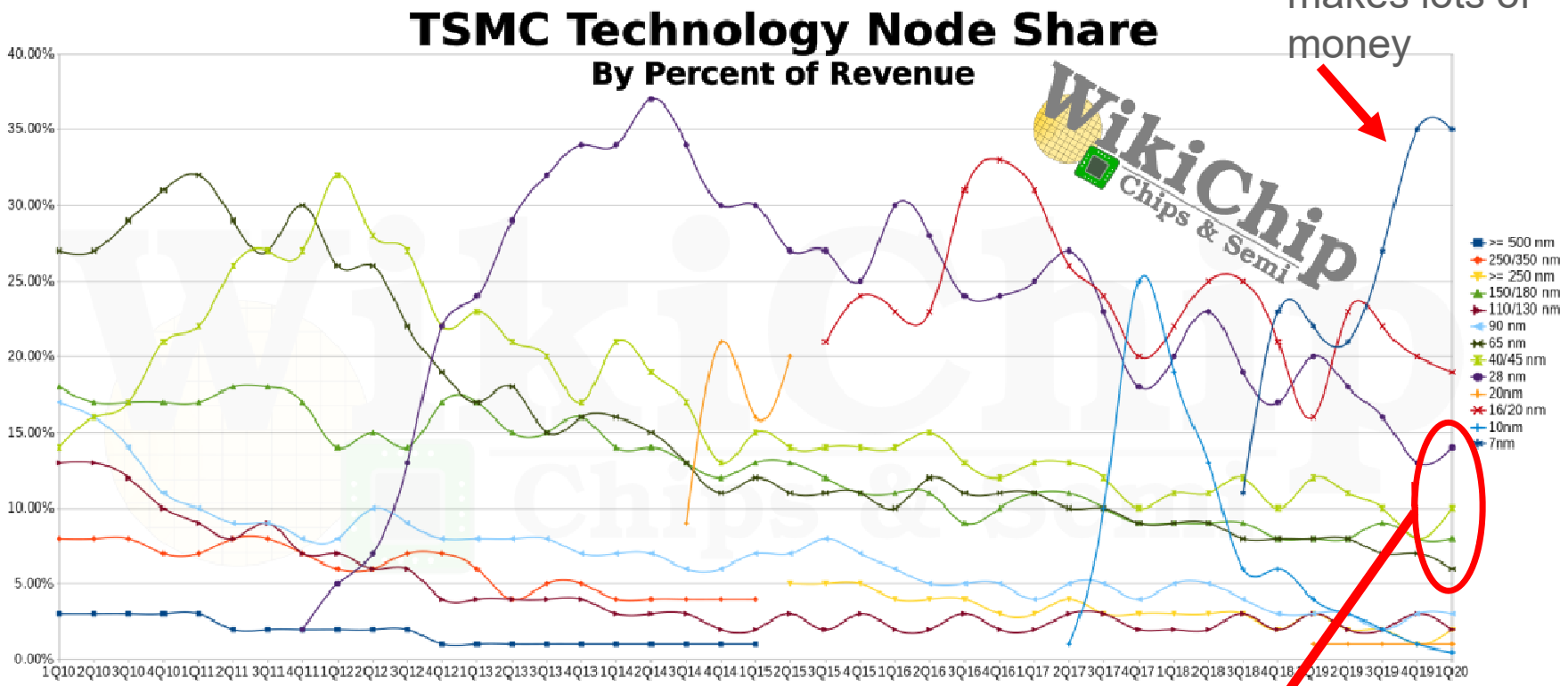
AI ICs everywhere

Cambrian explosion: lots of Archi+Circuit innovation

arXiv:2009.00993v1 [cs.DC] 2020

How? Not all (AI) ICs need 3nm tech

Most advanced FINFET node makes lots of money



Long-lived bulk CMOS nodes – very affordable!

How? Open Source Hardware

Hardware whose design is made publicly available so that anyone can study, modify, distribute, make, and sell the design or hardware based on that design

(*source: Open Source Hardware (OSHW) Statement of Principles 1.0*)

Very wide definition – includes PCBs and makers' stuff

I will focus on Open Souce Computing Hardware (OSCHW)

OSCHW Needs an Open Source ISA

RISC-V is a game changer

OS SW listed (not complete)

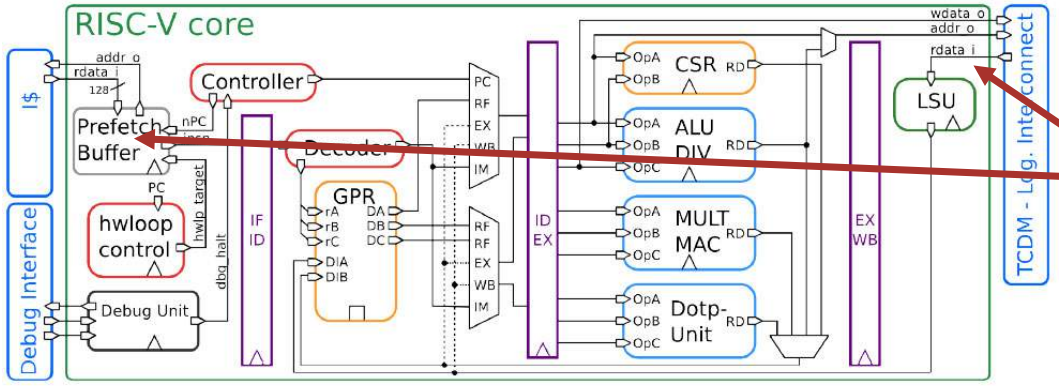
It's the Software, stupid!

- Toolchains → GCC, LLVM
- System tools → Emulators: QEMU, TinyEMU, Spike, Renode
  Bootloaders: Coreboot, U-boot, BBL, OpenSBI
  BINUTILS, GDB, OpenOCD, Glibc, Musl, Newlib
- Language Runtimes → C, C++, Fortran, GO, Rust, Java, Ocaml,
- Operating Systems → Linux: Fedora, OpenSUSE, Gentoo, OpenEmbedded/Yocto, Buildroot, OpenWRT, FreeBSD
  FreeRTOS, Zephyr, RTEMS, Xv6, HelenOS

https://github.com/riscv/riscv-software-list

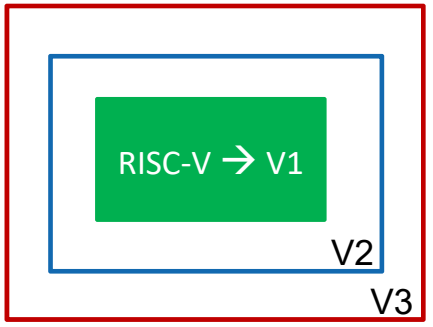
Open HW Core → ISA & Microarchitecture tuning

RI5CY – An Open MCU-class RISC-V Core for EE-AI
3-cycle ALU-OP, 4-cyle MEM-OP→IPC loss: LD-use, Branch



RISC-V
ISA is extensible *by construction*

I, D mem IF tuned for low latency & time borrowing



V1 Baseline RISC-V RV32IMC (not good for ML)

V2 HW loops. Post modified Load/Store, MAC

V3 SIMD 2/4 + DotProduct + Shuffling.Bit manipulation, Lightweight fixed point

XPULP extensions: 25 kGE → 40 kGE (1.6x) but 9x ML perf!

PULP: not only cores – many IPs for a Platform

RISC-V Cores

RI5CY	Ibex	Snitch	Ariane + Ara
32b	32b	32b	64b

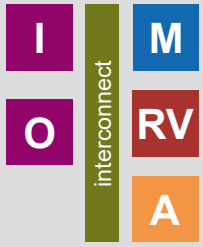
Peripherals

JTAG	SPI
UART	I2S
DMA	GPIO

Interconnect

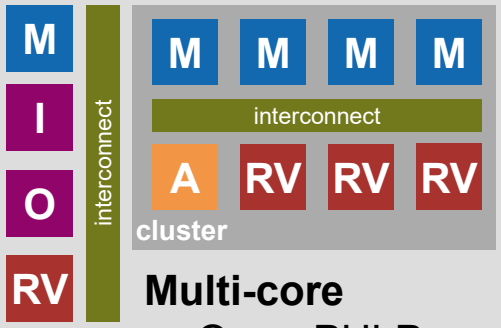
- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

Platforms



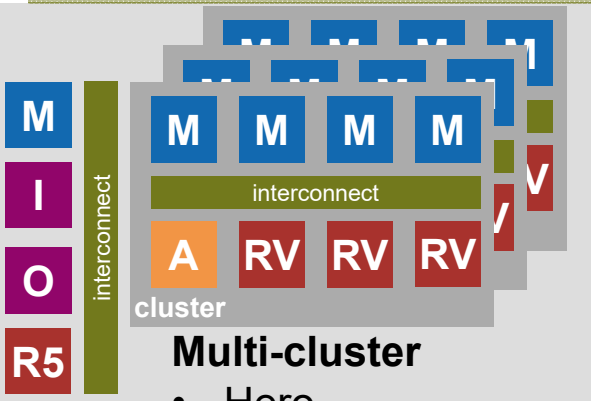
Single Core

- PULPino
- PULPissimo



Multi-core

- Open-PULP
- PULP-PM



Multi-cluster

- Hero
- Manticore

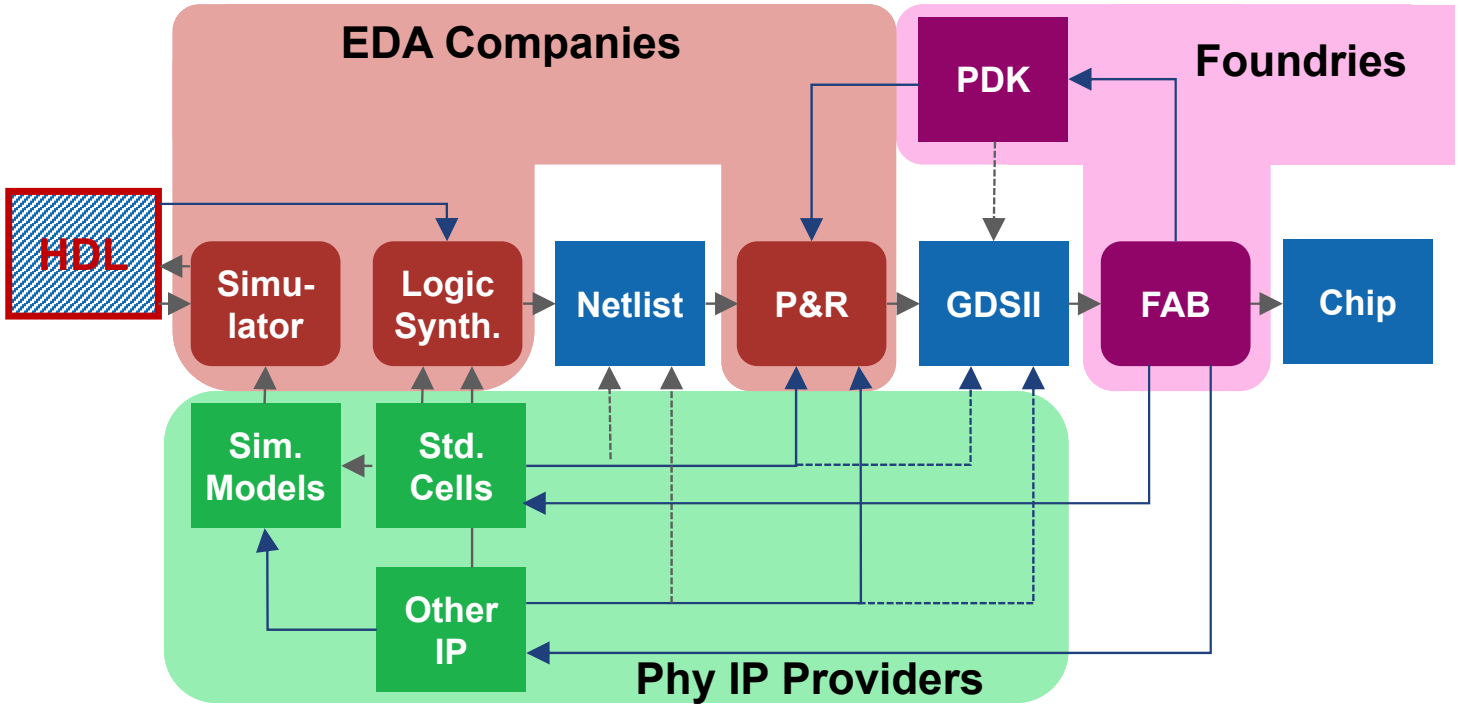
IOT → HPC

Accelerators

HWCE (convolution)	Neurostream (ML)	HWCrypt (crypto)	PULPO (1st ord. opt)

Nice, but what exactly is "open" in OSCHW?

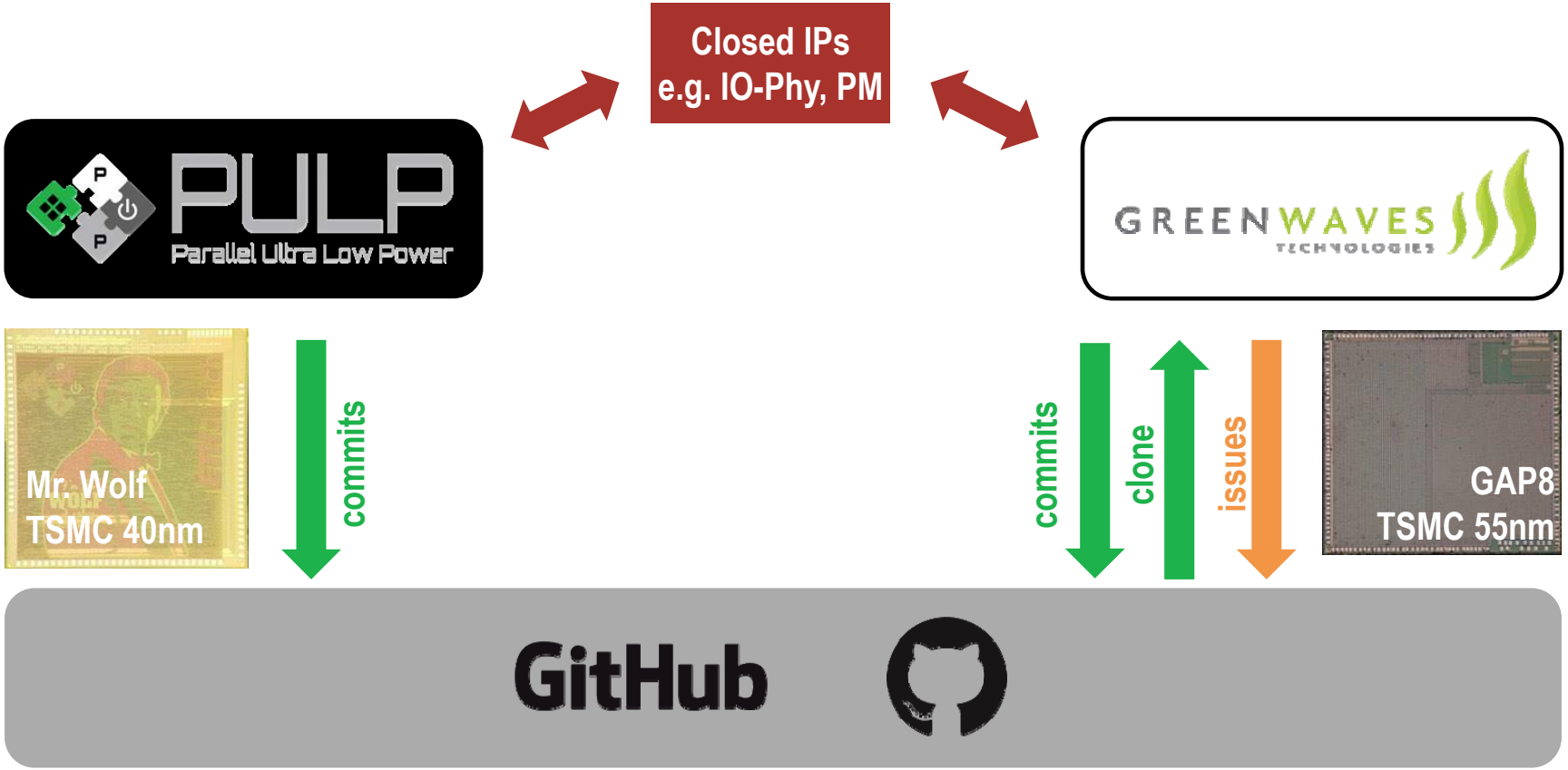
- Only the first stage of the silicon production pipeline
  → **RTL source code** (***permissive****, e.g. Apache is key for industrial adoption)
- Later stages contain closed IP of various actors → not open source by default



Cadence **license** for academic usage forbids ***permissive*** open sourcing of designs made with CDNS tools unless a ***reciprocal**** license is used

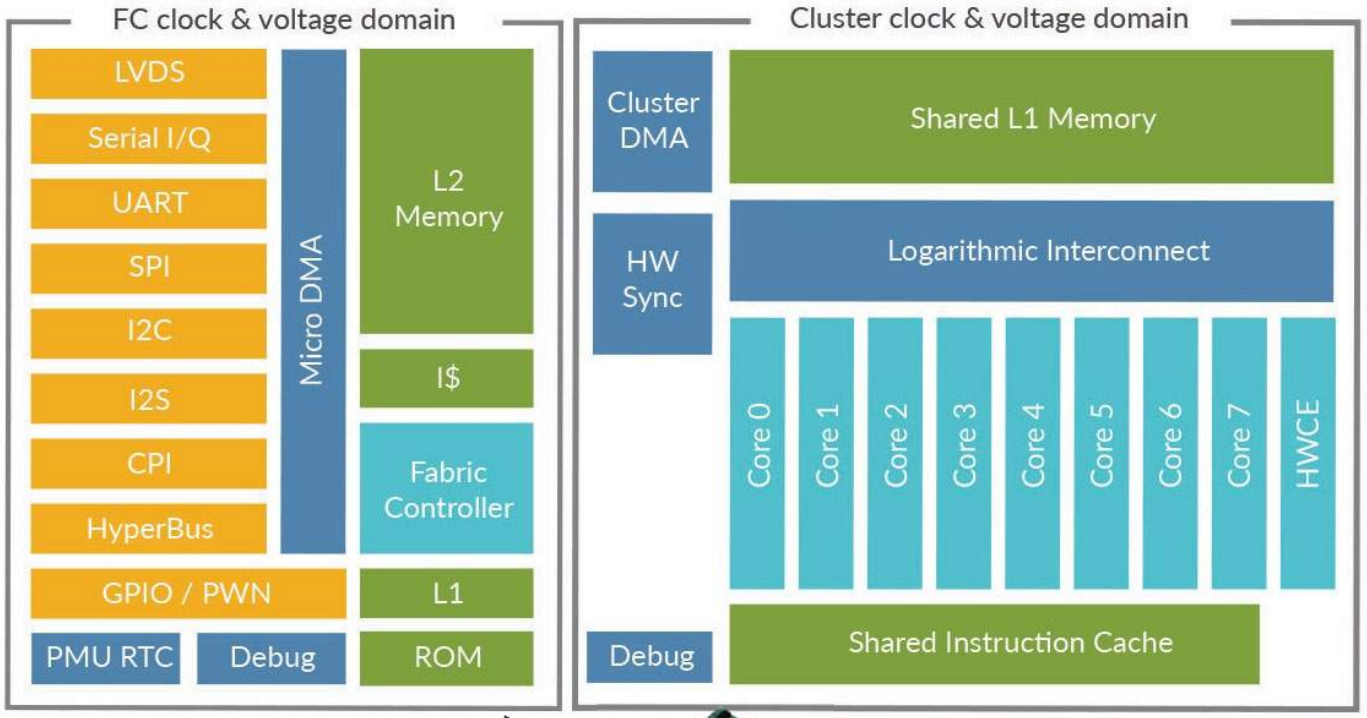
"See: https://cern-ohl.web.cern.ch/ (CERN-OHL-S, -W, -P)

Open source collaboration scheme explained



Successful product development: GWT's GAP8

TSMC 55mn, Two independent clock and voltage domains, from 0-133MHz/1V up to 0-250MHz/1.2V

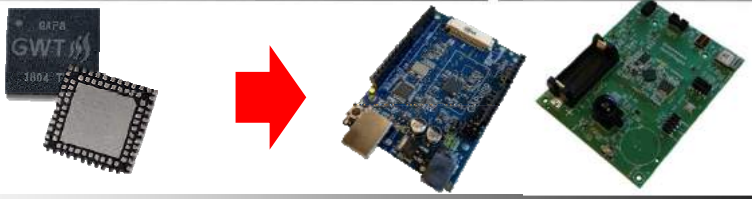


MCU

- Extended RISC-V core
- Extensive I/O set
- Micro DMA
- Embedded DC/DC converters

Computation engine

- 8 extended RISC-V cores
- Fully programmable
- Efficient parallelization
- Shared instruction cache
- HW synchronization
- HW convolution Engine (3 * 3x3)



20pJ/OP @32bit 3.5GOPS

Academic open source → Industrial open source

OPENHW GROUP — PROVEN PROCESSOR IP

Rick O'Connor (OpenHW CEO, former RISC-V foundation director)

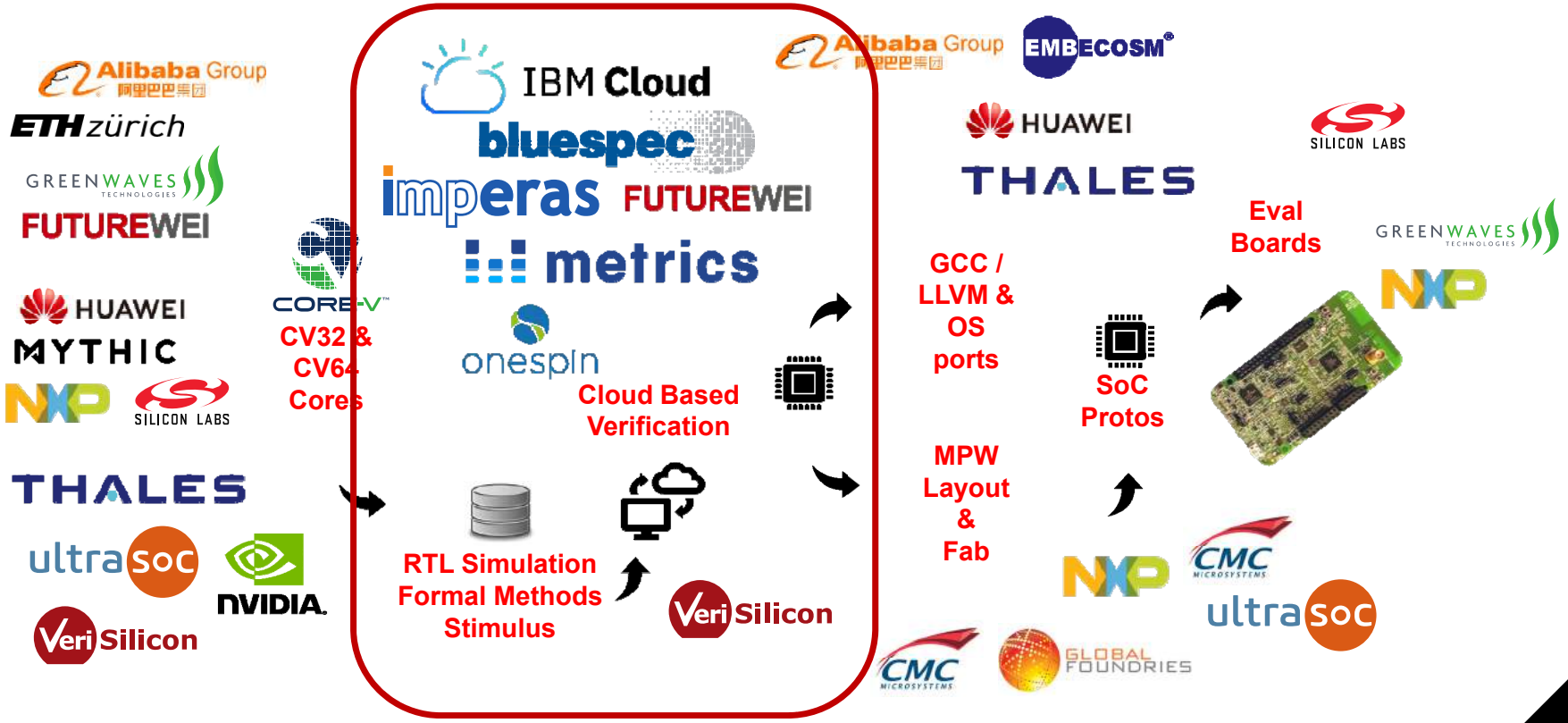
- **OpenHW Group** is a not-for-profit, global organization (EU,NA,Asia) where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the **Core-V** family
- **OpenHW Group** provides an infrastructure for hosting high quality open-source HW developments in line with industry best practices.

PULP — Parallel Ultra Low Power

RI5CY, ARIANE

CORE-V™

OpenHW Group Ecosystem



Verification is Key!

What about End-to-End Open HW (pdk, tools)?

Open Source Shuttle Program

Google + efabless.com

START HERE

Open source process design kit for usage with SkyWater Foundry 130nm tech.
https://github.com/google/skywater-pdk

ASIC EDA flows
http://opencircuitdesign.com/qflow/

FOSS 130nm Production PDK

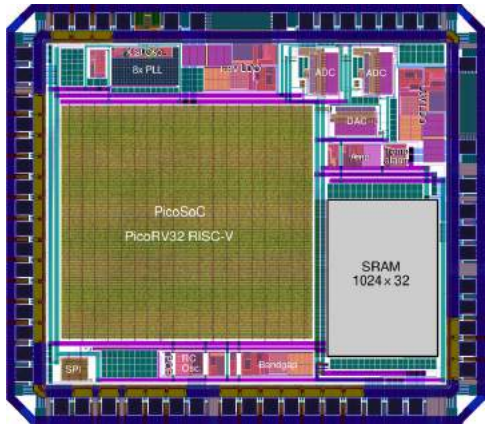
We are excited to collaborate with Google to create engagement and accelerate design on the FOSS 130nm Production PDK.

Efabless will make designs for this PDK simple and affordable by integrating resources on our cloud-based design platform, including:

- An open-source-based end-to-end ASIC design flow, including OpenRoad, Electric, Magic, and others
- The open-source striVe family of full ASIC reference designs
- A marketplace for monetizing your IP or designs

Additionally - Efabless is managing an **Open Source Shuttle Program** sponsored by Google.

The first shuttle is targeted for November 2020 and will provide 40 project slots, free of charge to any fully open-source design.



Raven 130nm mixed-signal SoC

Closing thoughts… IC design is a hot job!

Moore's law is not ending, it's just changing!

IC demand is stronger than ever

AI is igniting architecture + circuit innovation

Bleeding edge tech is not always the best choice

Open HW can help to lower design cost

PULP

Parallel Ultra Low Power

Luca Benini, Davide Rossi, Andrea Borghesi, Michele Magno, Simone Benatti, Francesco Conti, Francesco Beneventi, Daniele Palossi, Giuseppe Tagliavini, Antonio Pullini, Germain Haugou, Lukas Cavigelli, Manuele Rusci, Florian Glaser, Renzo Andri, Fabio Montagna, Bjoern Forsberg, Pasquale Davide Schiavone, Alfio Di Mauro, Victor Javier Kartsch Morinigo, Tommaso Polonelli, Fabian Schuiki, Stefan Mach, Andreas Kurth, Florian Zaruba, Manuel Eggimann, Philipp Mayer, Marco Guermandi, Xiaying Wang, Michael Hersche, Robert Balas, Antonio Mastrandrea, Matheus Cavalcante, Angelo Garofalo, Alessio Burrello, Gianna Paulin, Georg Rutishauser, Andrea Cossettini, Luca Bertaccini, Maxim Mattheeuws, Samuel Riedel, Sergei Vostrikov, Vlad Niculescu, Frank K. Gurkaynak,
and many more that we forgot to mention

http://pulp-platform.org @pulp_platform