Moore's Law is In trouble... More Jobs in IC Design!

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Moore’s Law is well and alive?

Density scaling is slowing down slightly
But it’s a super-tough game!
And even if you do not build fabs…

Source: IBS
Prospects are dire…

Technology is super-expensive to develop
Design cost is ballooning

IC jobs only in a few places in USA, Asia?

Think again!
Why? Another take on Moore’s law
How? 3D IC
How? Wafer Scale Processing

Cerebras
WSE
46'225 mm² silicon
1.2 Trillion
Transistors

GPU
815 mm² silicon
21.1 Billion
Transistors
Cerebras: Vast array of flexible cores
Why? More IC demand!
Growing fast: Automotive, IoT, Cloud

AI ICs everywhere
Cambrian explosion: lots of Archi+Circuit innovation
How? Not all (AI) ICs need 3nm tech

Long-lived bulk CMOS nodes – very affordable!

Most advanced FINFET node makes lots of money
How? Open Source Hardware

Hardware whose design is made publicly available so that anyone can study, modify, distribute, make, and sell the design or hardware based on that design

(source: Open Source Hardware (OSHW) Statement of Principles 1.0)

Very wide definition – includes PCBs and makers’ stuff

I will focus on Open Source Computing Hardware (OSCHW)
OSCHW Needs an Open Source ISA

A modern, open, free ISA, extensible by construction
Endorsed and Supported by 600+ Members
But... an open ISA is not Open HW (it's a prerequisite!)

Risc-V international moved to Zürich, CH
for international neutrality, 1/3 of members from EU
RISC-V is a game changer

It’s the Software, stupid!

- Toolchains: GCC, LLVM
- System tools: Emulators: QEMU, TinyEMU, Spike, Renode
- Bootloaders: Coreboot, U-boot, BBL, OpenSBI
  BINUTILS, GDB, OpenOCD, Glibc, Musl, Newlib
- Language Runtimes: C, C++, Fortran, GO, Rust, Java, Ocaml,
- Operating Systems: Linux: Fedora, OpenSUSE, Gentoo,
  OpenEmbedded/Yocto, Buildroot, OpenWRT, FreeBSD
  FreeRTOS, Zephyr, RTEMS, Xv6, HelenOS

https://github.com/riscv/riscv-software-list

OS SW listed (not complete)
Open HW Core → ISA & Microarchitecture tuning

RI5CY – An Open MCU-class RISC-V Core for EE-AI
3-cycle ALU-OP, 4-cyle MEM-OP → IPC loss: LD-use, Branch

ISA is extensible by construction

I, D mem IF tuned for low latency & time borrowing

V1  Baseline RISC-V RV32IMC (not good for ML)
V2  HW loops. Post modified Load/Store, MAC
V3  SIMD 2/4 + DotProduct + Shuffling. Bit manipulation, Lightweight fixed point

XPULP extensions: 25 kGE → 40 kGE (1.6x) but 9x ML perf!
PULP: not only cores – many IPs for a Platform

RISC-V Cores
- RI5CY 32b
- Ibex 32b
- Snitch 32b
- Ariane + Ara 64b

Platforms
- Single Core
  - PULPino
  - PULPiSSimIO

Multi-core
- Open-PULP
- PULP-PM

Interconnect
- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

Accelerators
- HWCE (convolution)
- Neurostream (ML)
- HWCrypt (crypto)
- PULPO (1st ord. opt)
Nice, but what exactly is “open” in OSCHW?

- Only the first stage of the silicon production pipeline → **RTL source code** (*permissive*, e.g. Apache is key for industrial adoption)
- Later stages contain closed IP of various actors → not open source by default

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Open source collaboration scheme explained

Closed IPs
e.g. IO-Phy, PM

Mr. Wolf
TSMC 40nm

PULP
Parallel Ultra Low Power

ETH Zürich

GitHub

GAP8
TSMC 55nm

Industrial Users

commits

clone

issues

Commit

Closed IPs

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GAP8
TSMC 55nm

Mr. Wolf
TSMC 40nm
Successful product development: **GWT’s GAP8**

TSMC 55nm, Two independent clock and voltage domains, from 0-133MHz/1V up to 0-250MHz/1.2V

- **MCU**
  - Extended RISC-V core
  - Extensive I/O set
  - Micro DMA
  - Embedded DC/DC converters

- **Computation engine**
  - 8 extended RISC-V cores
  - Fully programmable
  - Efficient parallelization
  - Shared instruction cache
  - HW synchronization
  - HW convolution Engine (3 * 3x3)

- **20pJ/OP @32bit 3.5GOPS**
Academic open source → Industrial open source

- **OpenHW Group** is a not-for-profit, global organization (EU, NA, Asia) where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the **Core-V family**.
- **OpenHW Group** provides an infrastructure for hosting high quality open-source HW developments in line with industry best practices.
OpenHW Group Ecosystem

Verification is Key!
What about End-to-End Open HW (pdk, tools)?

Open Source Shuttle Program

Google + efabless

Open source process design kit for usage with SkyWater Foundry 130nm tech. https://github.com/google/skywater-pdk

ASIC EDA flows http://opencircuitdesign.com/qflow/

FOSS 130nm Production PDK

We are excited to collaborate with Google to create engagement and accelerate design on the FOSS 130nm Production PDK.

Efabless will make designs for this PDK simple and affordable by integrating resources on our cloud-based design platform, including:

- An open-source-based end-to-end ASIC design flow, including OpenRoad, Electric, Magic, and others
- The open-source striVe family of full ASIC reference designs
- A marketplace for monetizing your IP or designs

Additionally - Efabless is managing an Open Source Shuttle Program sponsored by Google.

The first shuttle is targeted for November 2020 and will provide 40 project slots, free of charge to any fully open-source design.
Closing thoughts… IC design is a hot job!

- Moore’s law is not ending, it’s just changing!
- IC demand is stronger than ever
- AI is igniting architecture + circuit innovation
- Bleeding edge tech is not always the best choice
- Open HW can help to lower design cost
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