



DATE²¹

DESIGN, AUTOMATION & TEST IN EUROPE

01 – 05 February 2021 · virtual conference

The European Event for Electronic
System Design & Test

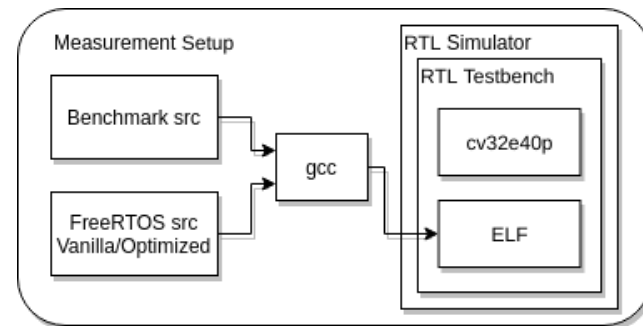
ETH zürich

RISC-V for Real-time MCUs – Software Optimization and Microarchitectural Gap Analysis

Robert Balas, Luca Benini

Summary

- **Analyze Real-time on RISC-V**
 - CV32E40P, an open-source industrially supported RV32IMFC core, 4-stage in order
 - FreeRTOS, a popular open-source RTOS
- 1. **Software Optimizations for FreeRTOS**
- 2. **Measure Interrupt Latency and Context Switch Time**
- 3. **Quantify gap to ARM Cortex-M3**
 - Difference due to automatic Register Stacking and Nested Interrupts
 - Come up with extensions



Optimized FreeRTOS	Context Switch Time (WCET)	Interrupt Latency (WCET)
vs Vanilla RISC-V FreeRTOS	+33%	+20%
vs ARM Cortex-M3 FreeRTOS	-26%	-50%