**Goal:** Characterize hardware gap with respect to ARM Cortex Series

**Setup**
- Baseline Characterization using the cv32e40p and vanilla FreeRTOS

**Software Optimizations FreeRTOS**
- Use features of hardware and compiler options

**Simulation and measurements**
- Cycle accurate
- On synthetic and real-life (power control unit) benchmark
- Measure context switch time and interrupt latency

**Description**

**Background & Motivation**
- Increasing RISC-V adoption in IoT/embedded Systems (MCU)
- Dealing with Real-time constraints
- Analyze RISC-V real-time support

**New Insights**
- Identified and quantified hardware gaps in the RISC-V Ecosystem with respect to real-time
- RISC-V solutions lag behind ARM Cortex Series

**Quantitative Impact**
- After optimizations, most difference attributable to hardware

<table>
<thead>
<tr>
<th>Optimized FreeRTOS</th>
<th>Context Switch Time Improvement (WCET)</th>
<th>Int. Latency Improvement (WCET)</th>
</tr>
</thead>
<tbody>
<tr>
<td>vs Vanilla FreeRTOS</td>
<td>+33%</td>
<td>+20%</td>
</tr>
<tr>
<td>vs ARM Cortex-M3 FreeRTOS</td>
<td>-26%</td>
<td>-50%</td>
</tr>
</tbody>
</table>

**Summary and Conclusion**
- ARM nested interrupts lower interrupt latency
- ARM automatic register stacking lower context switch time and interrupt latency
- Potential for new RISC-V extensions