



DESIGN, AUTOMATION
AND TEST IN EUROPE

THE EUROPEAN EVENT FOR
ELECTRONIC SYSTEM DESIGN & TEST

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LYON, FRANCE

CENTRE DE CONGRÈS DE LYON



TCDM Burst Access: Breaking the Bandwidth Barrier in Shared-L1 RVV Clusters Beyond 1000 FPUs

Diyoun Shen^{1*}, Yichao Zhang^{1*}, Marco Bertuletti*, Luca Benini^{*§}

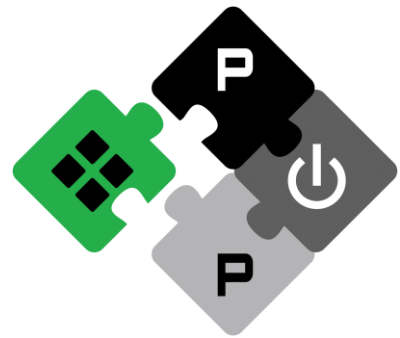
**ETH Zurich, Switzerland*

§University of Bologna, Italy

¹ These two authors contribute equally to the paper

ETH zürich

CORENEXT



Many-Core Cluster is Rocking

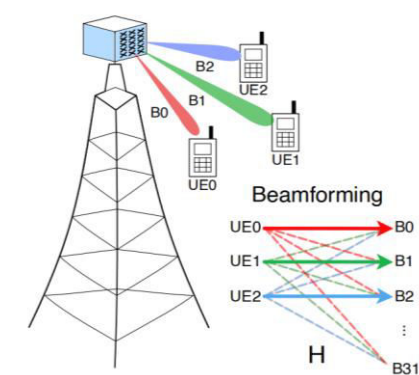
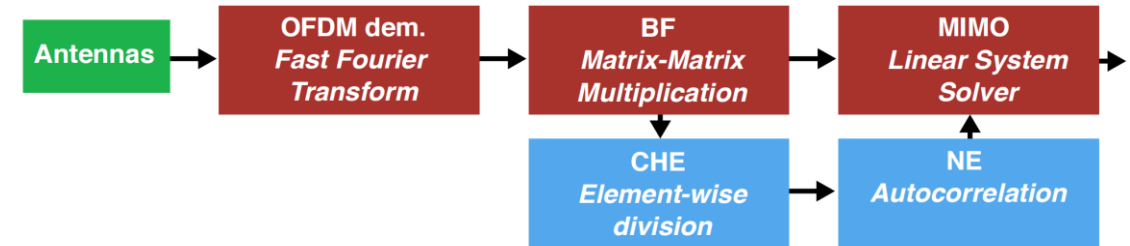
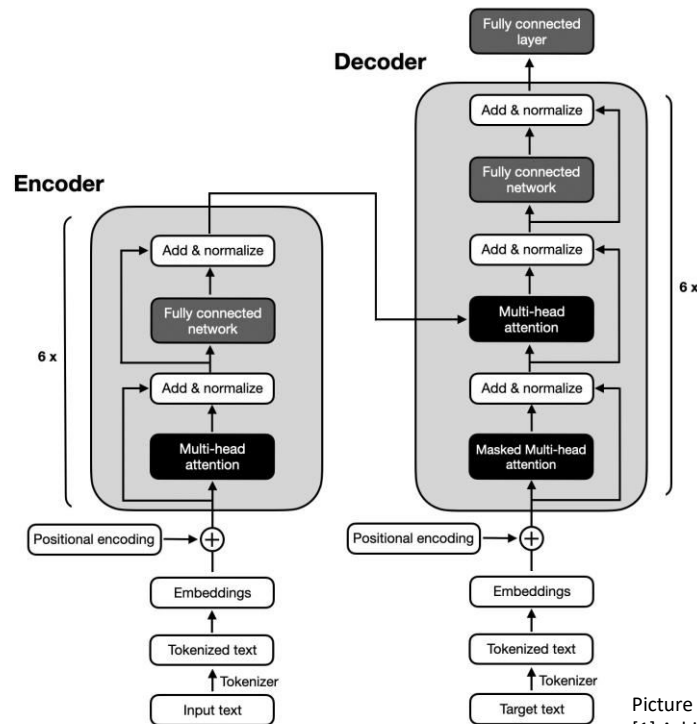
- **Emerging fields need more computation**

- Attention-Based AI Models
- B5G Communication



More Cores

More Data Movements



Picture Sources:

- [1] Ashish Vaswani, Noam Shazeer, Niki Parmar, Jakob Uszkoreit, Llion Jones, Aidan N. Gomez, Lukasz Kaiser, & Illia Polosukhin. (2023). Attention Is All You Need.
- [2] Marco Bertuletti, Yichao Zhang, Alessandro Vanelli-Coralli, & Luca Benini. (2022). Efficient Parallelization of 5G-PUSCH on a Scalable RISC-V Many-core Processor.

Diyou Shen / ETH Zurich

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More Cores
More Data Movements

- **How to keep efficient?**

- Reduce number of instructions
- Reduce data duplication & memory transfers



SIMD/SIMT
Shared L1 Cluster

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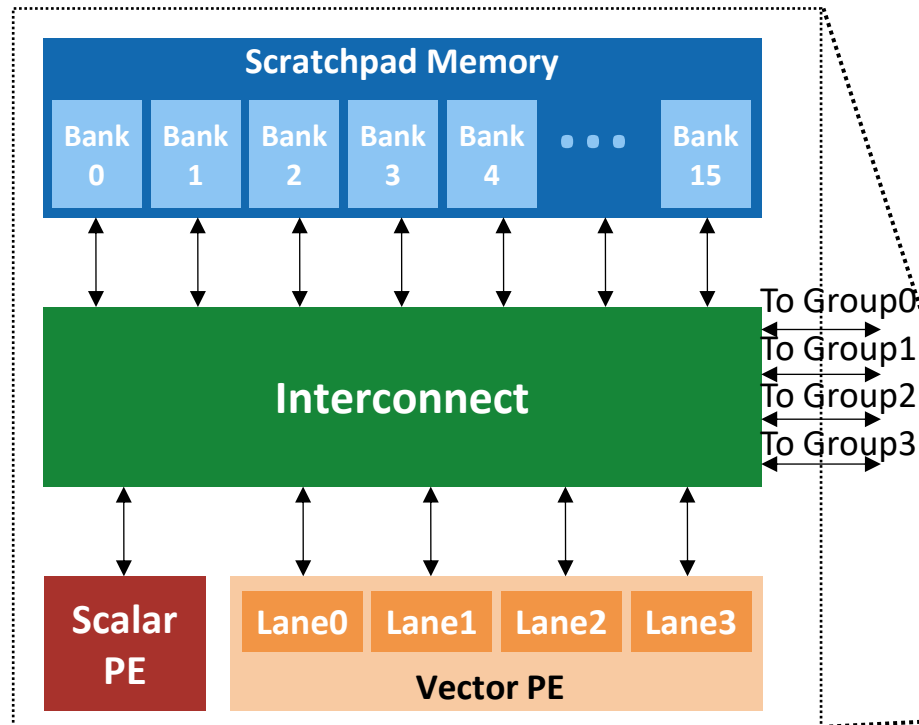
SIMD/SIMT

Shared L1 Cluster

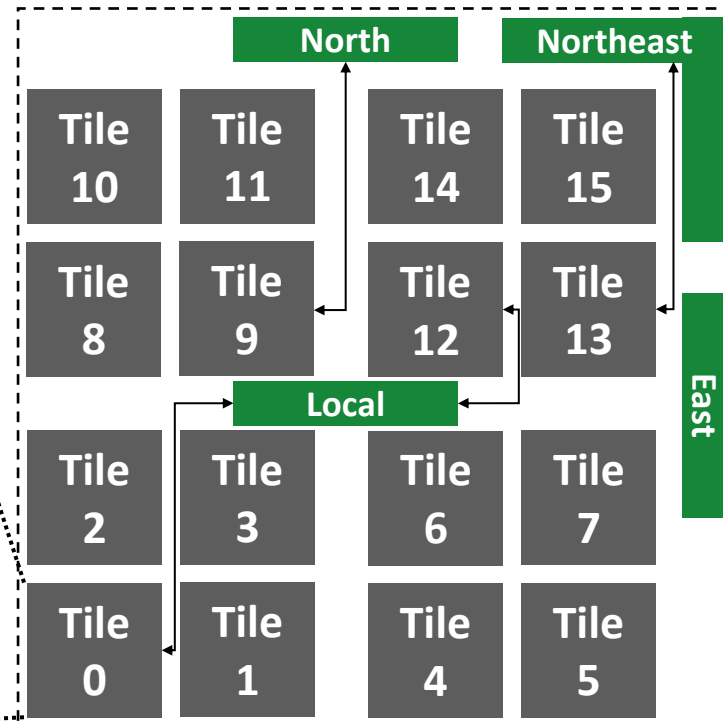
Many-Core Vector Shared-L1 Cluster

Hierarchical design is needed to route over **hundreds** cores

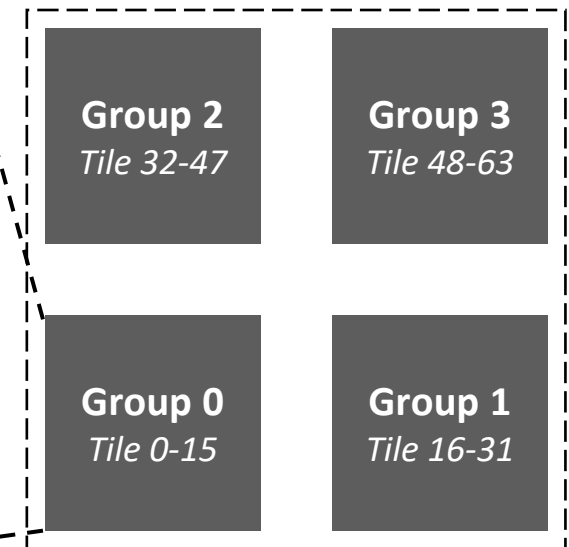
Building Block: Tile



Next Hierarchy

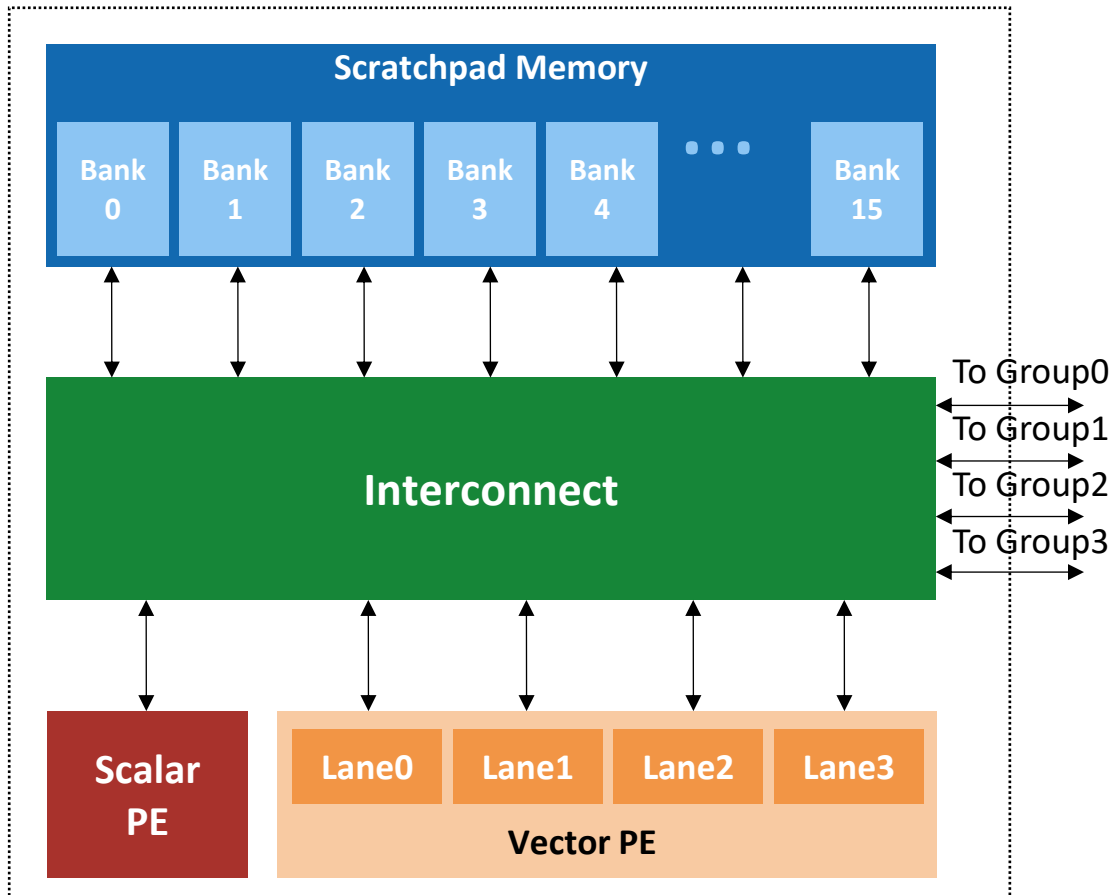


Top Hier: Cluster



And what, Gul'Dan, must we give it return?

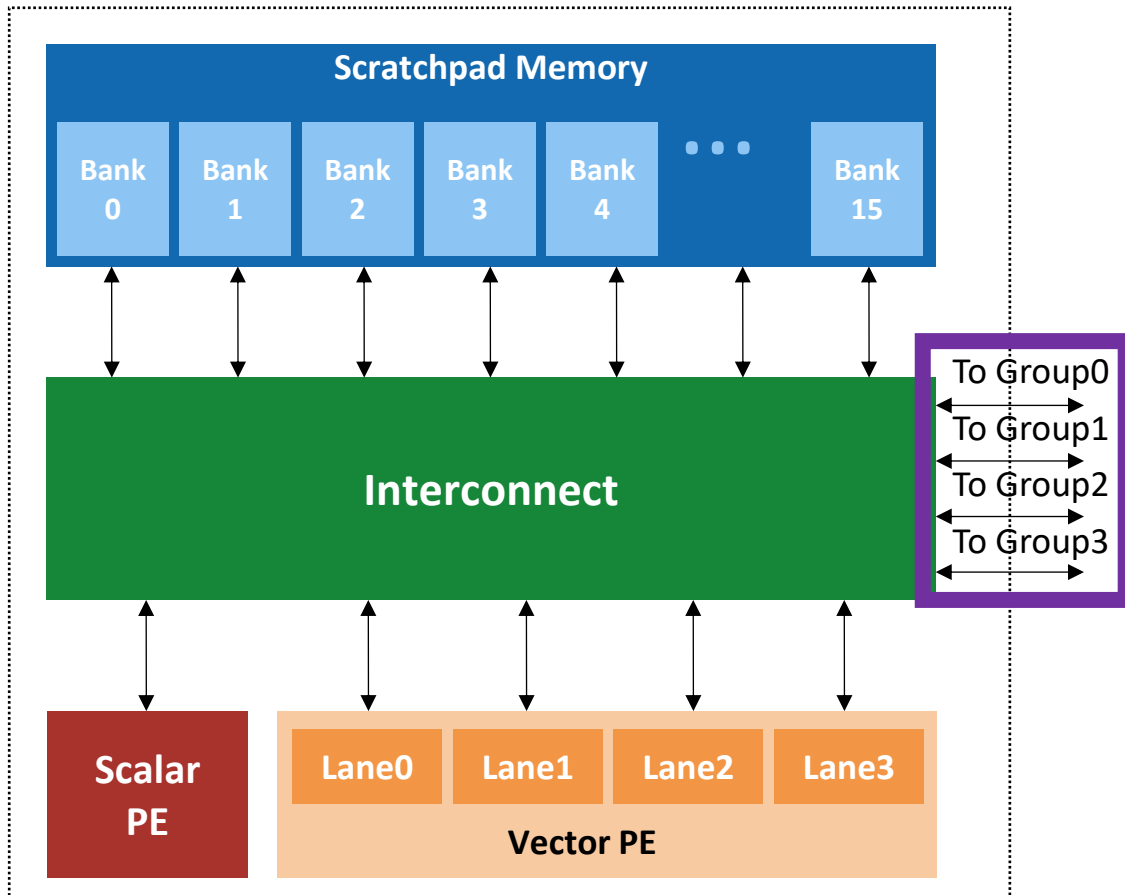
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- **Limited** routing resources for connecting hundreds of cores

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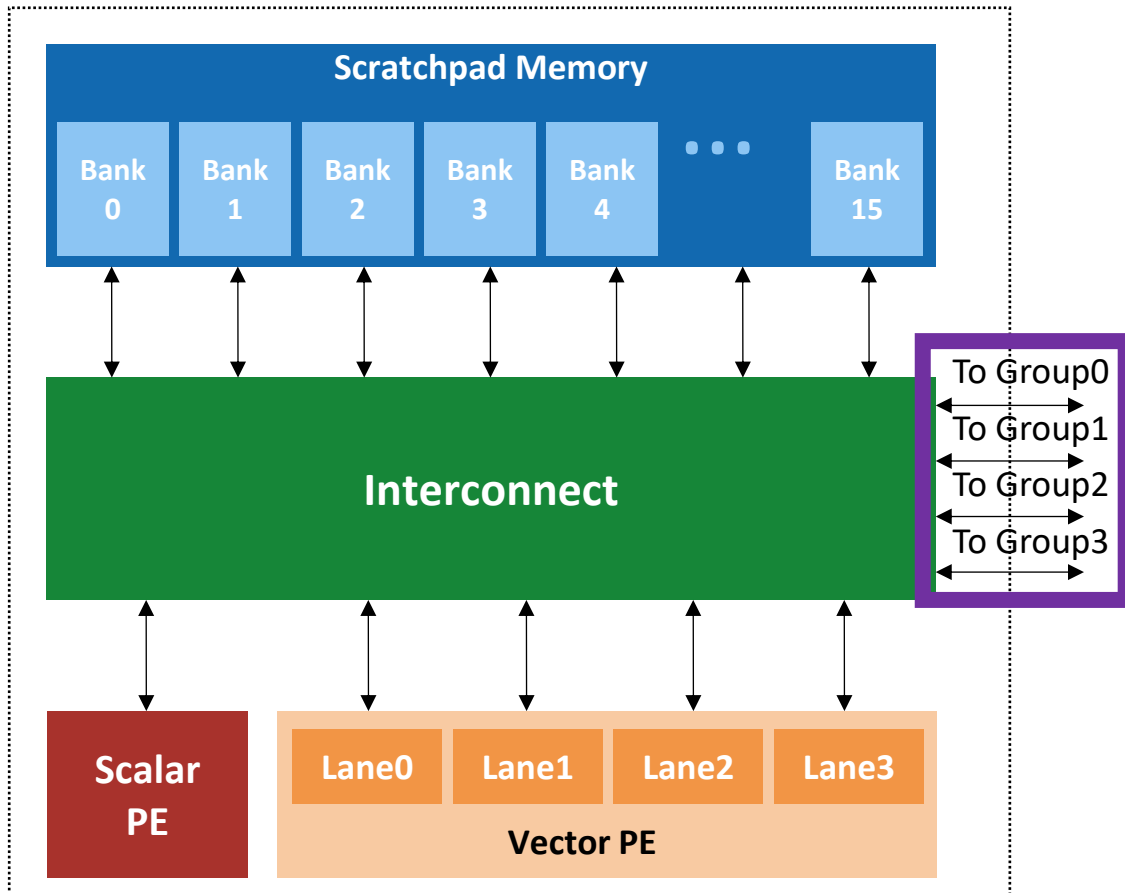
Building Block: Tile



- **Limited** routing resources for connecting hundreds of cores
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 - Physically feasible
 - Maintain low latency
 - But, limit the BW due to arbitration

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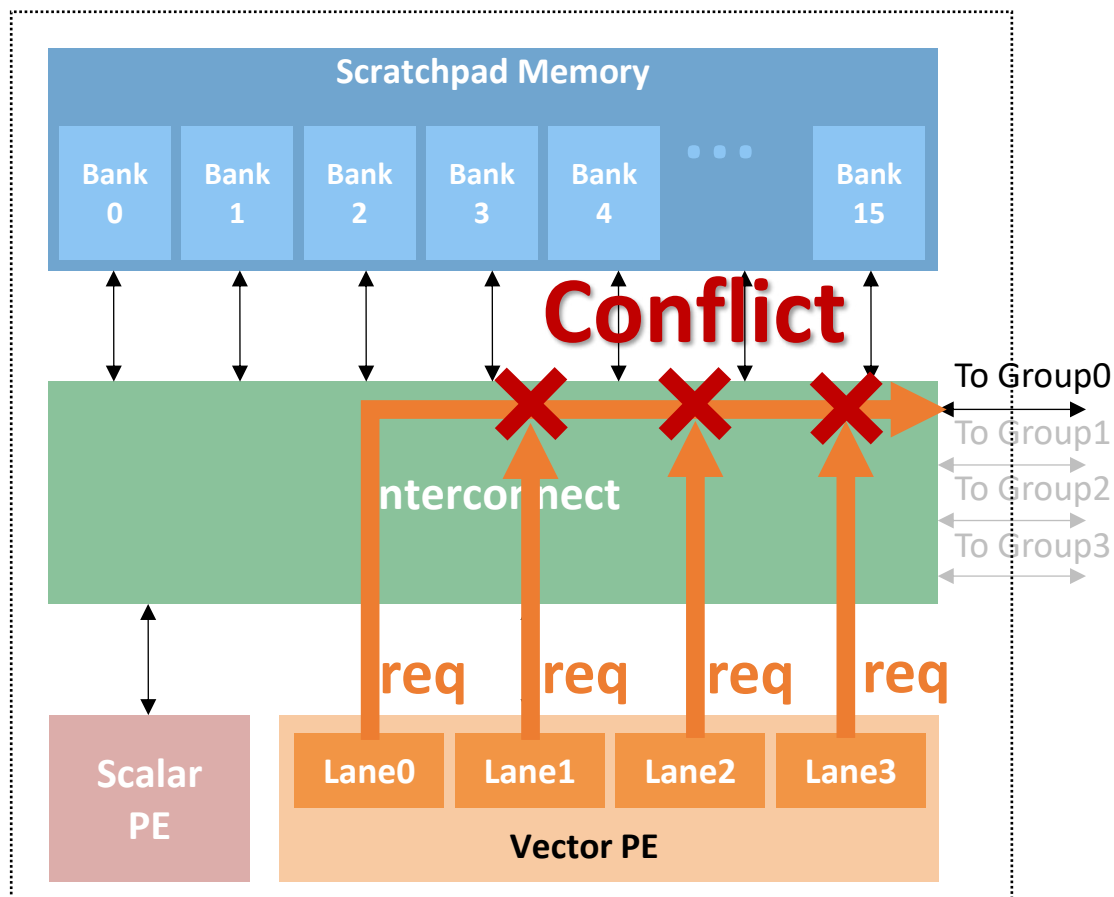
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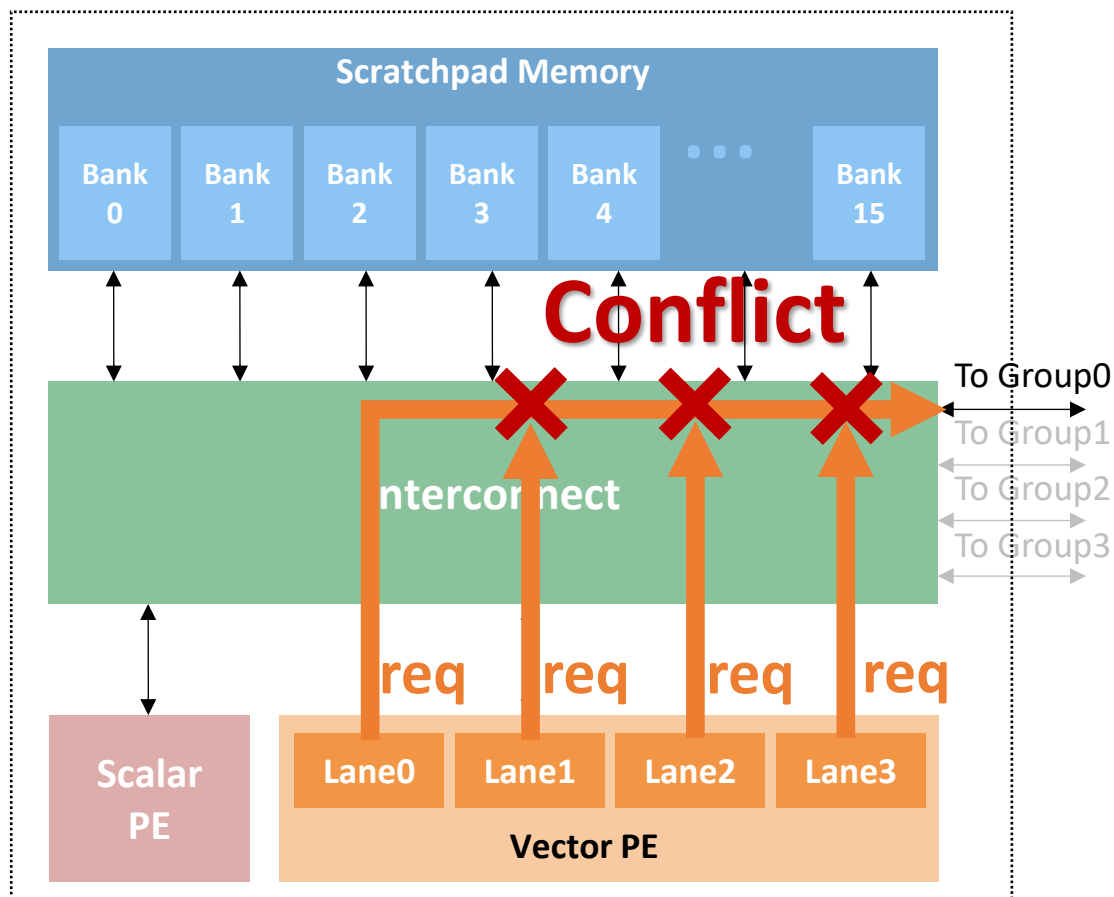
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Our Solution: TCDM Burst Access

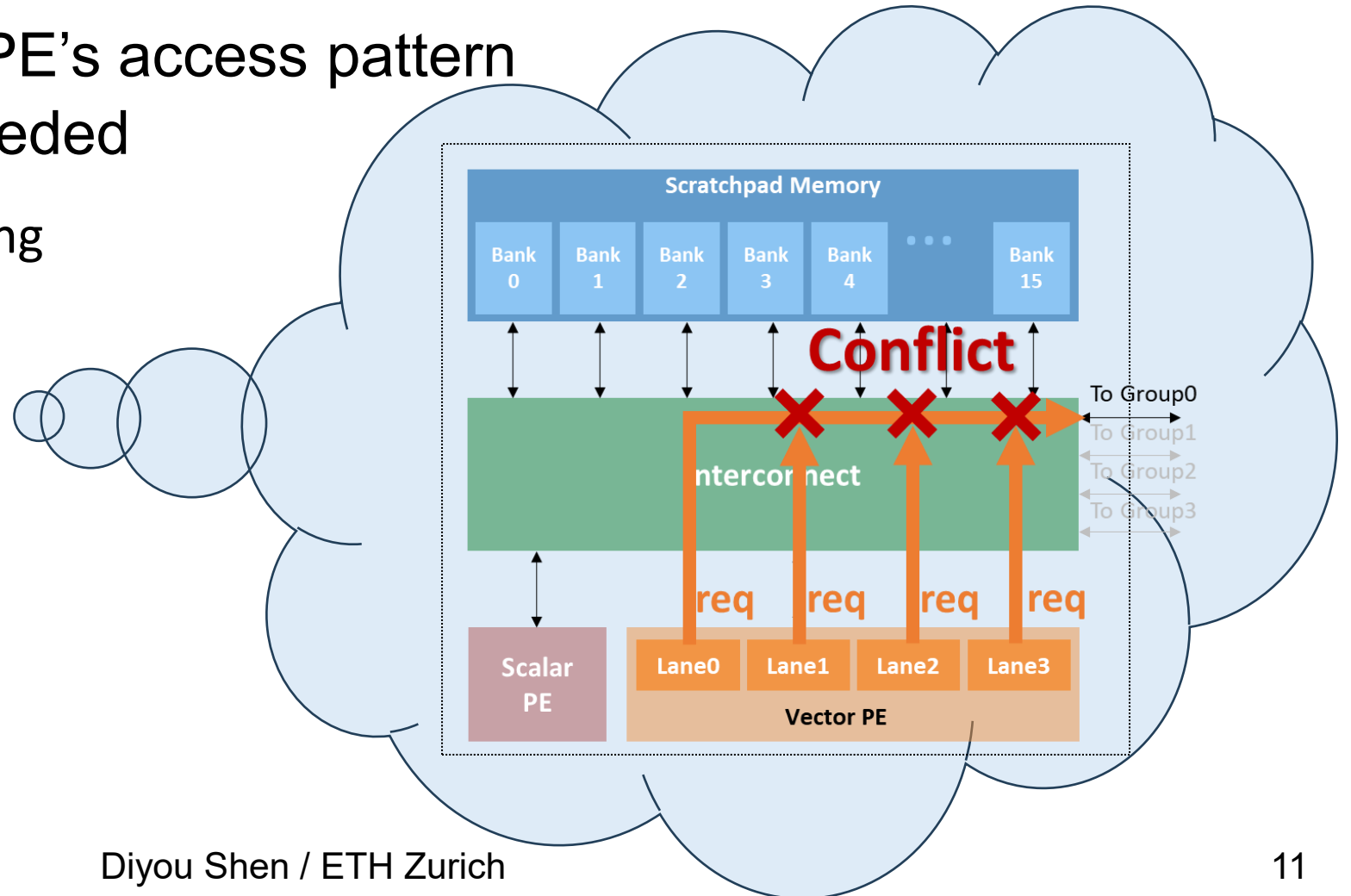
- **Pack the requests into a short burst**

- Fits well with Vector PE's access pattern
- No extra resource needed

Baseline

Vector Loading

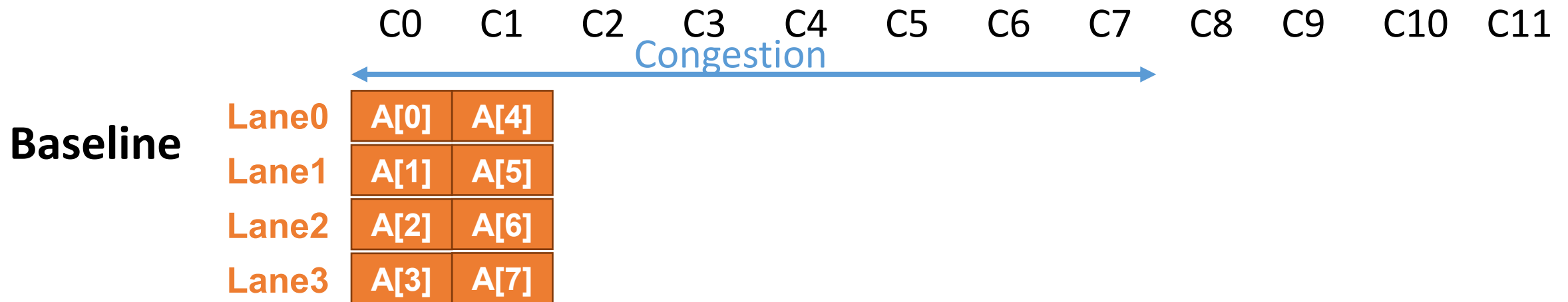
Lane0	A[0]	A[4]
Lane1	A[1]	A[5]
Lane2	A[2]	A[6]
Lane3	A[3]	A[7]



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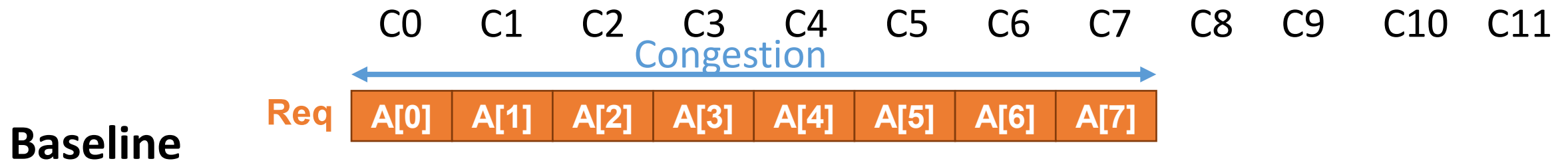
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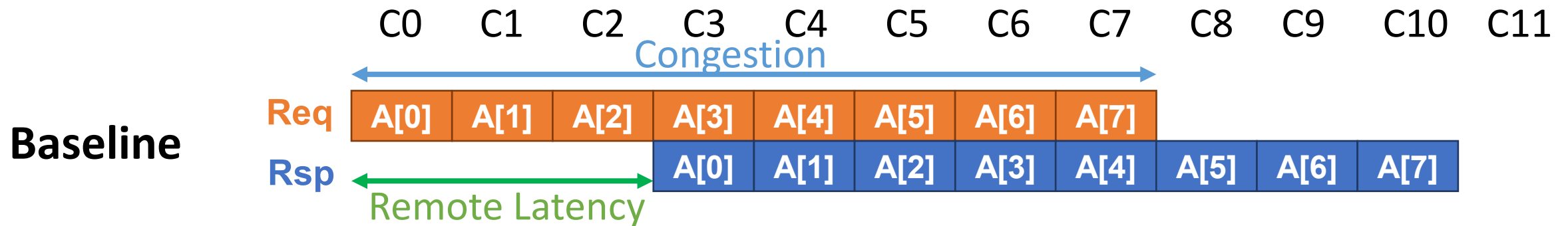
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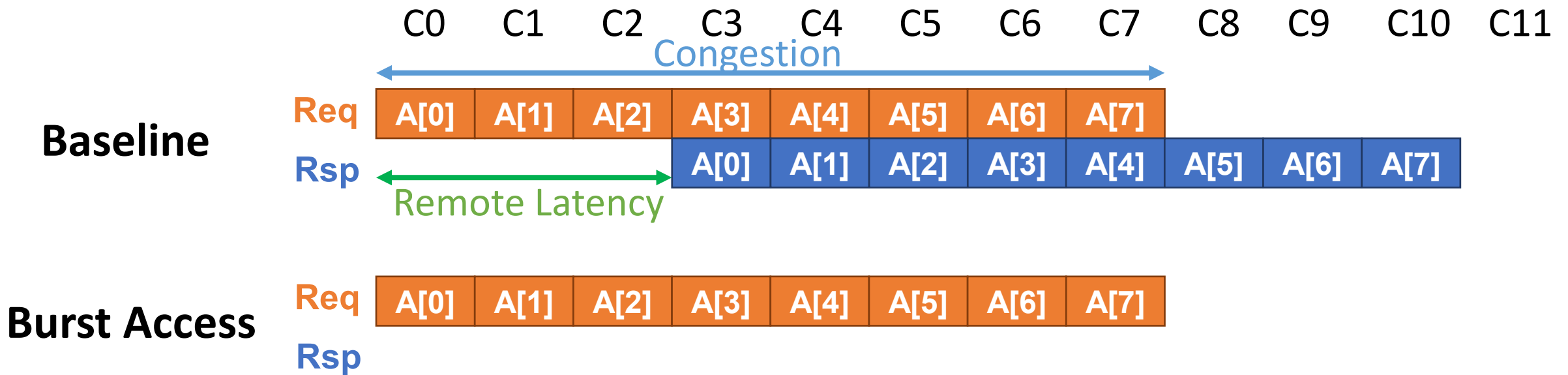
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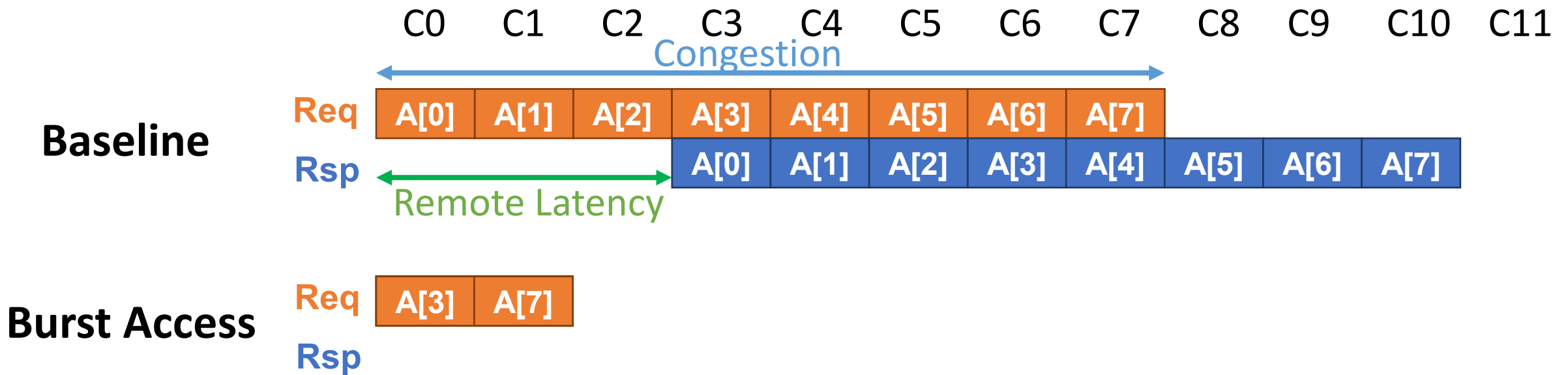
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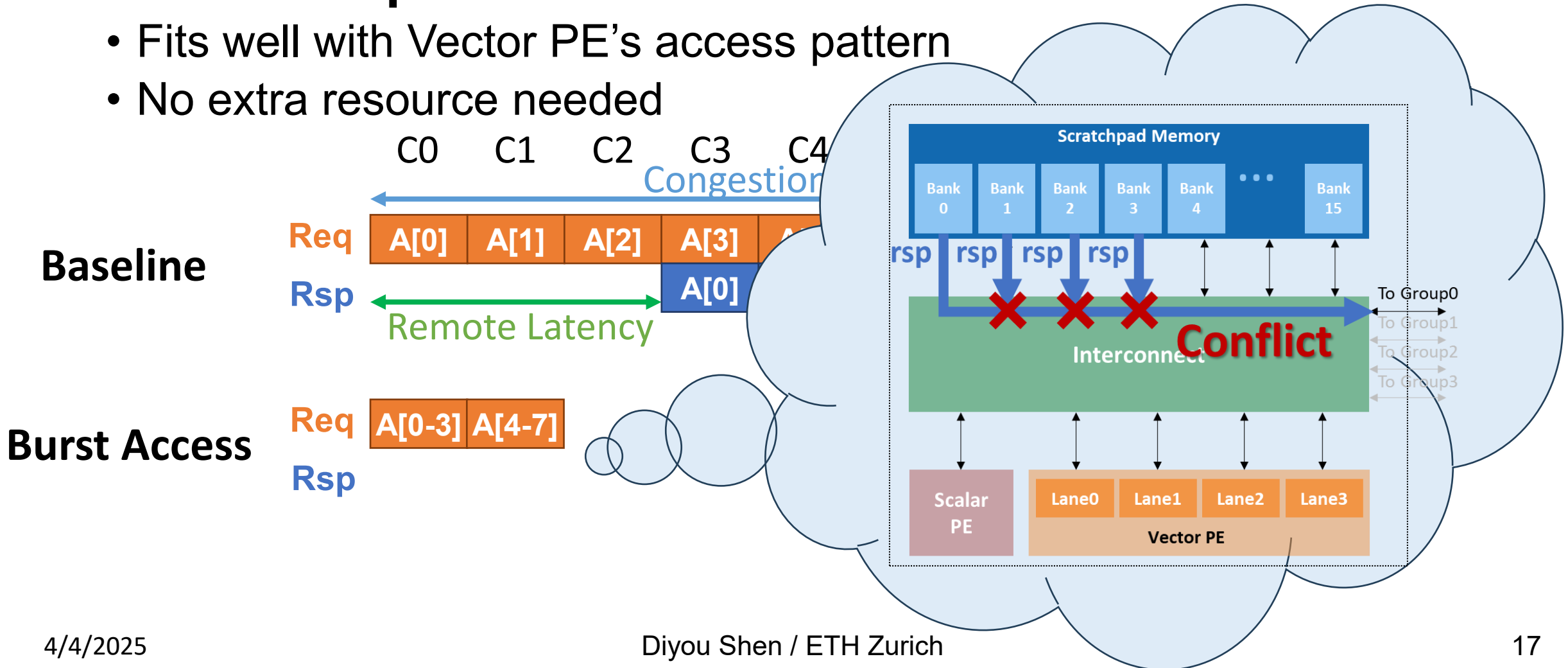
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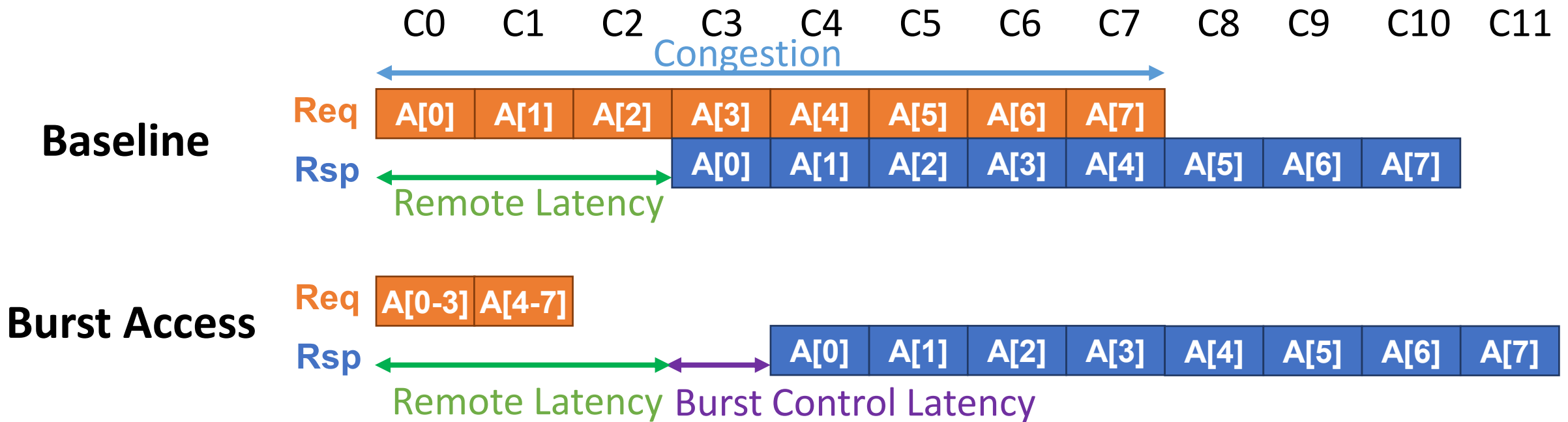
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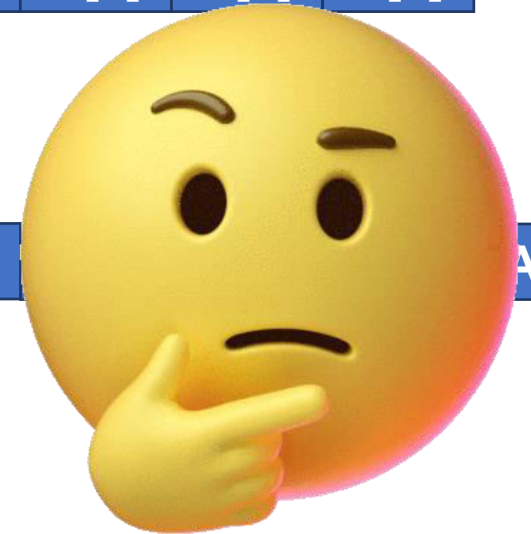
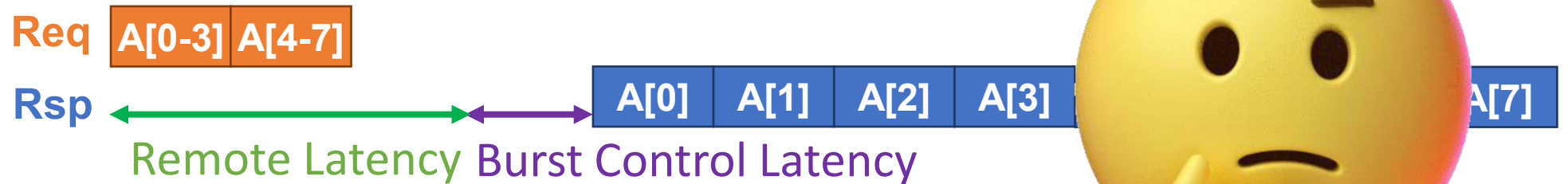
- **Pack the requests into a short burst**

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- No

We need higher data BW!

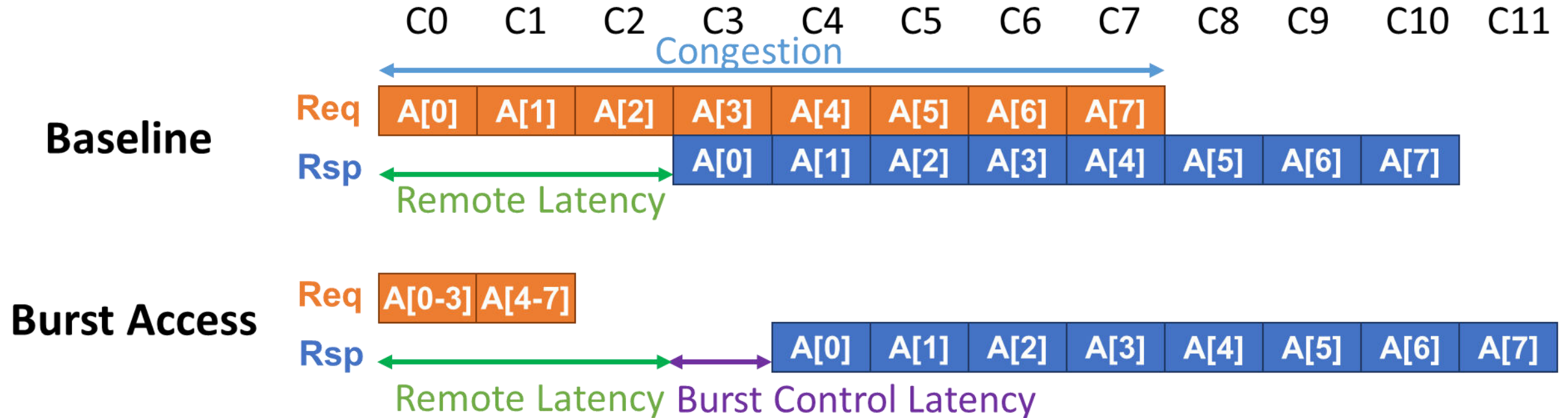


Burst Access

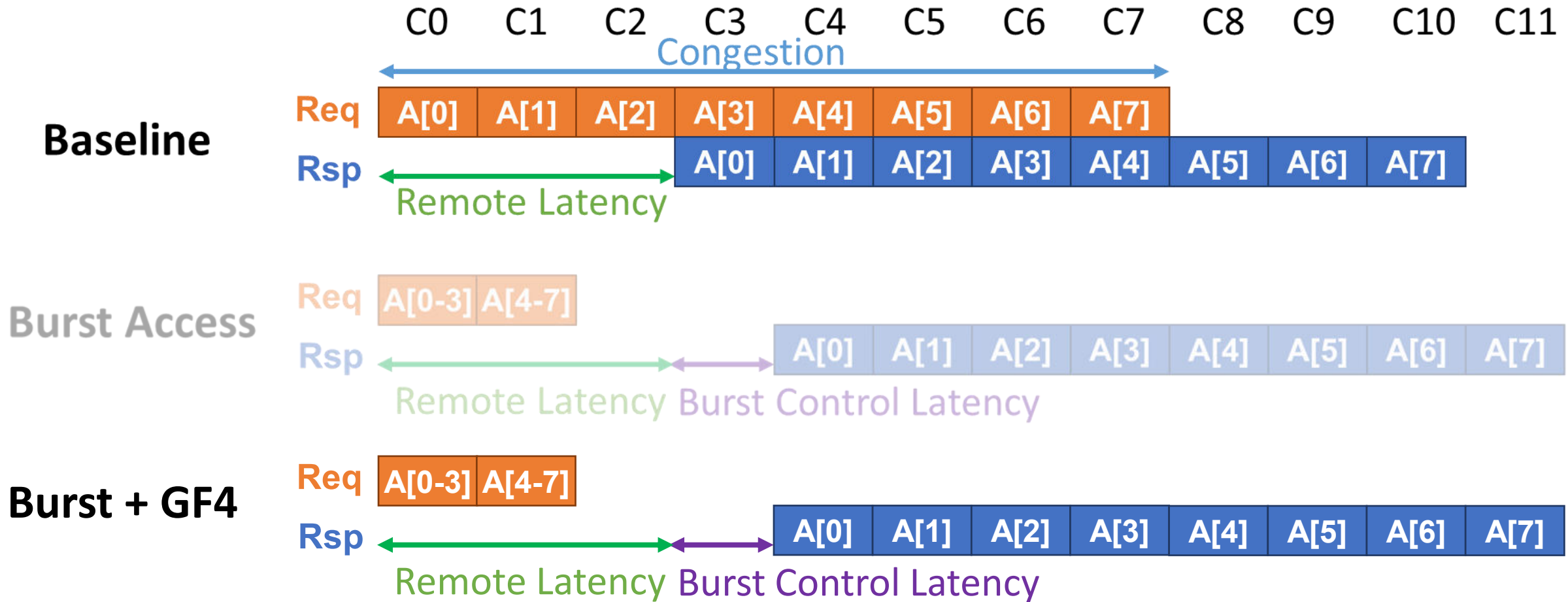


- **Group multiple data in a single transfer**
 - Have **higher data bandwidth** on response channel
 - **Minimize** the cost: only widen the response data field
 - **Configurable**: 2x data width (GF2), 4x data width (GF4), ...

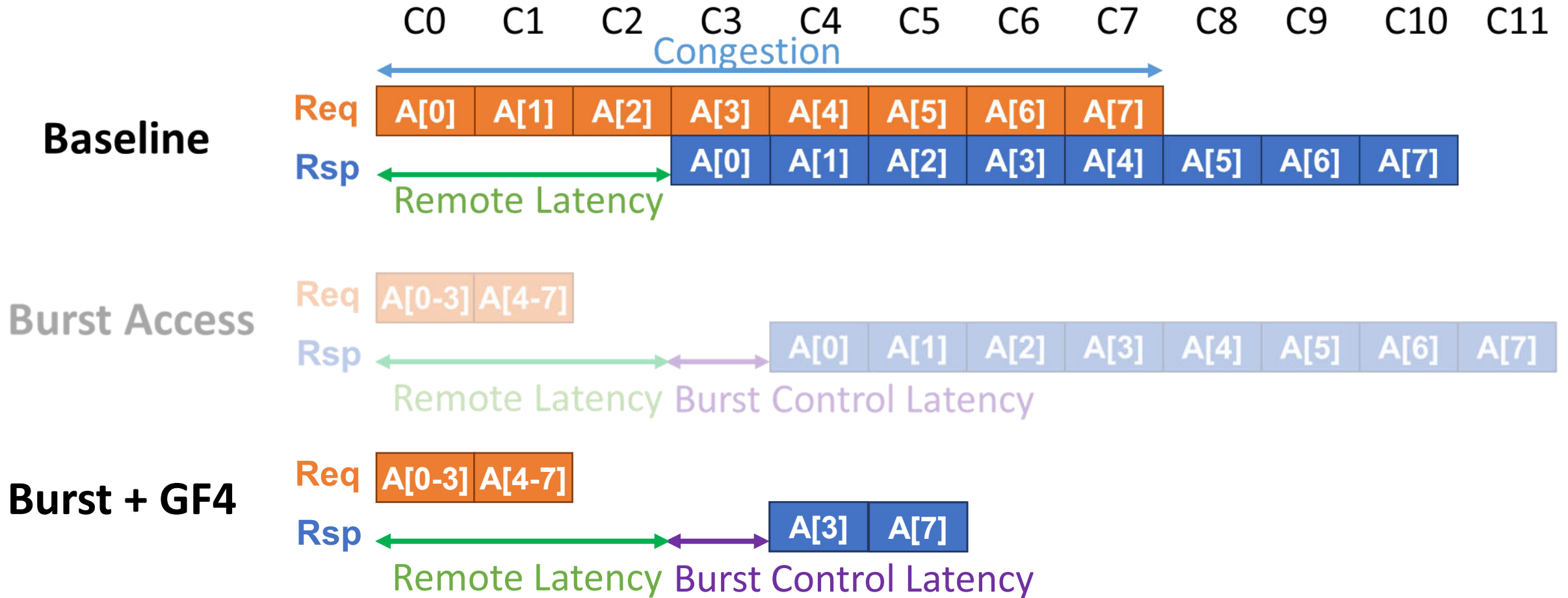
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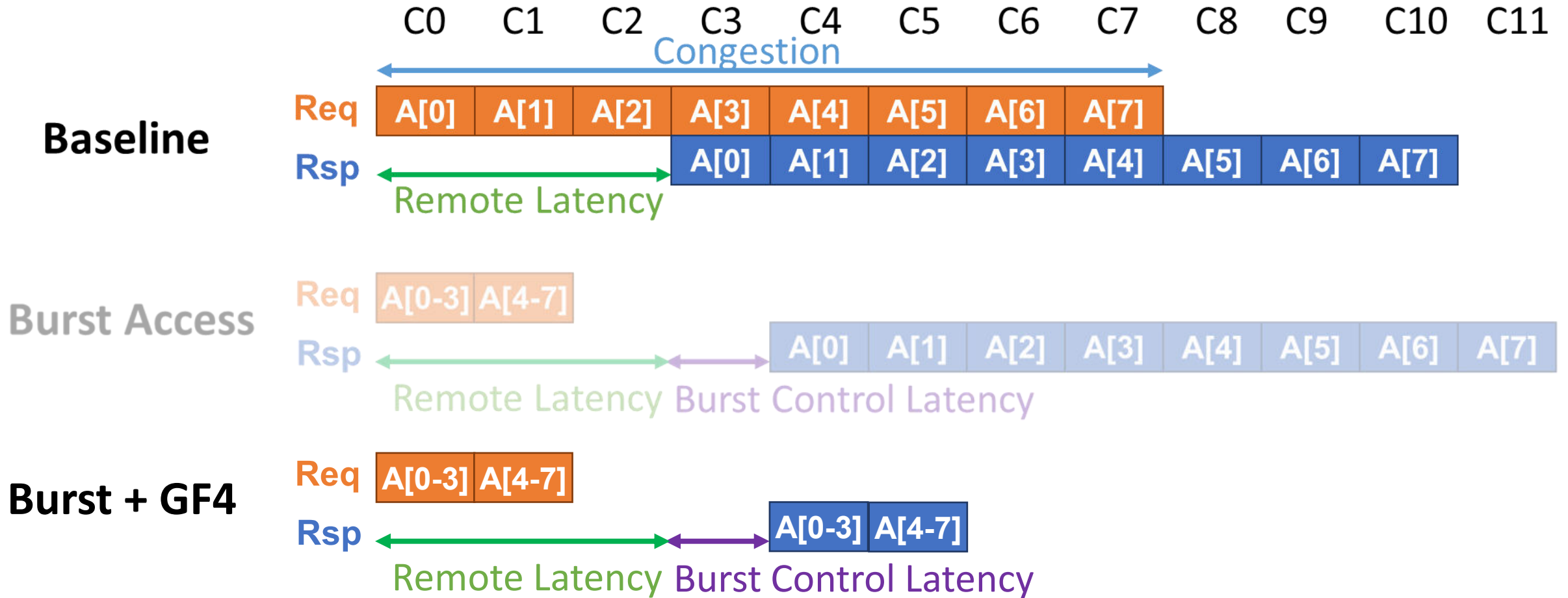
TCDM Burst Extension: Grouped Responses



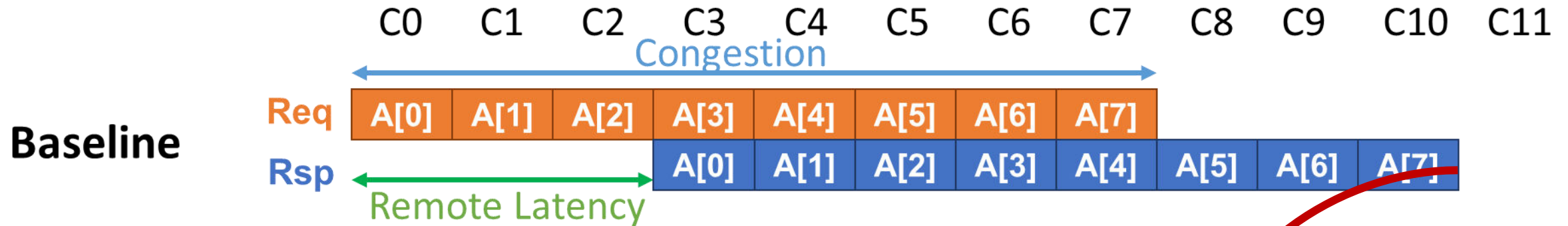
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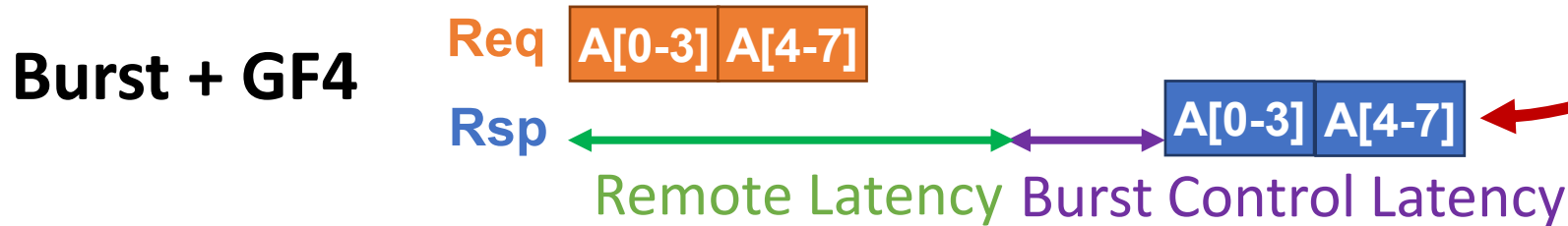
TCDM Burst Extension: Grouped Responses



Burst Access

$$Cyc_{baseline} = L_{remote} + V_{len}$$

$$Cyc_{GFK} = L_{remote} + 1 + \frac{V_{len}}{K}$$



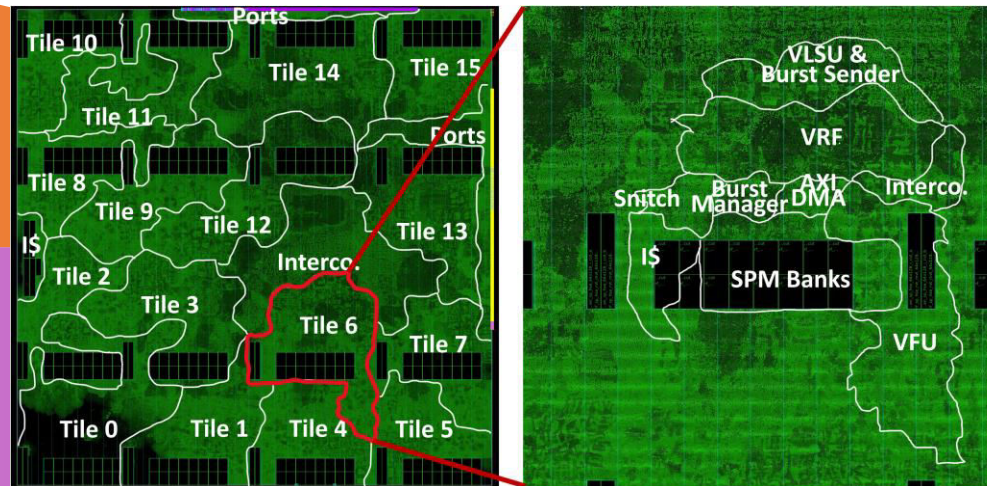
$Speedup_{GF4} \rightarrow 4$ for long vectors

Fully Routable and Highly Efficient!

Implement on MemPool₆₄-Spatz₄ Cluster in GF12 tech.

3.26x Effective BW

Up to 2.76x Performance Improvement



770 MHz @WW
Less than 7.7% Area

Up to 1.9x Energy Efficiency

We design TCDM Burst Access

- A **physically feasible, high performance, low energy** interconnection extension for **large shared-L1 clusters**.

Come to our poster and discover more!

- Tested on different cluster sizes.
- Roofline models to evaluate the designs.
- Fully **open-sourced!**



github.com/pulp-platform/mempool

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[@pulp_platform](#)



ETH zürich

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