ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

STMicroelectronics

A Fine-Grained Multithreaded RISC-V Core for Efficient and Predictable Real-Time Microcontrollers

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ETH Zürich, Switzerland[3] Fondazione Chips-IT[4]

Motivation

Context

Microcontroller Unit (**MCU**) designs must adhere to **strict constraints**:

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Solution

FGMT can address both in **efficient way!**

Contribution

1 **Dual-Threaded Fine-Grained Multithreading (FGMT) on a RISC-V Pipeline**

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2. **Thread Forwarding (TFW) Enhancement to FGMT**

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4. Physical Implementation & PPA Analysis in commercial technology

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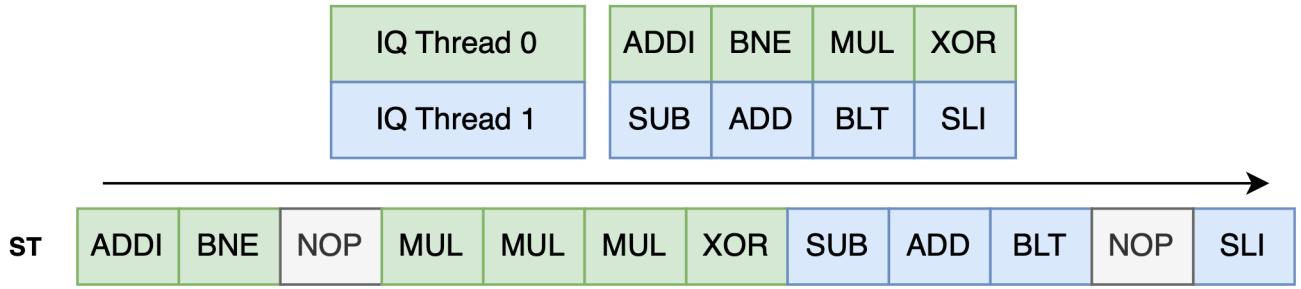

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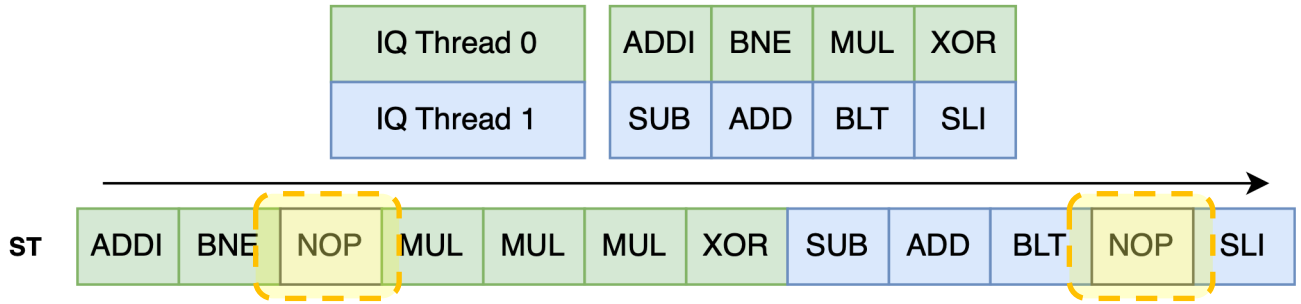

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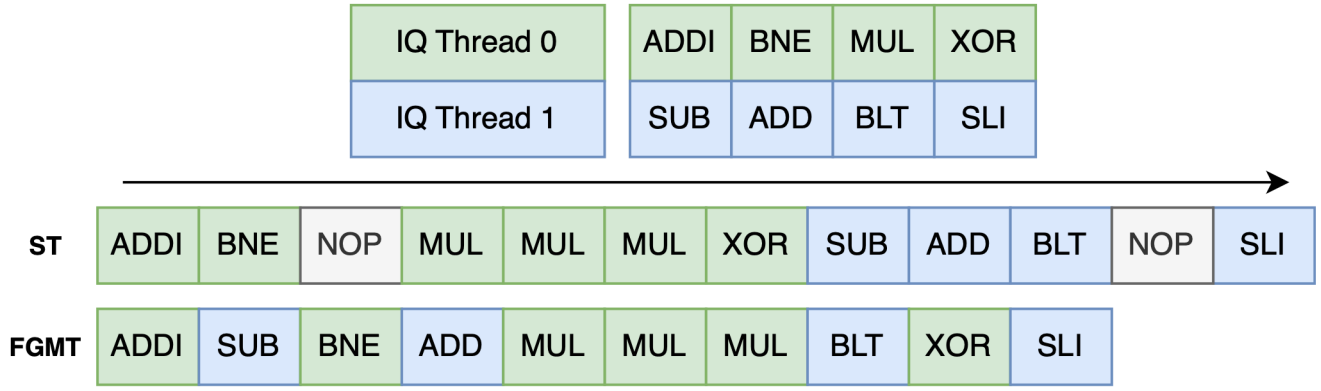

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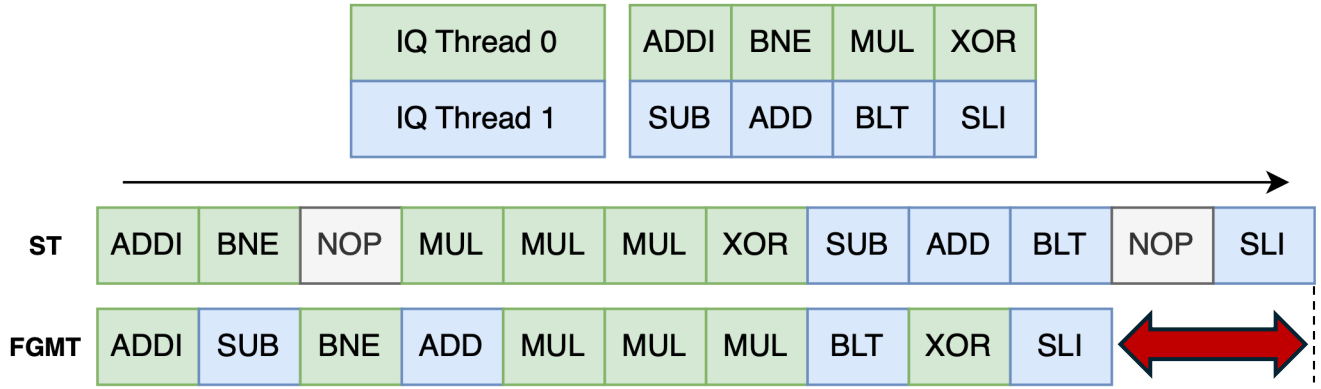

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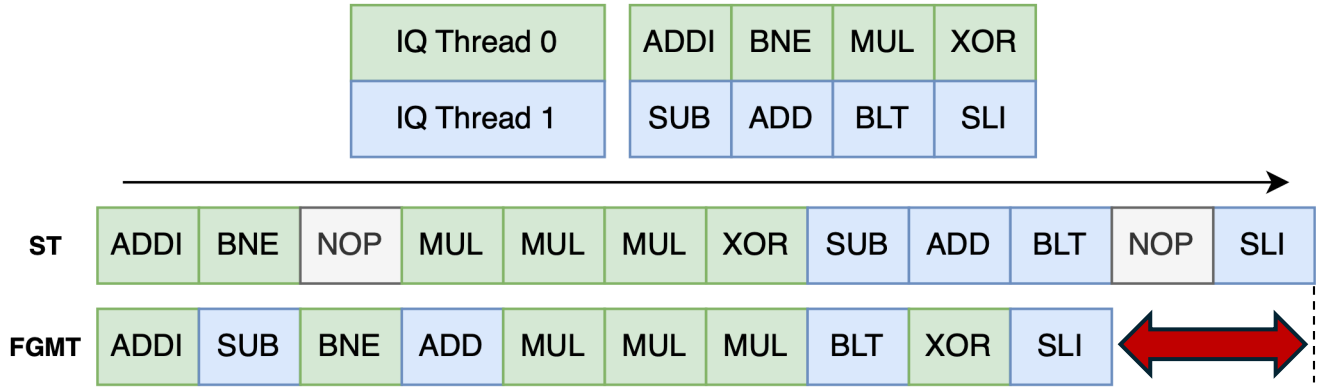

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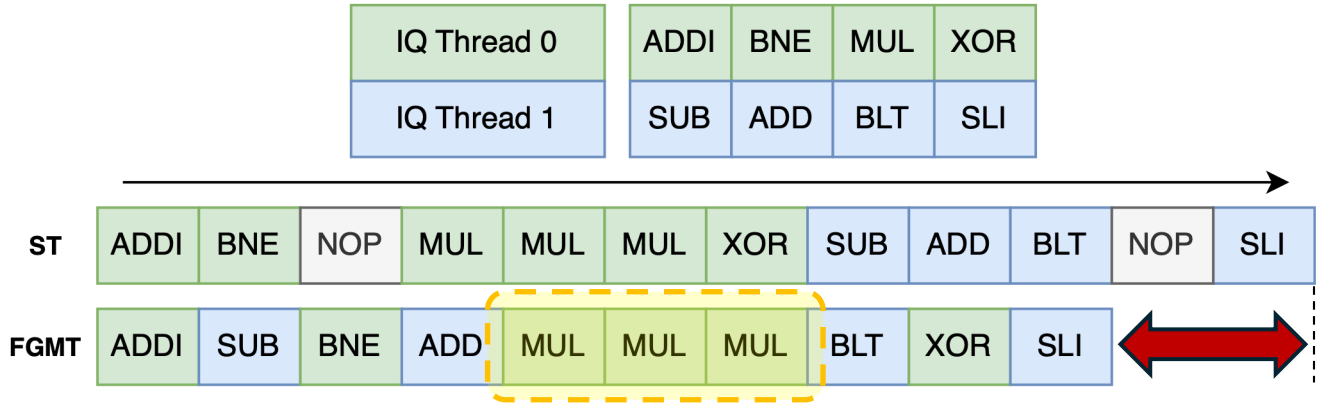

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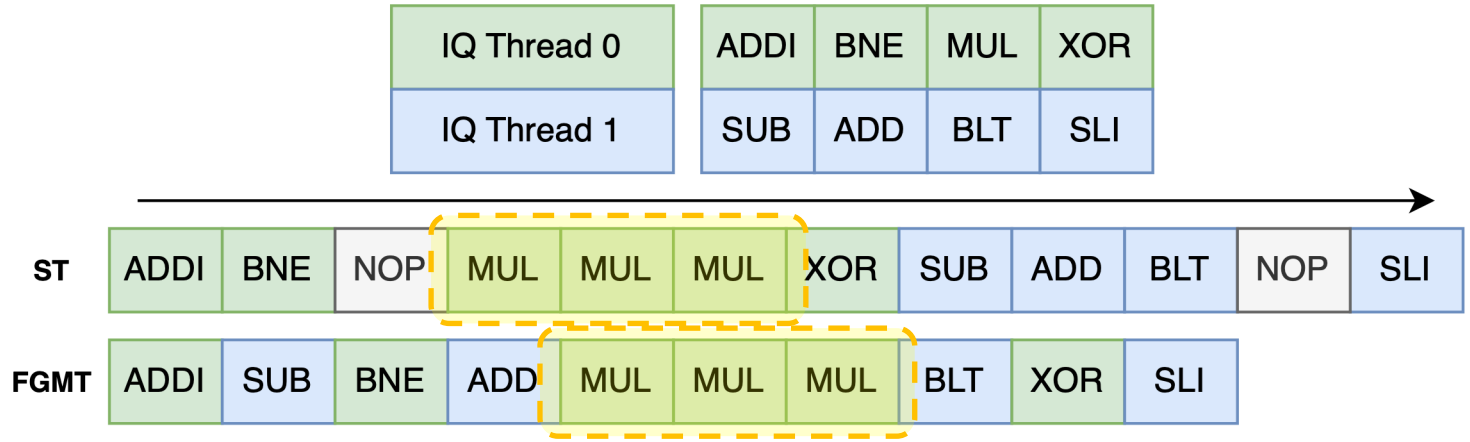

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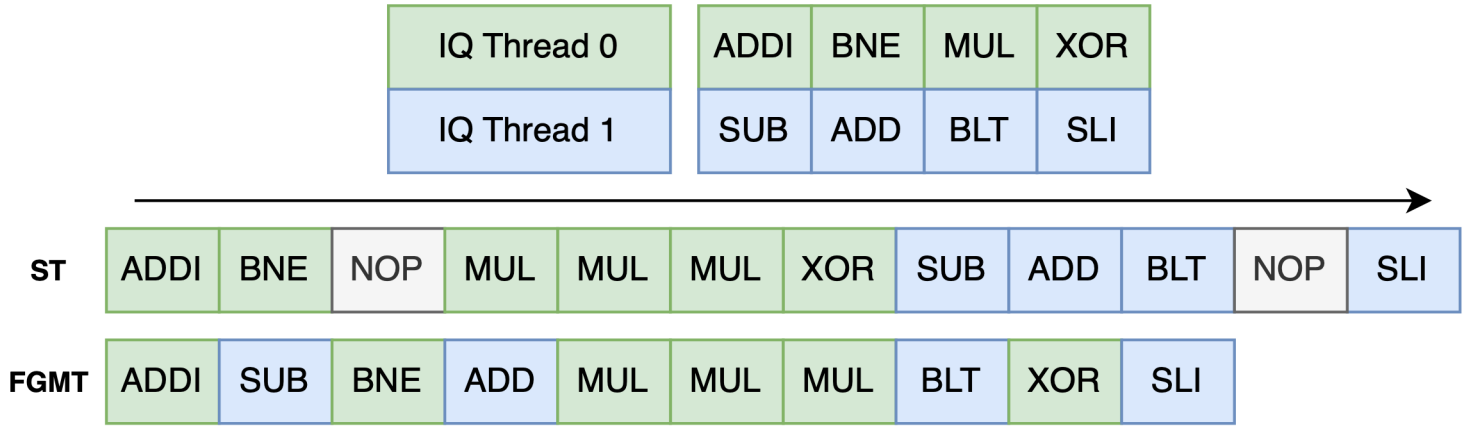

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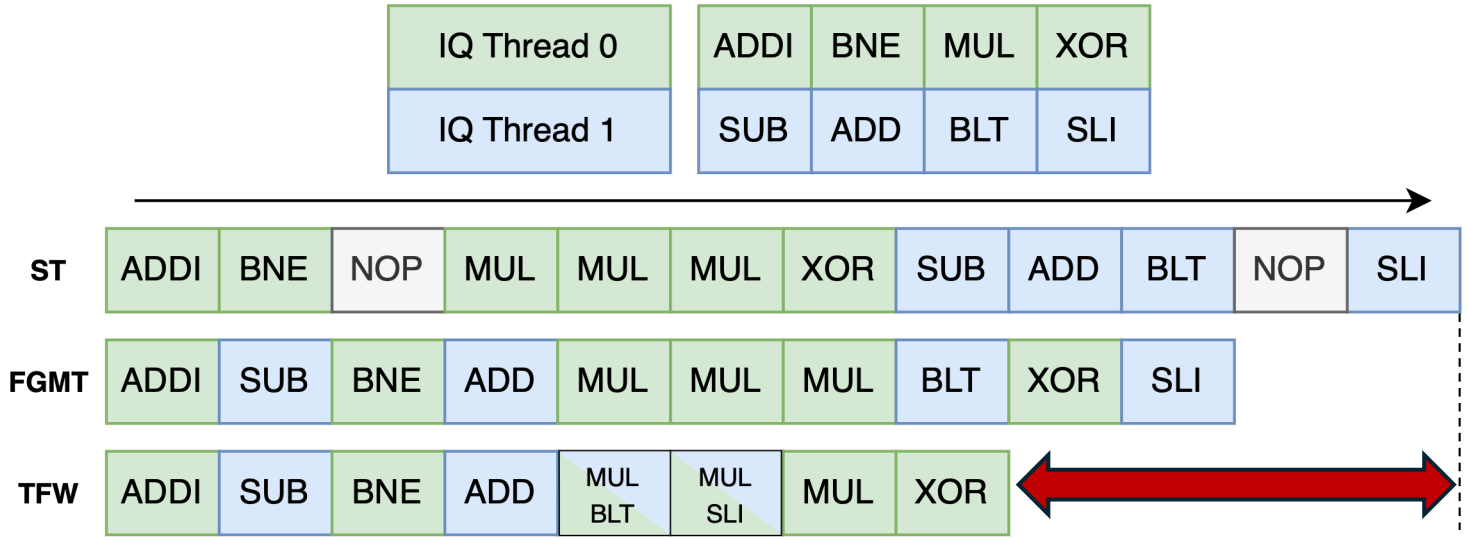
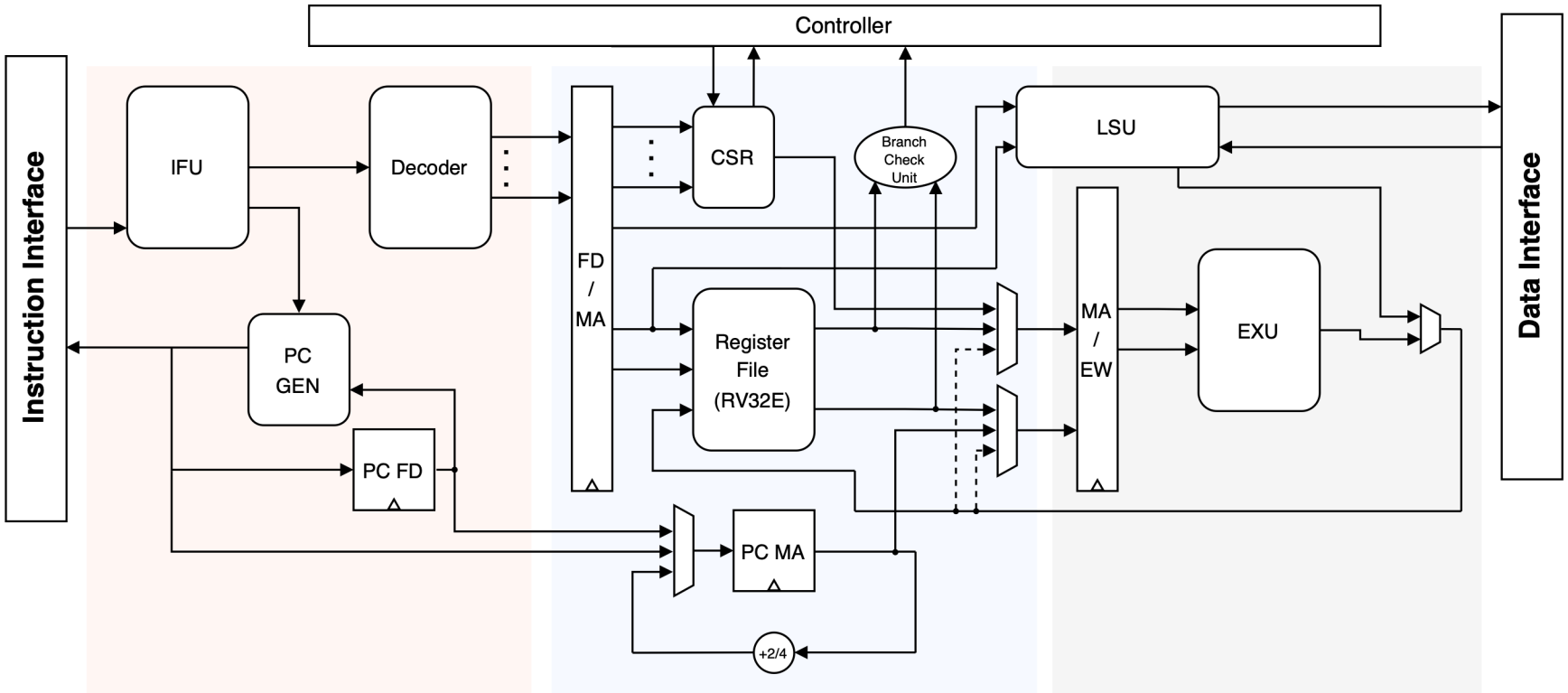
The **alternative thread** can **utilize** the **idle** functional units



Baseline core: STRIVE-L

STRIVE-L, an industrial **RISC-V** baseline optimized for low-area and low-power **embedded applications**



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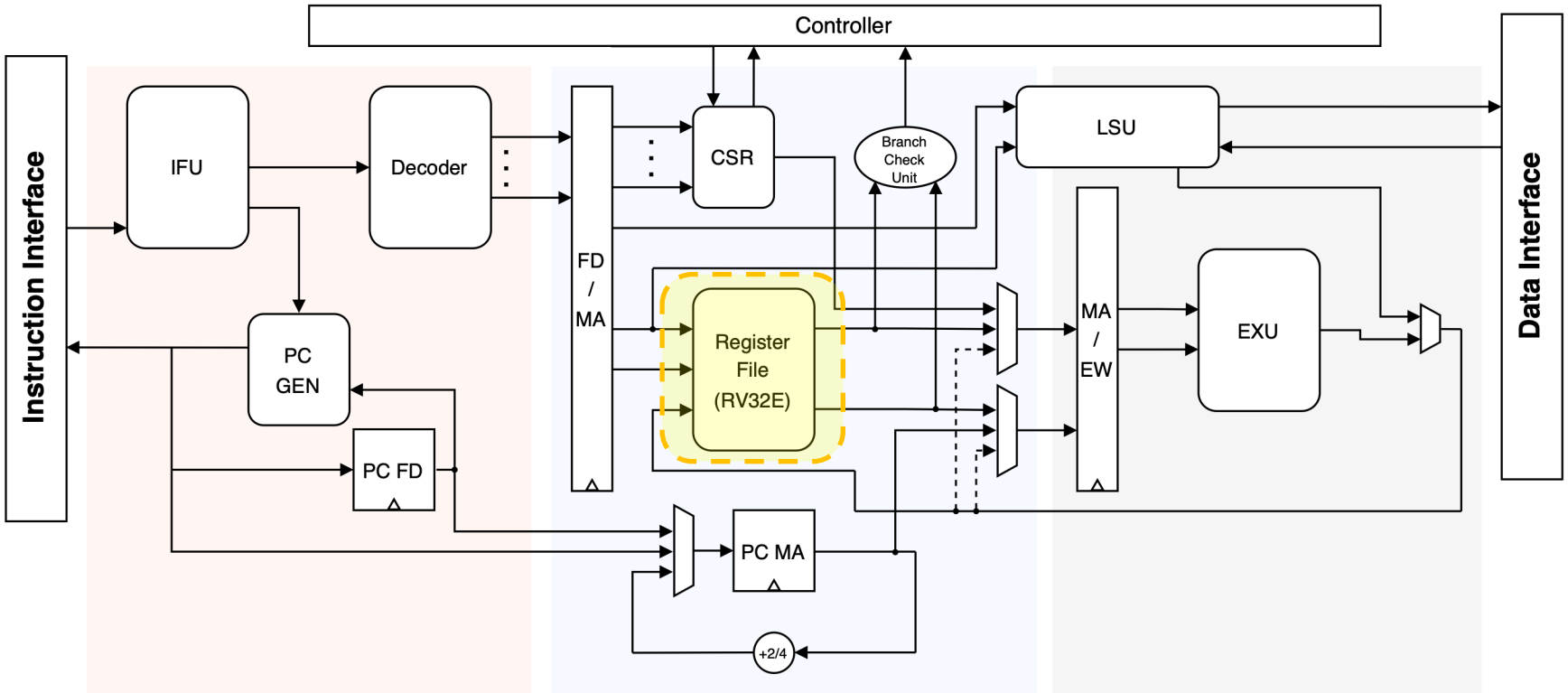

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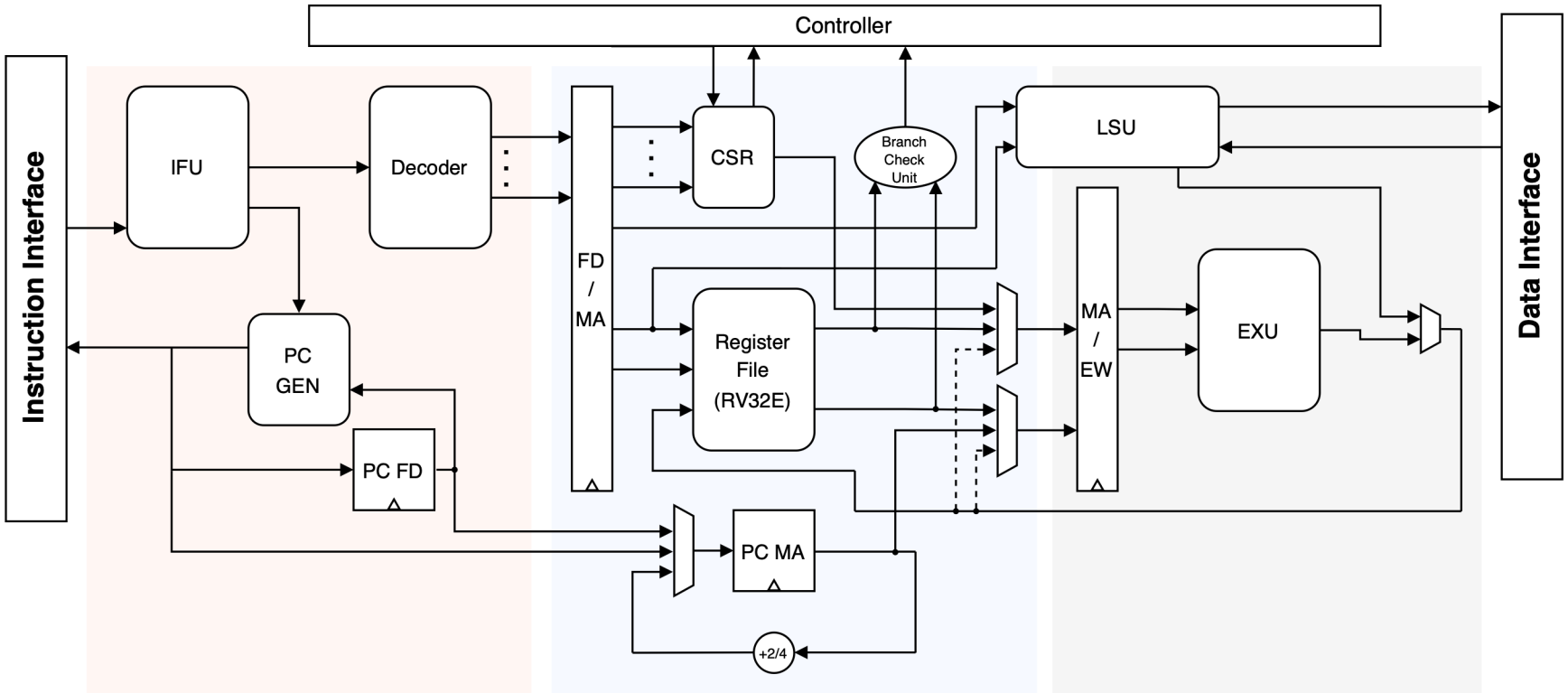

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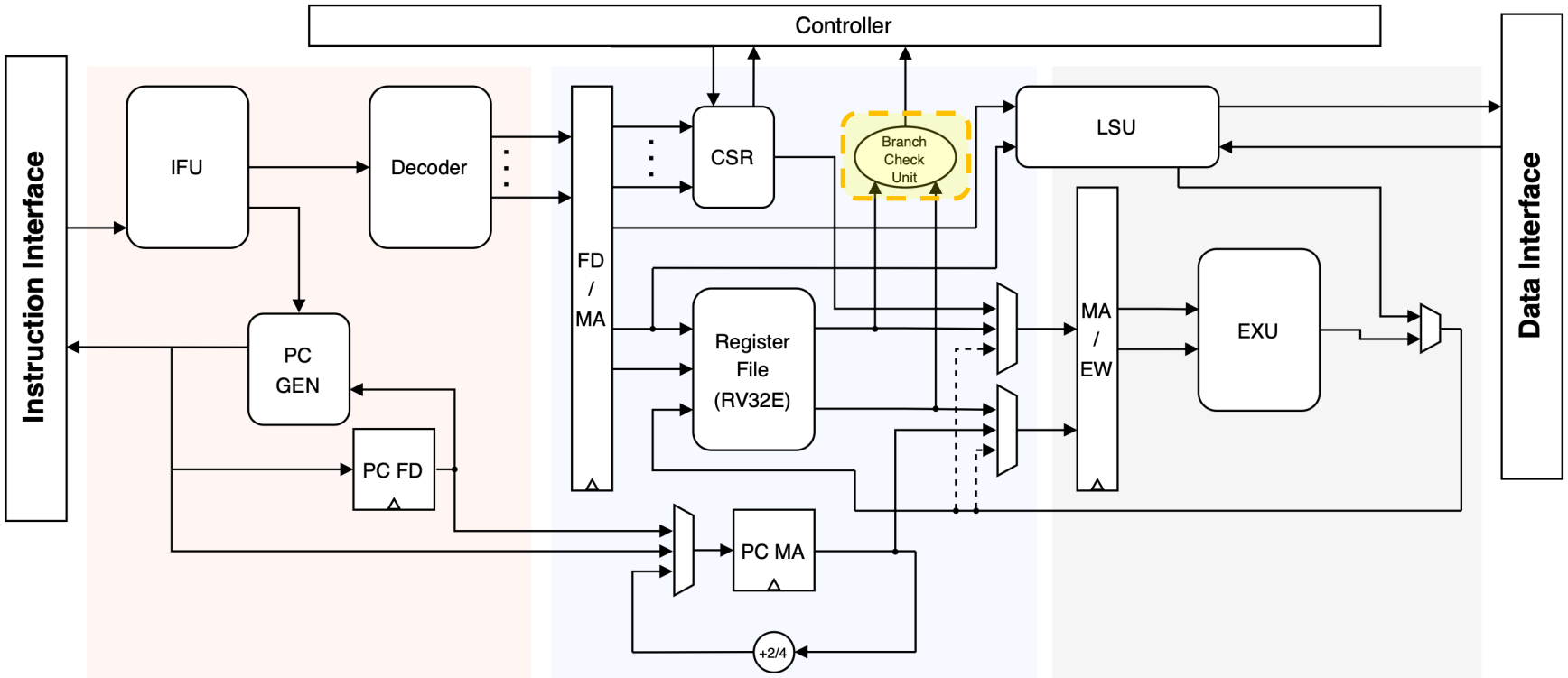

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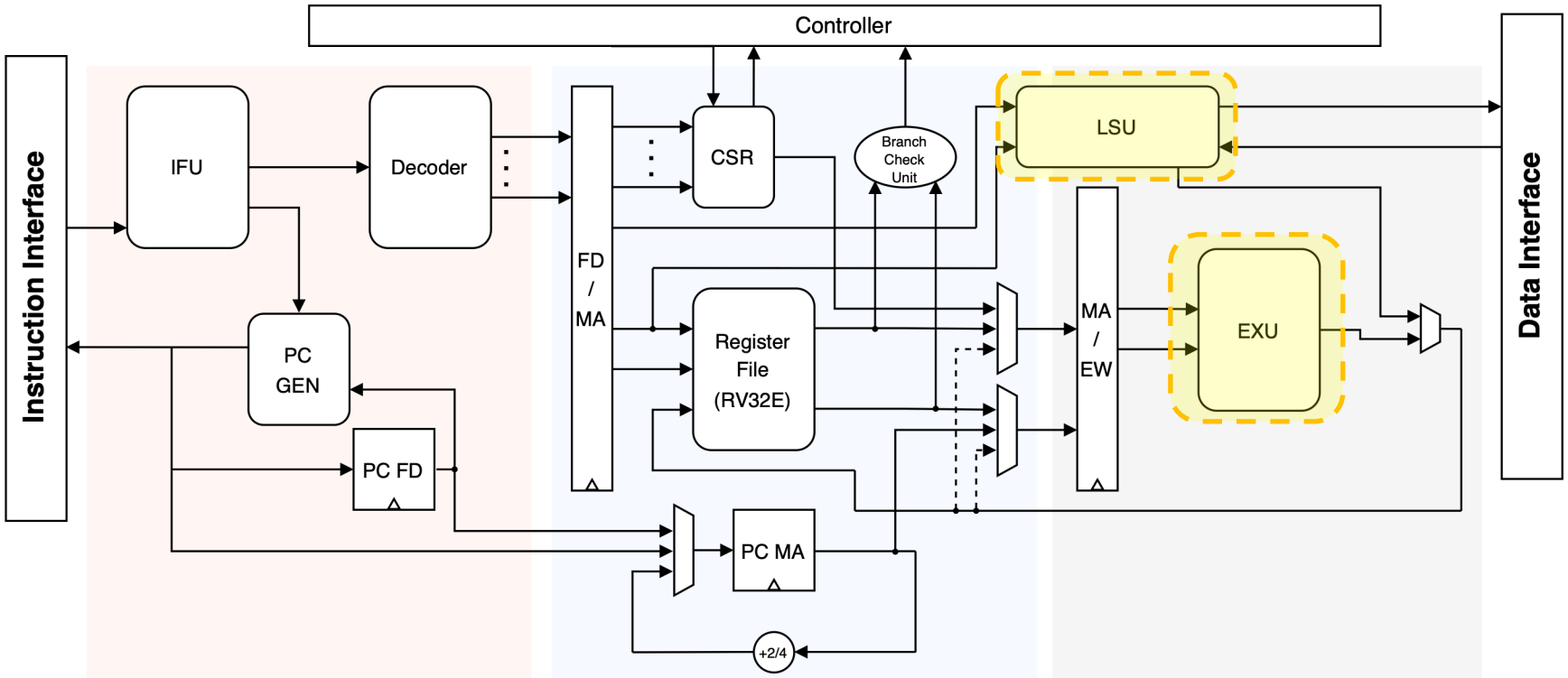

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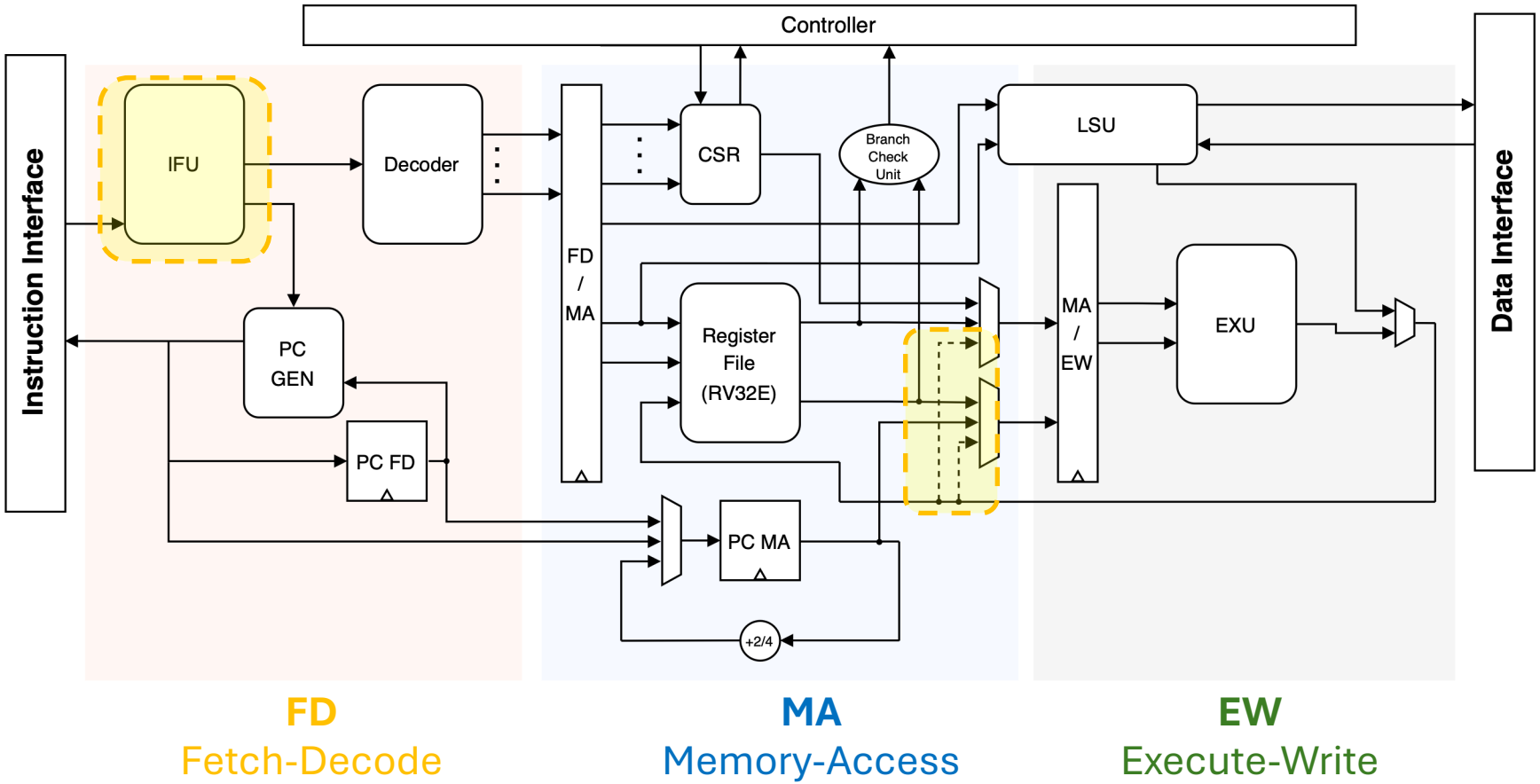

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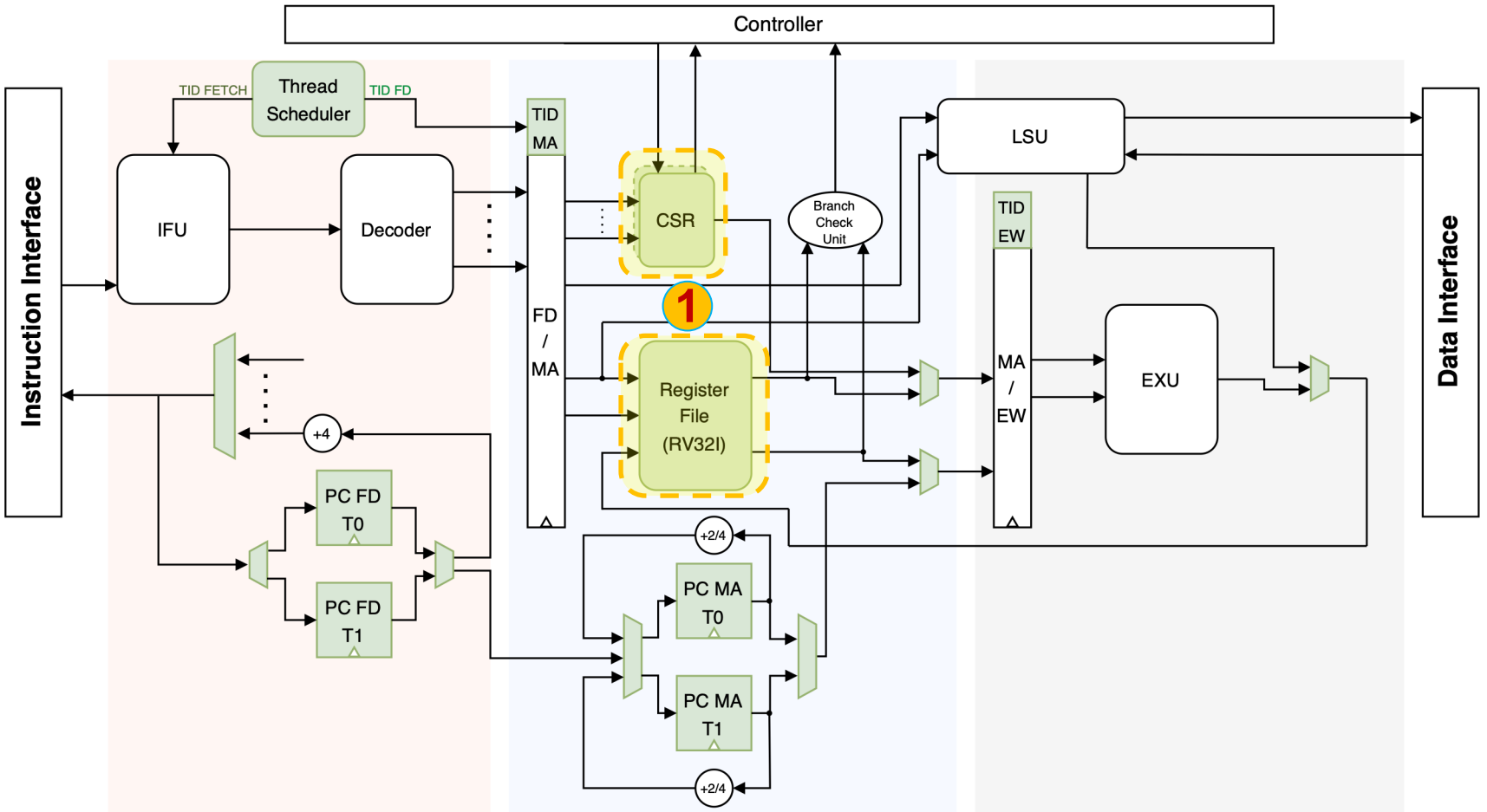

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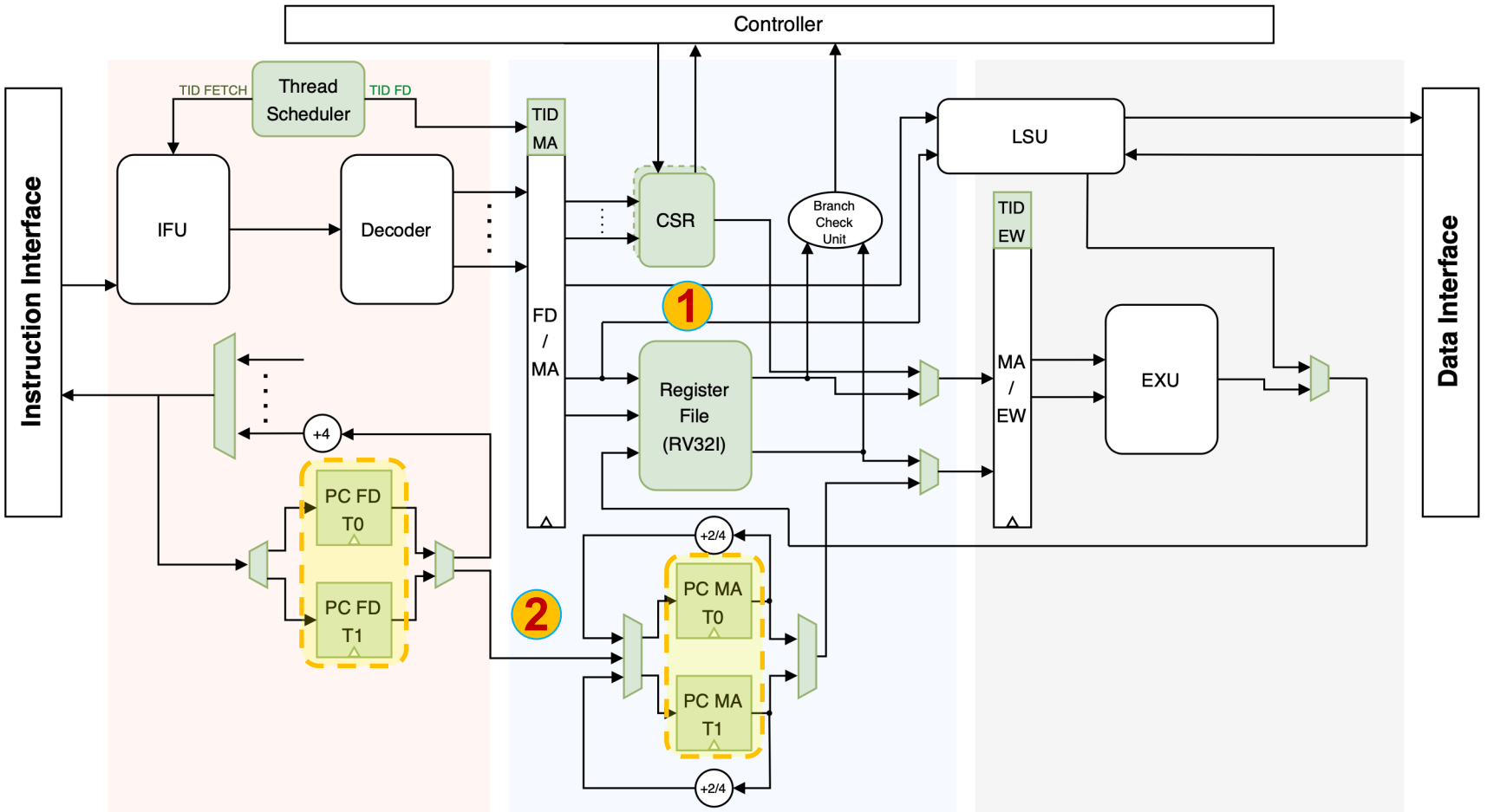

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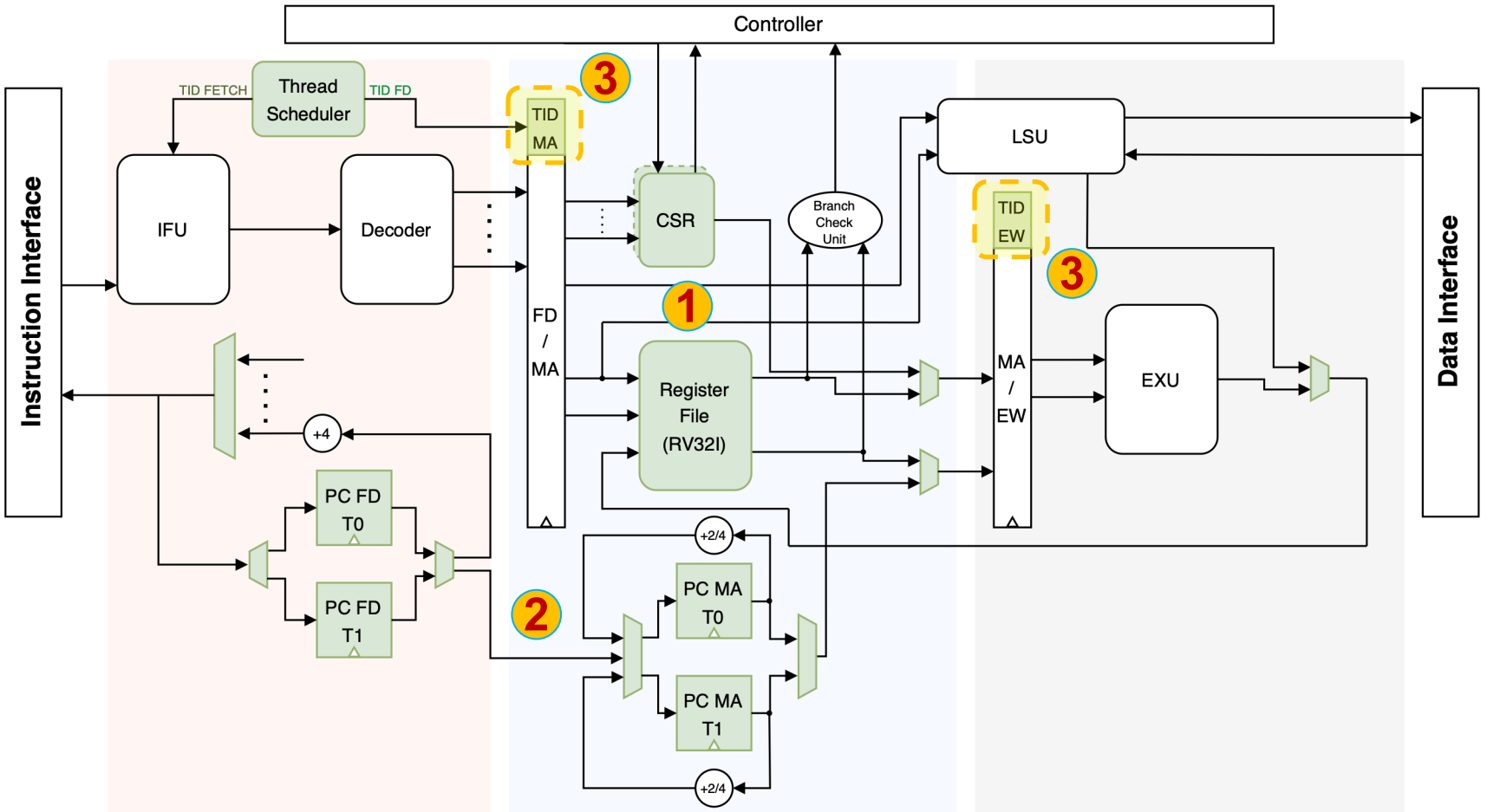

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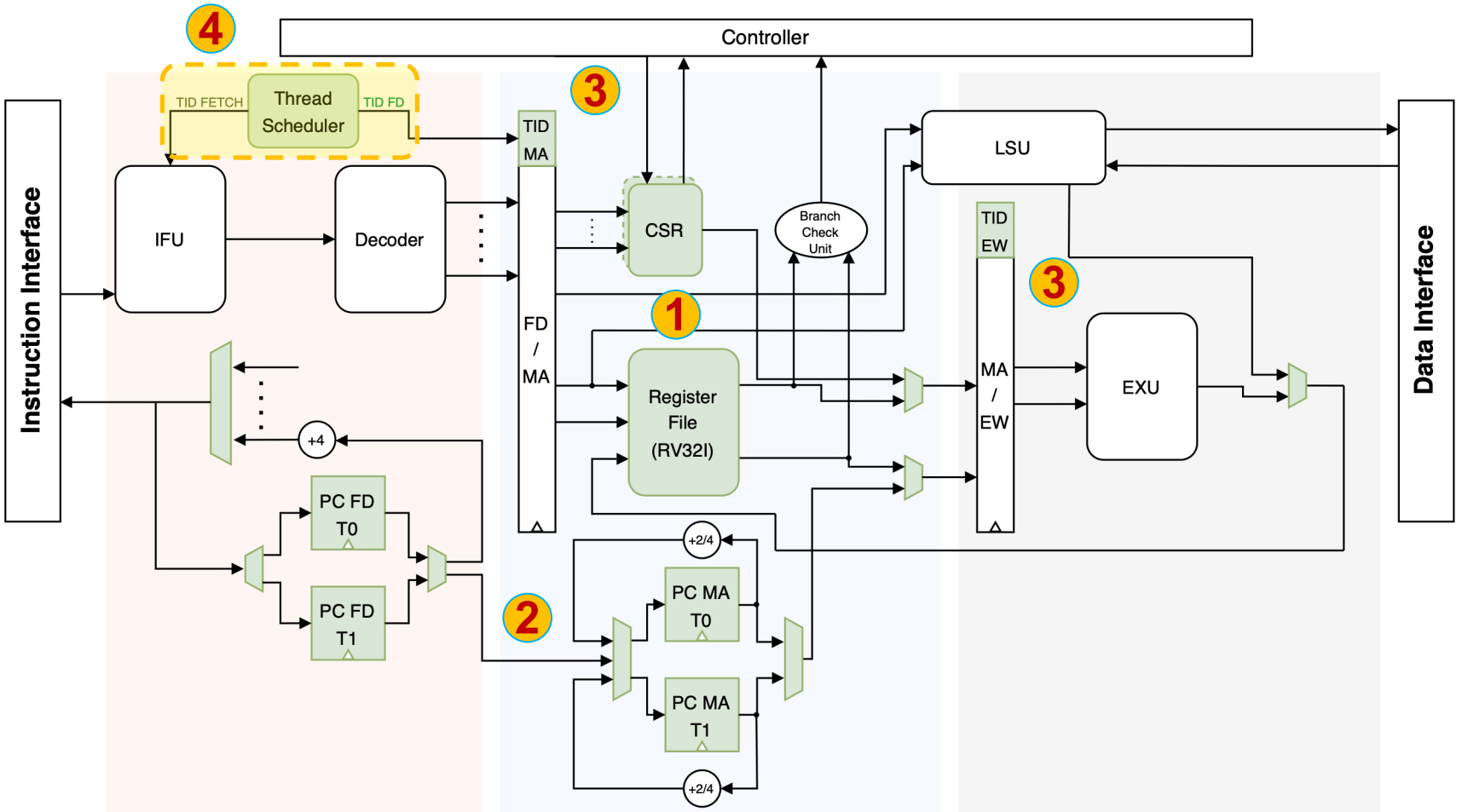

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***Strictly alternates** the active thread every clock cycle to **interleave instructions and mask hazards**.*

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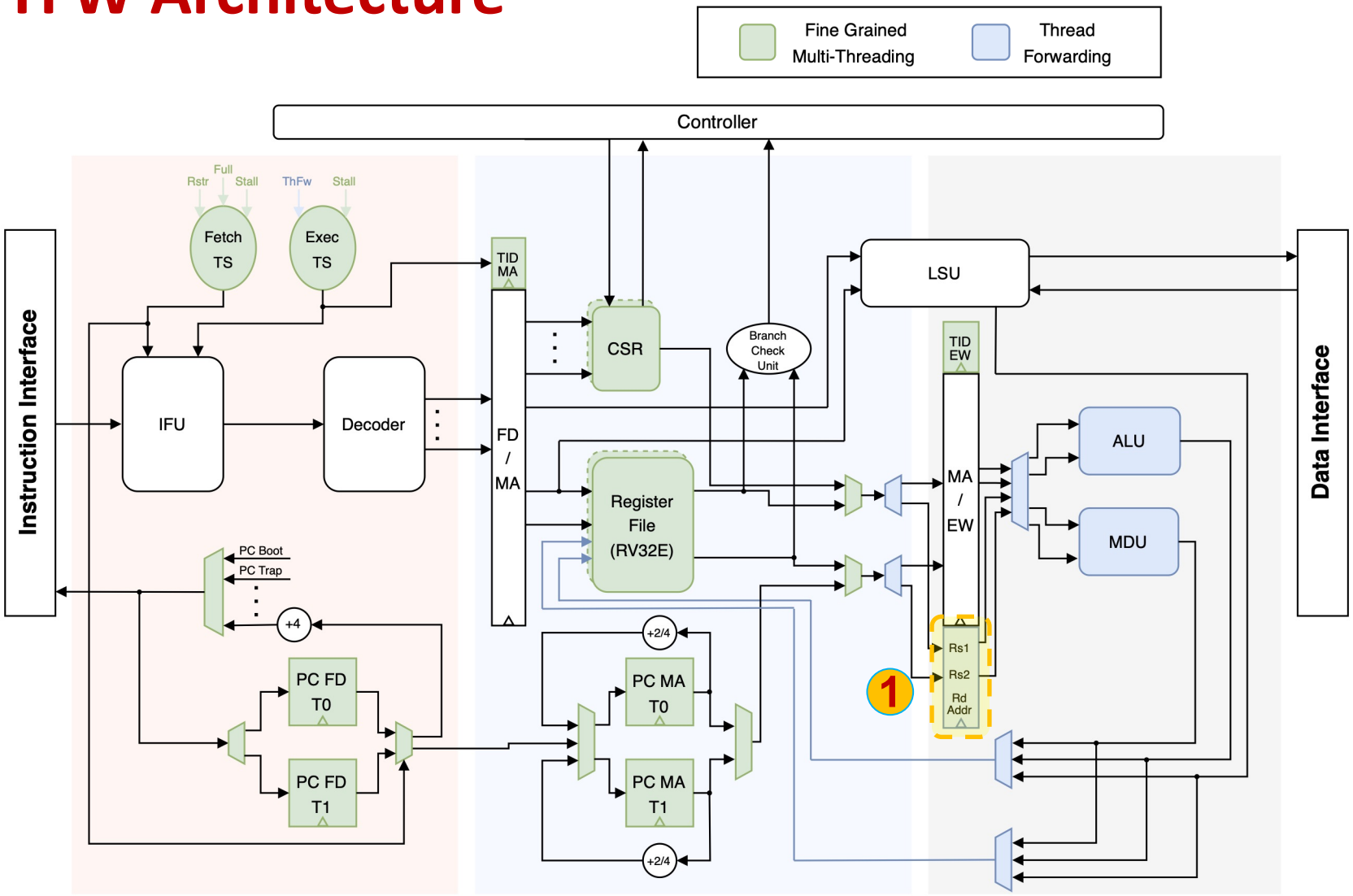

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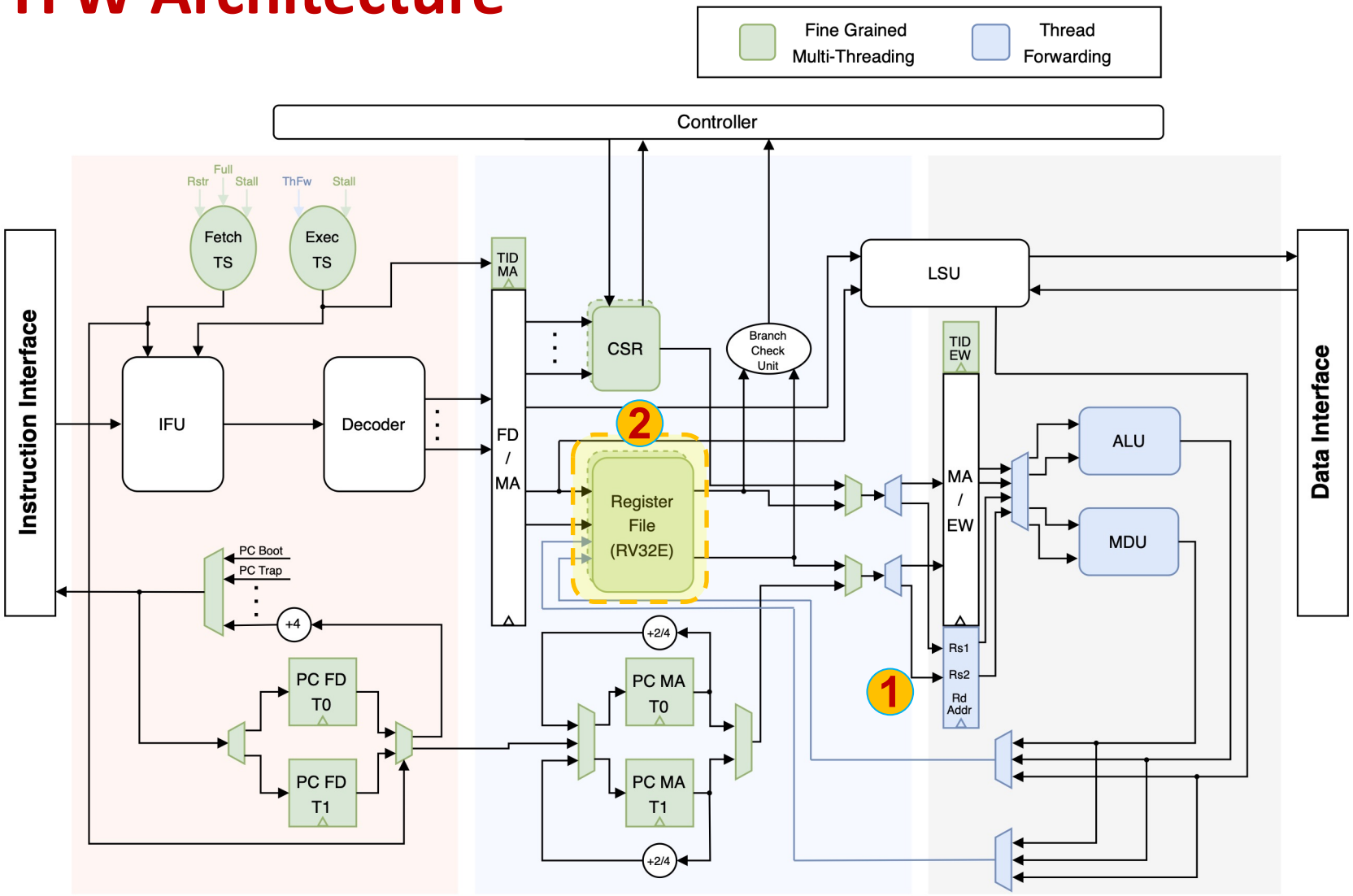

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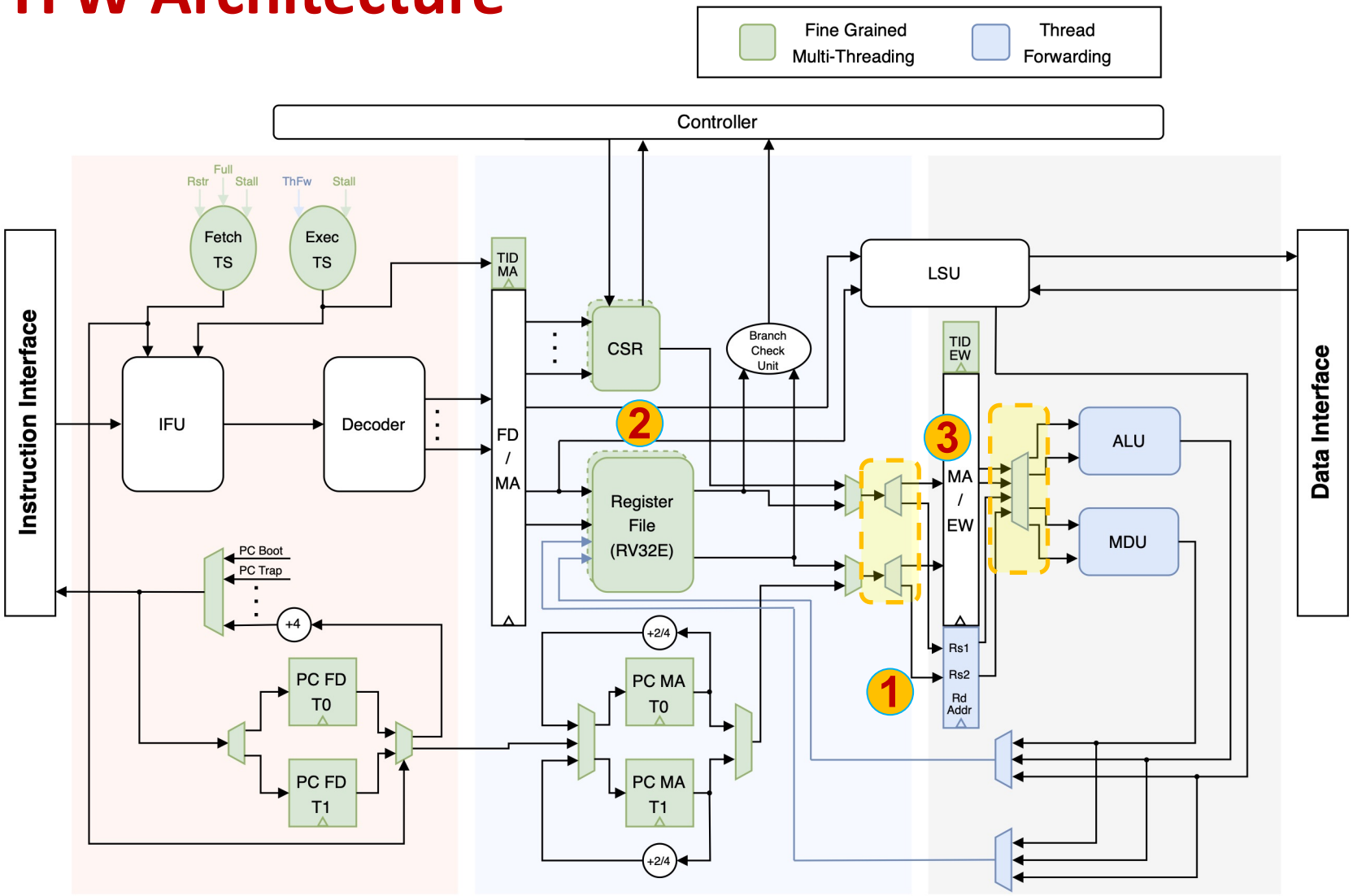

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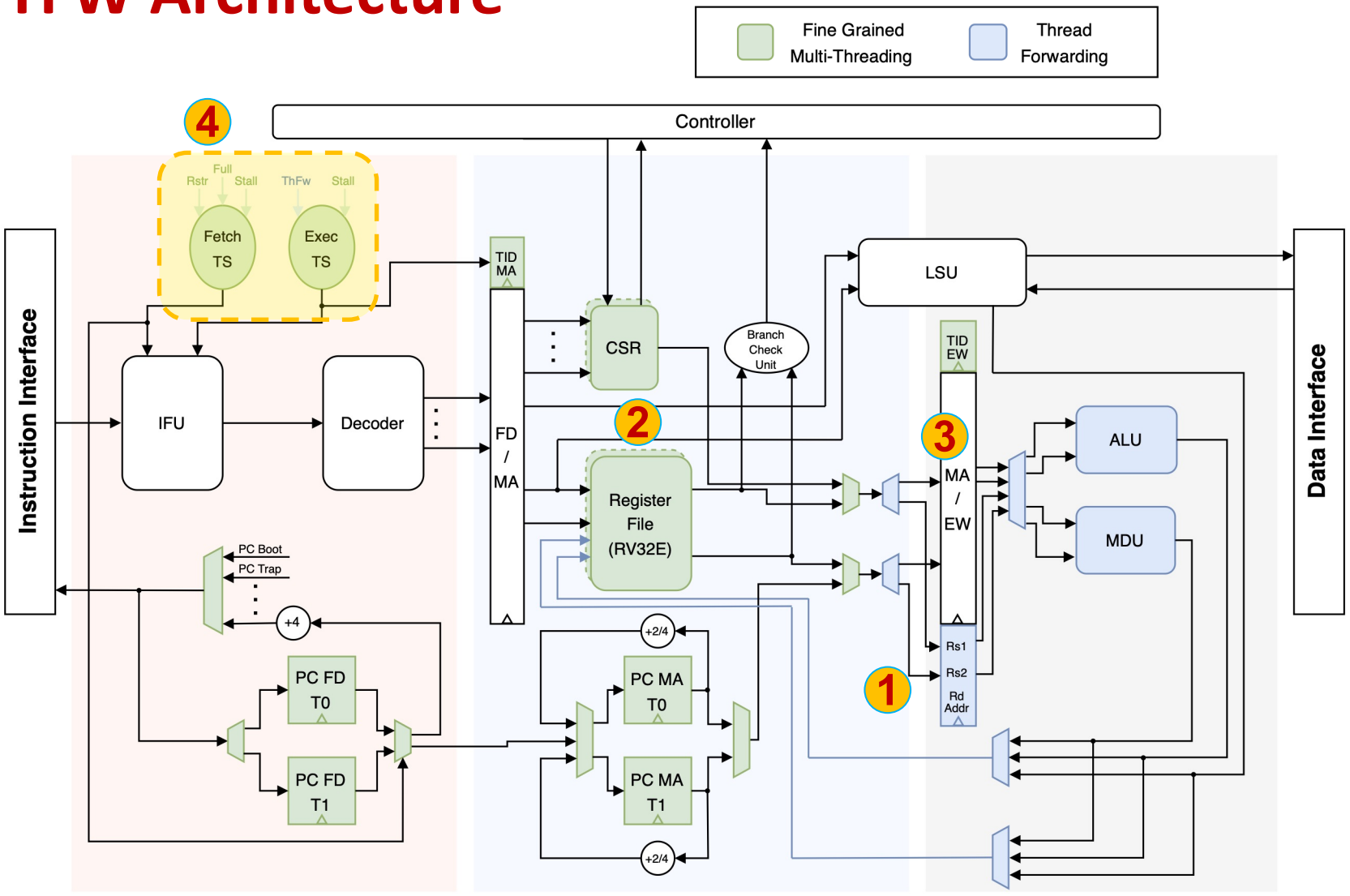

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Suspends interleaving during **multicycle instructions** to fetch consecutive instructions from the alternate thread.

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- **Tool:** DesignCompiler (Synopsys)
- **Frequency:** 300MHz
- **Tech:** C40
- **Corner**: SS, 1.05V, -40°C

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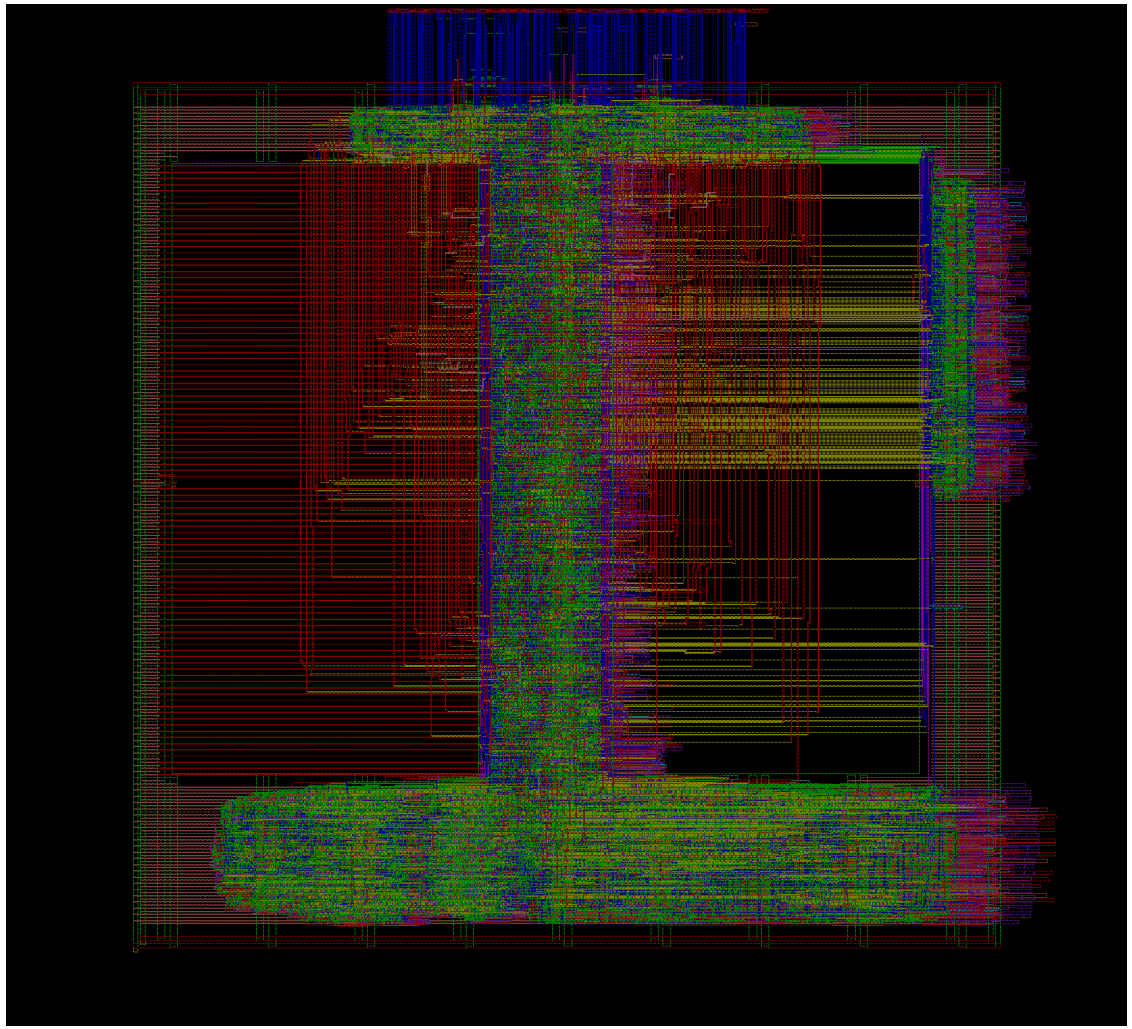

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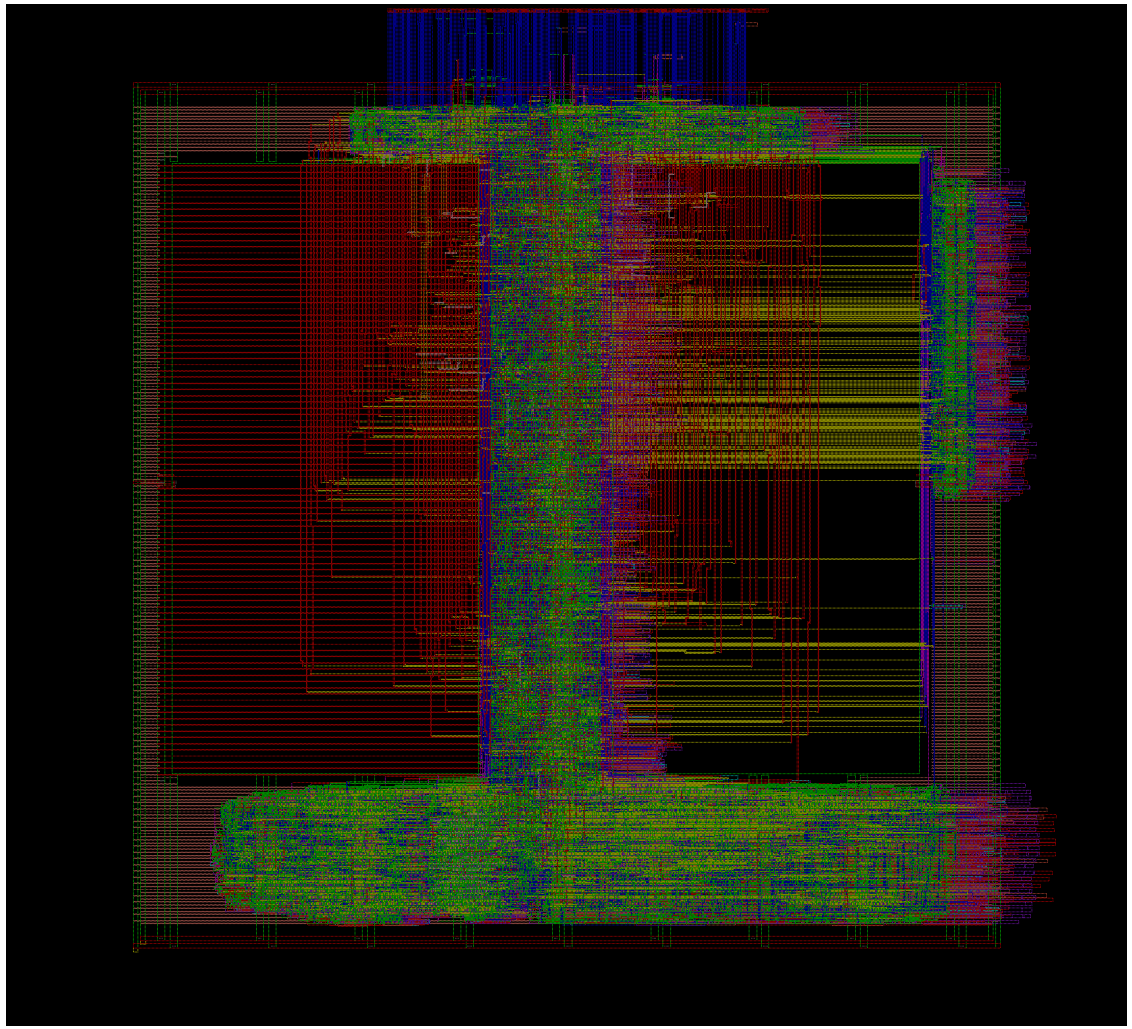

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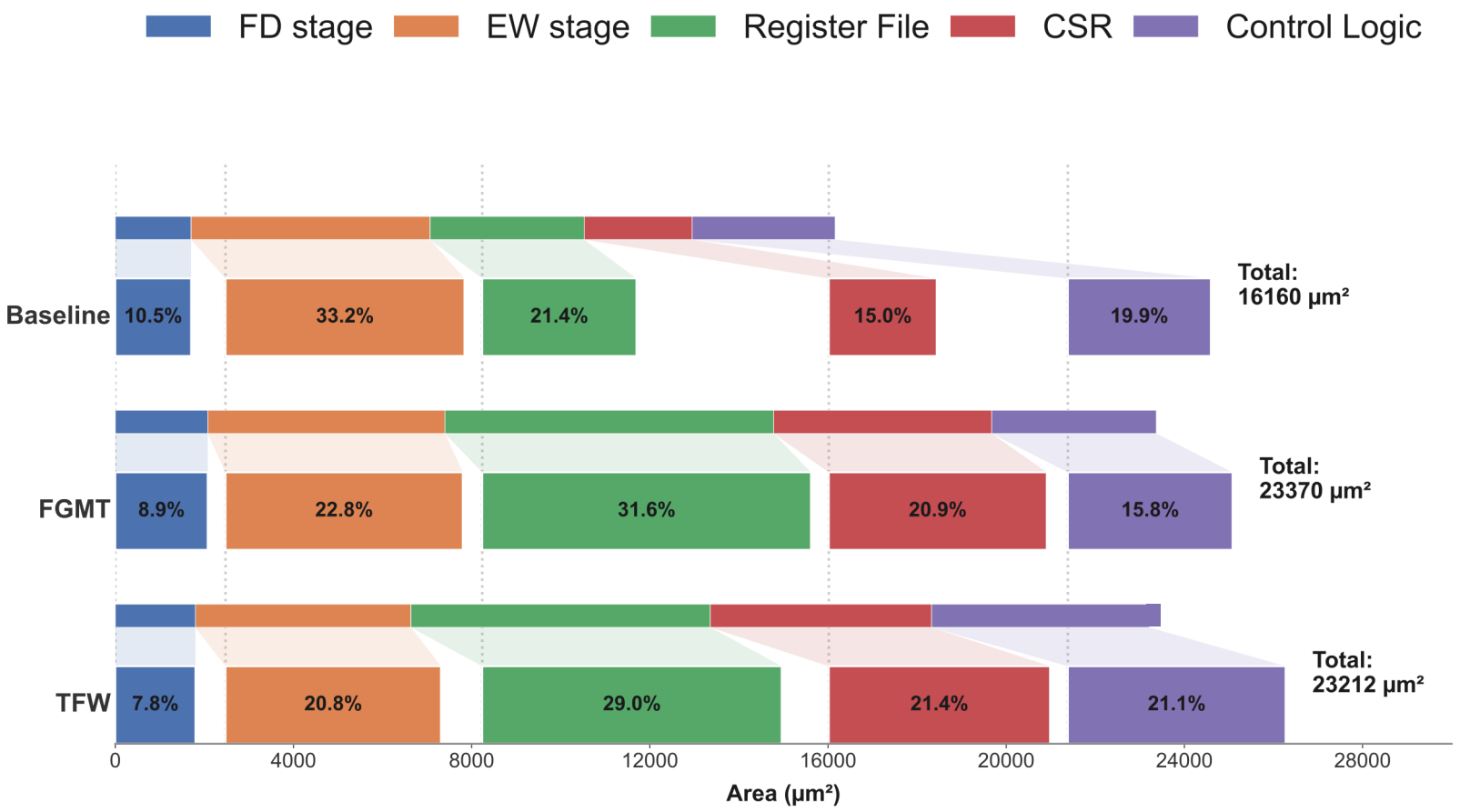

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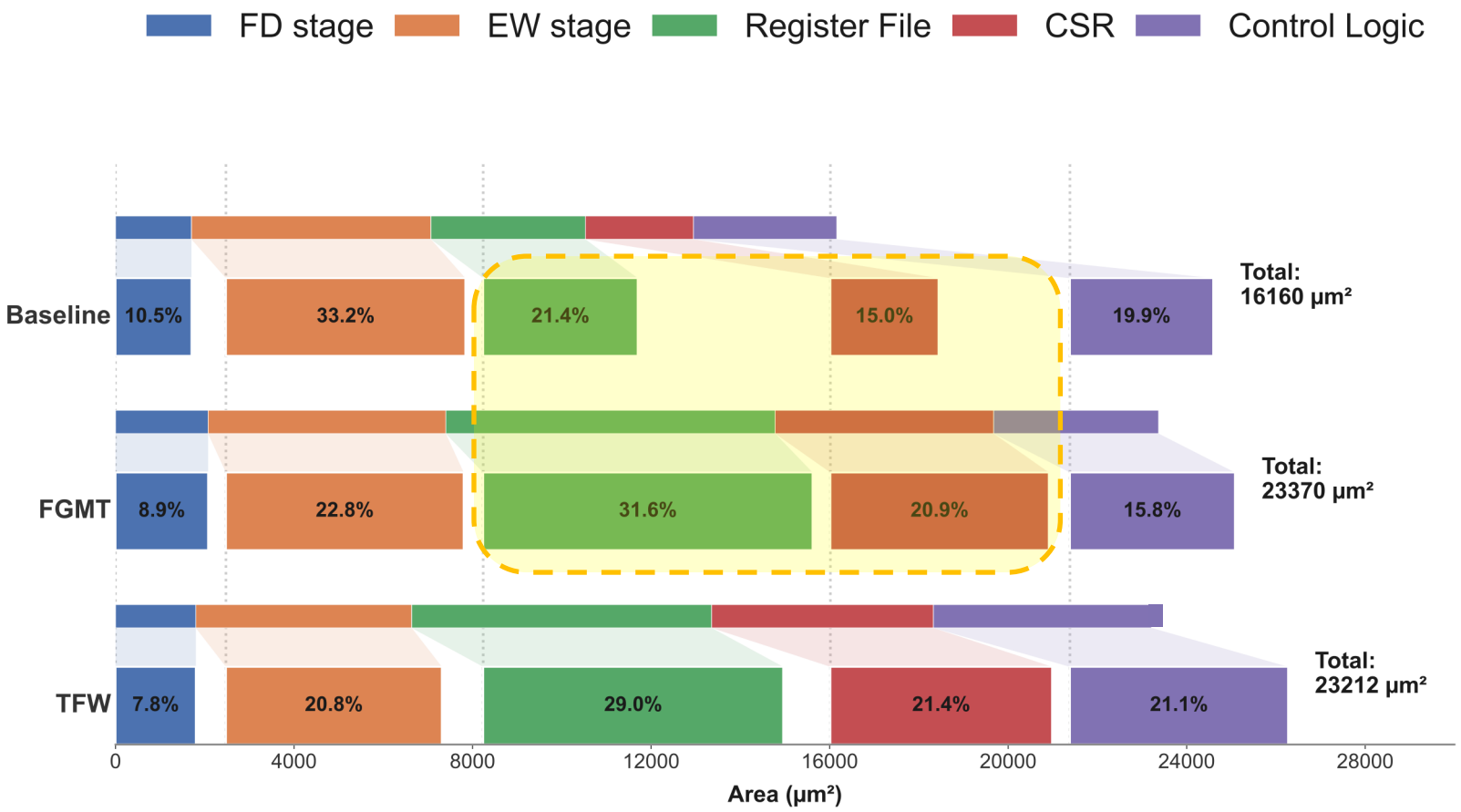

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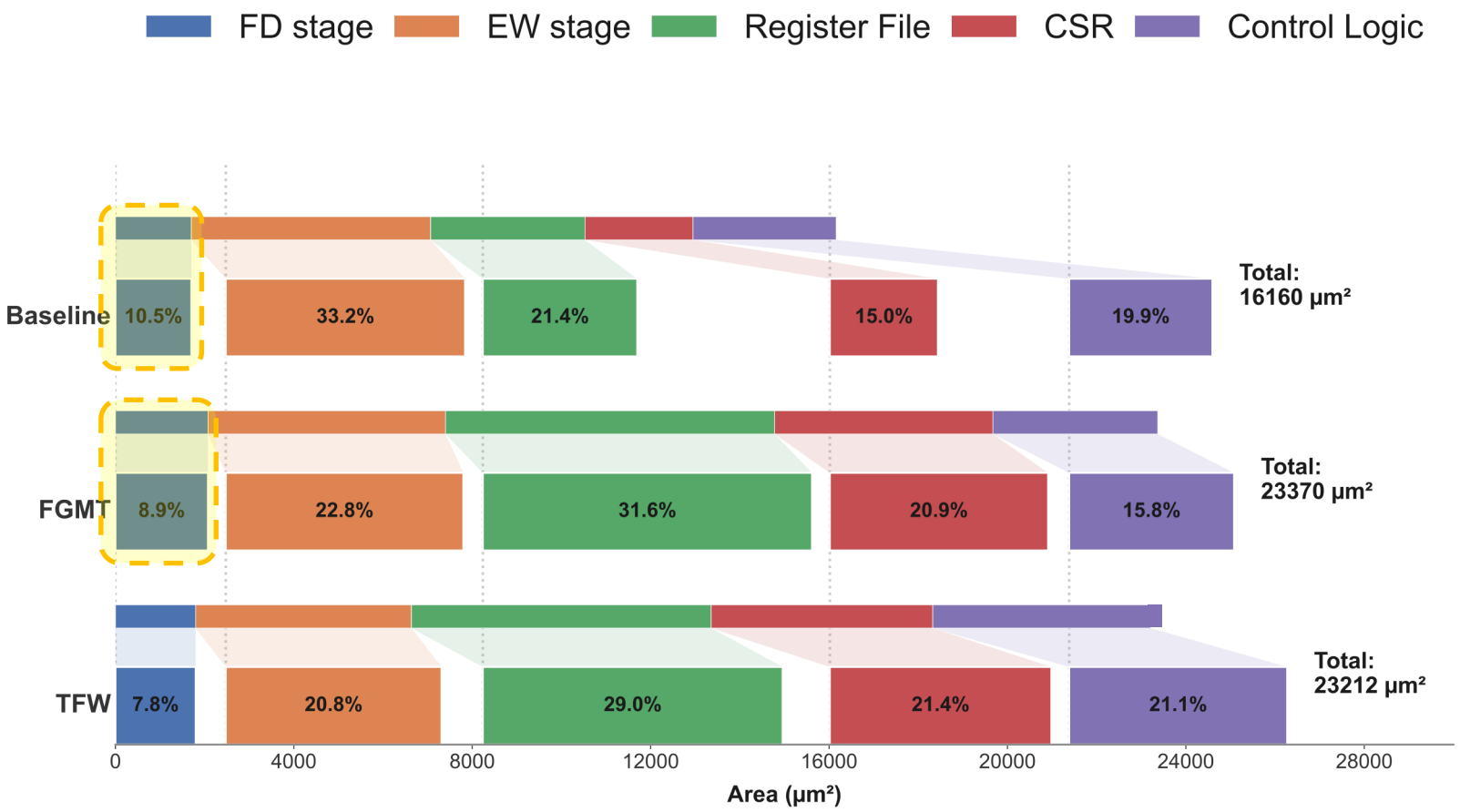

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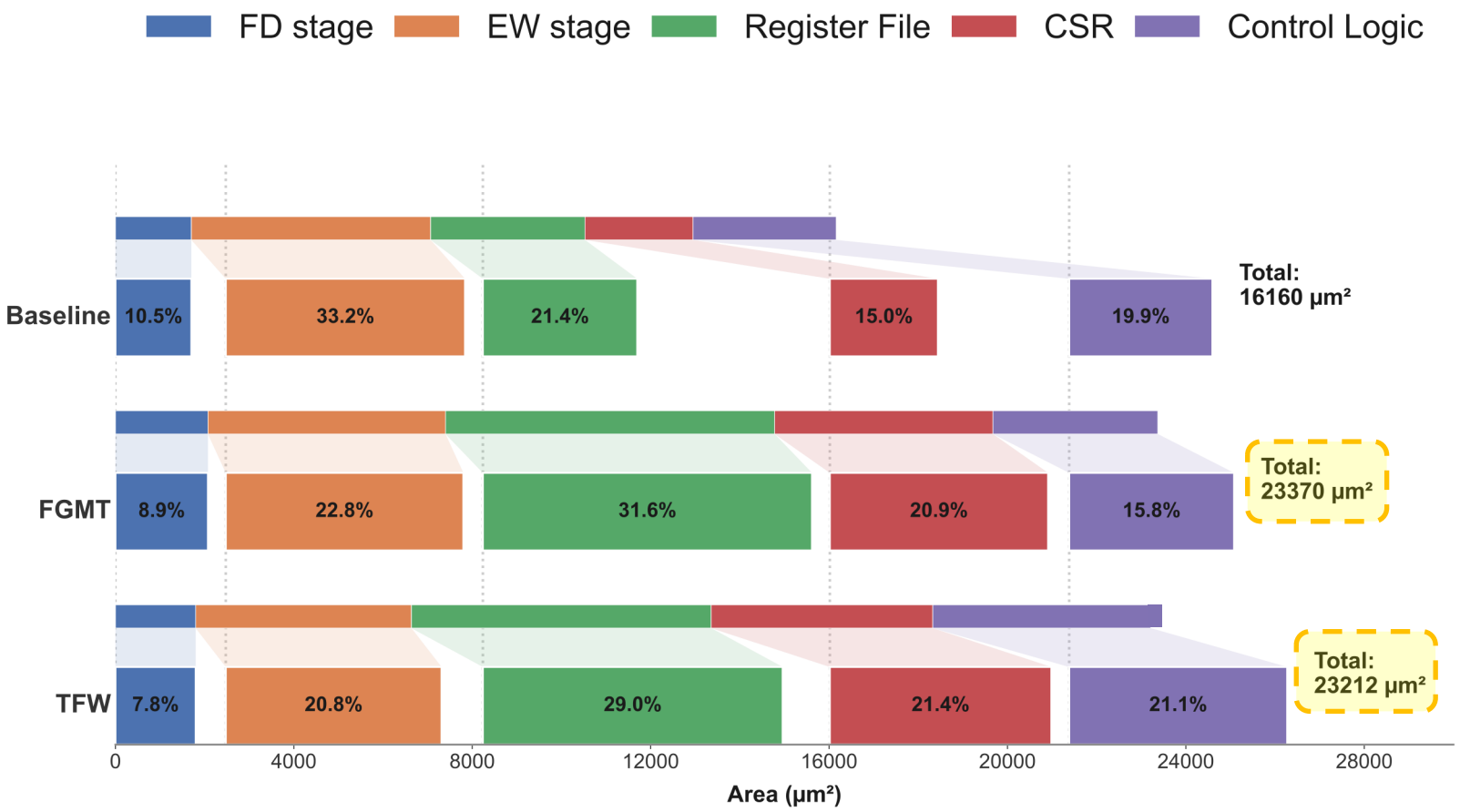

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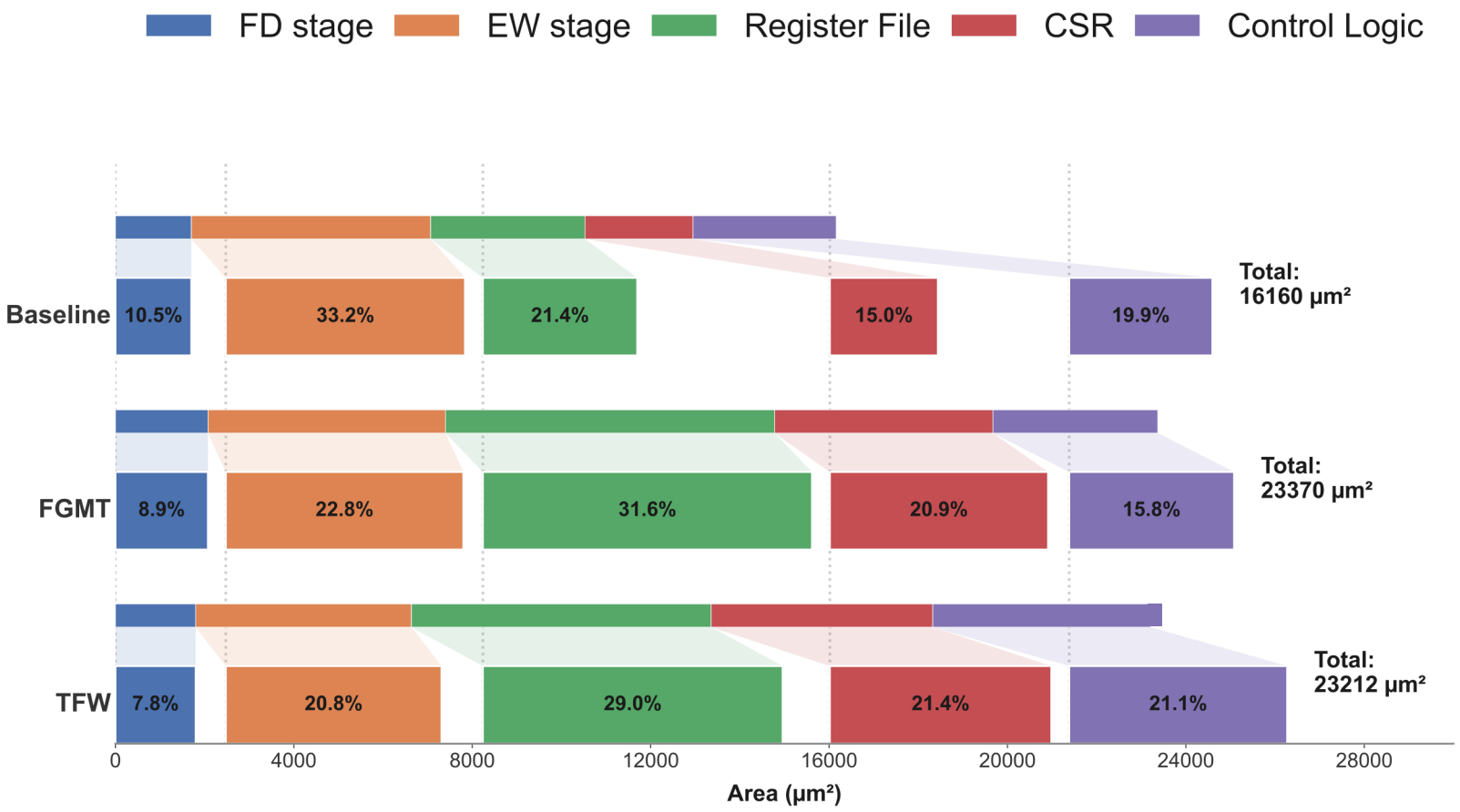

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- **Overhead** of:
  - Core level: +44%
  - **SoC level: +9%**

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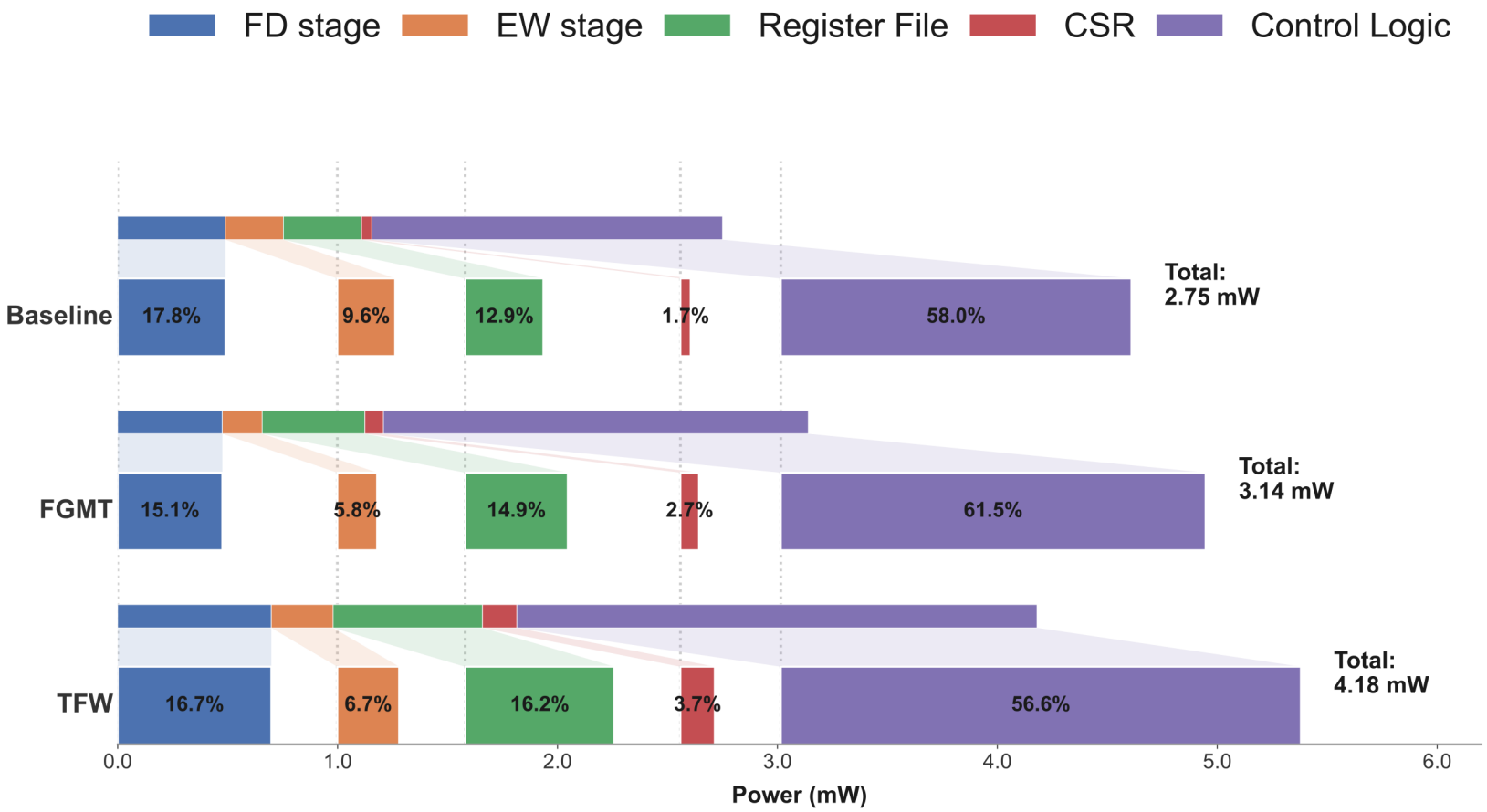

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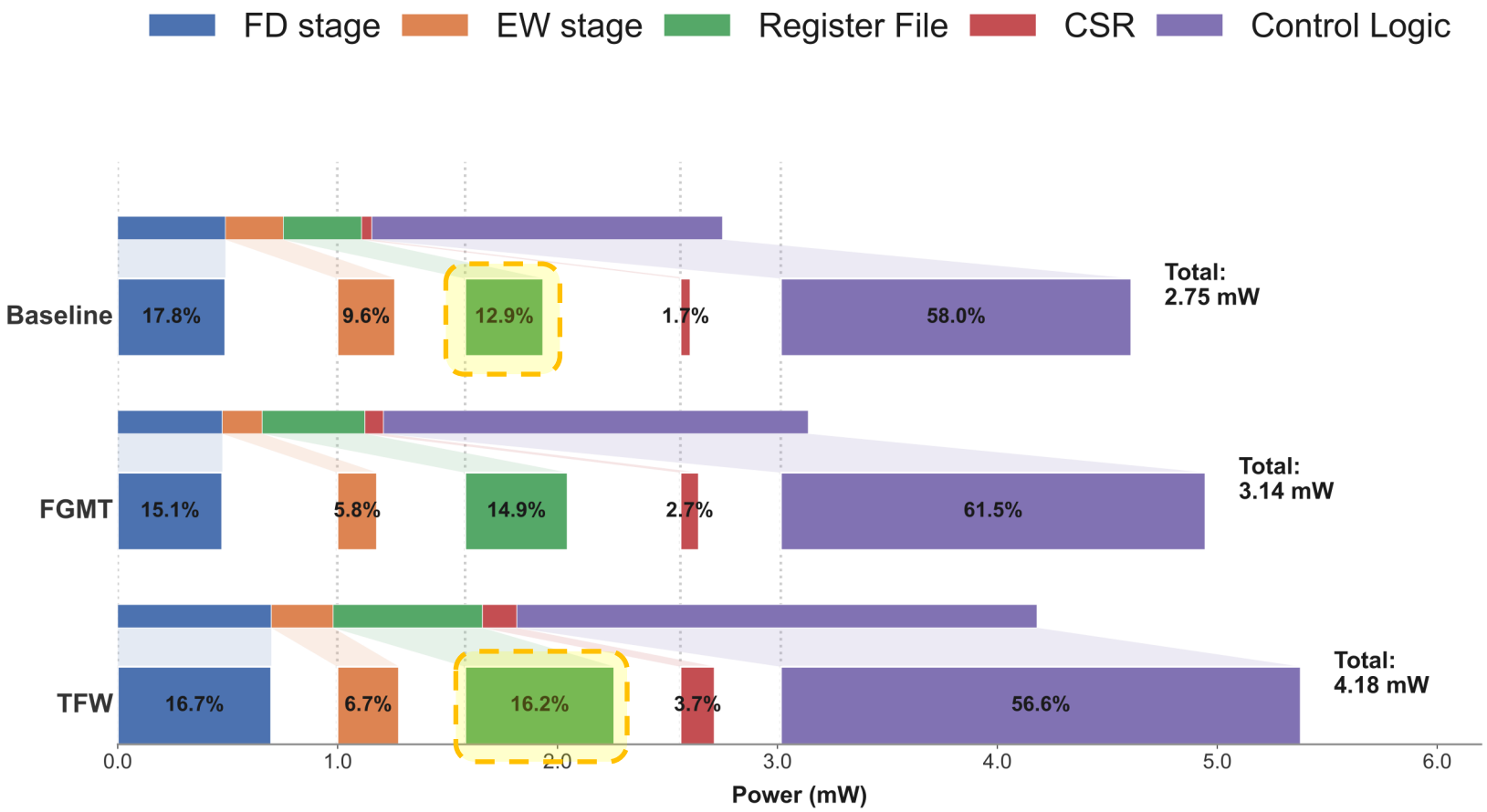

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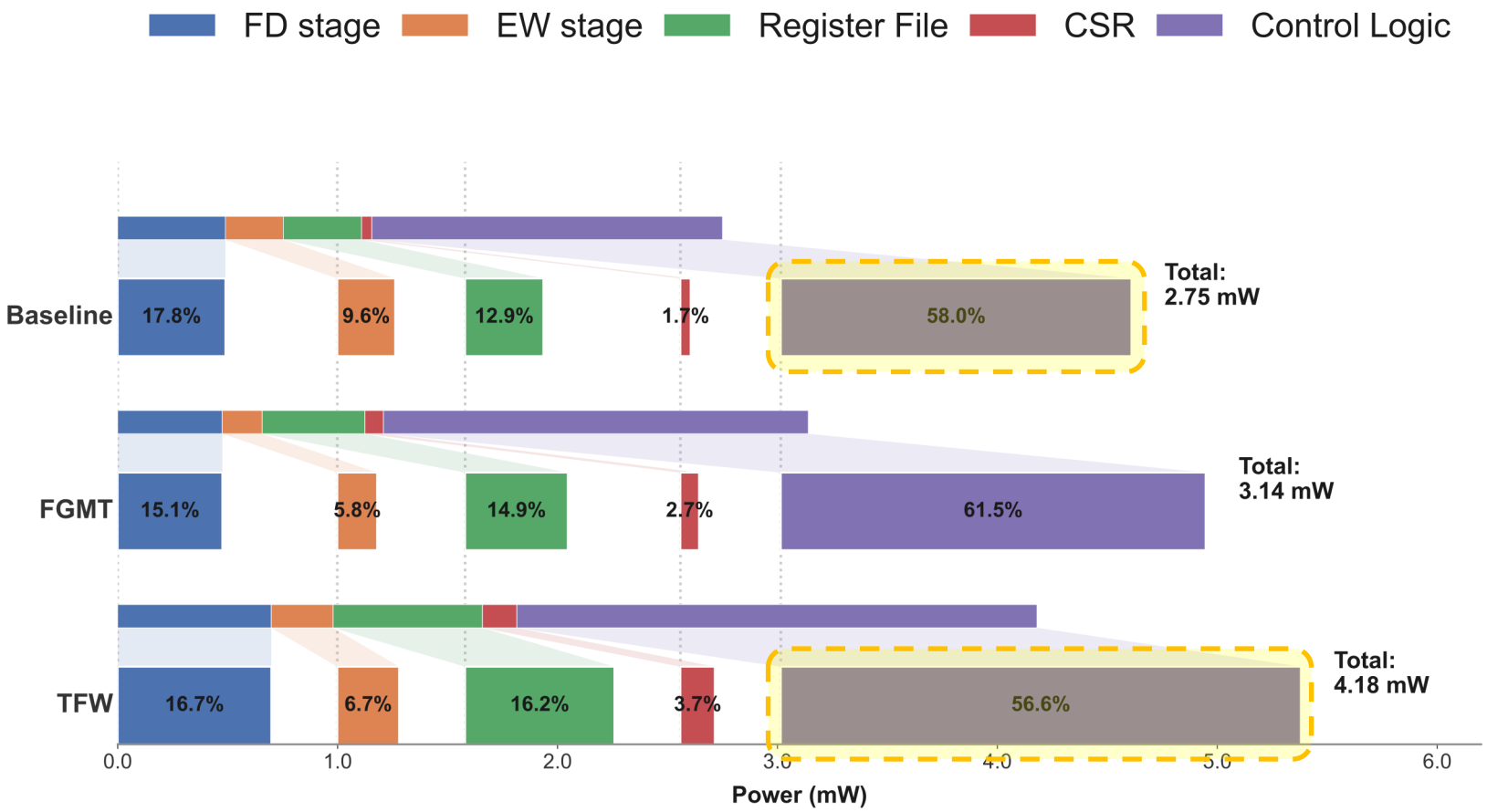

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  - *Higher* ***concurrent utilization*** *of functional units*
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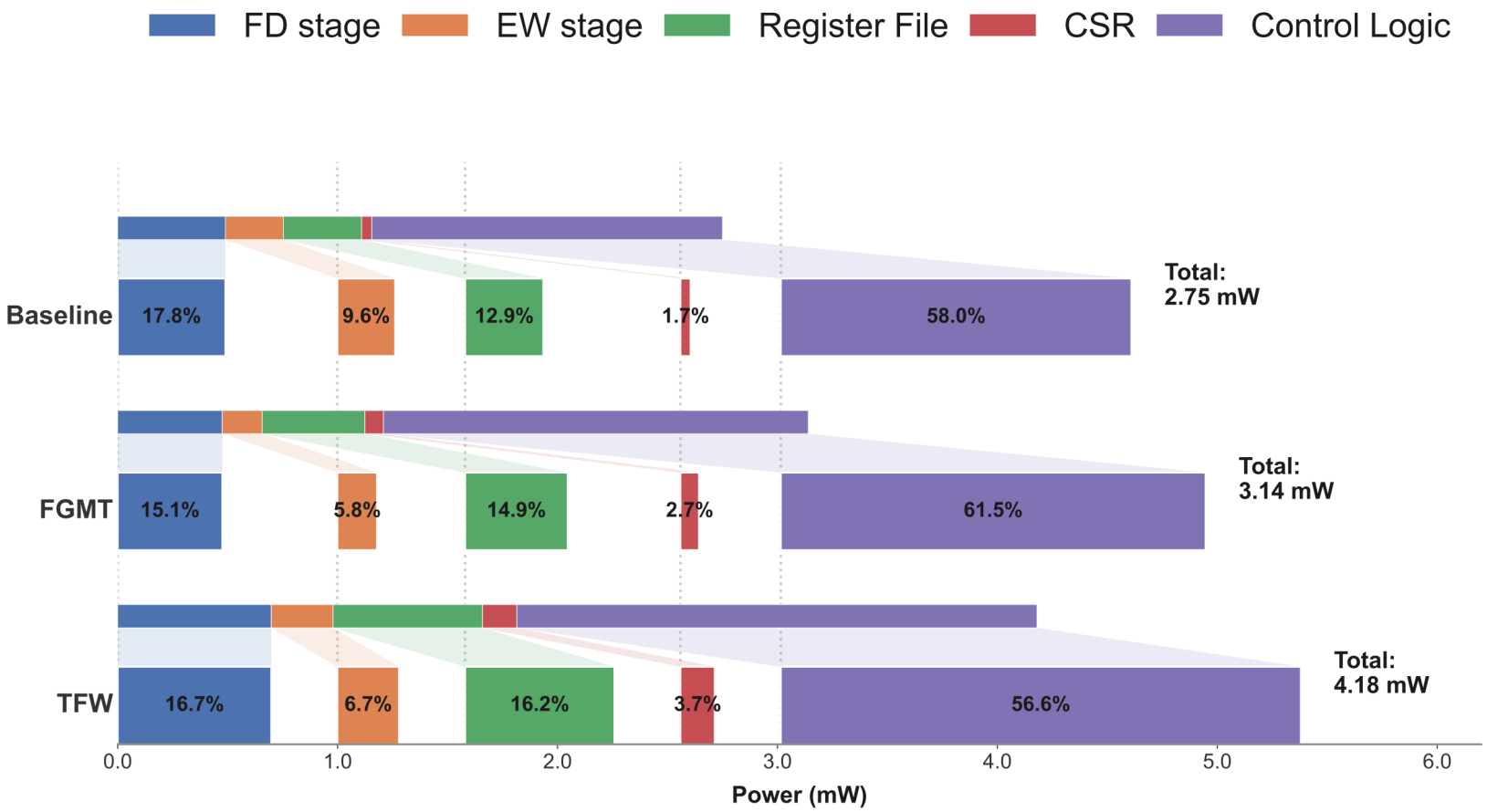

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  - ***Duplicated*** *RF and CSR*
- **TFW Power**
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- Overall **overhead** of:
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  - **TFW → +8%**

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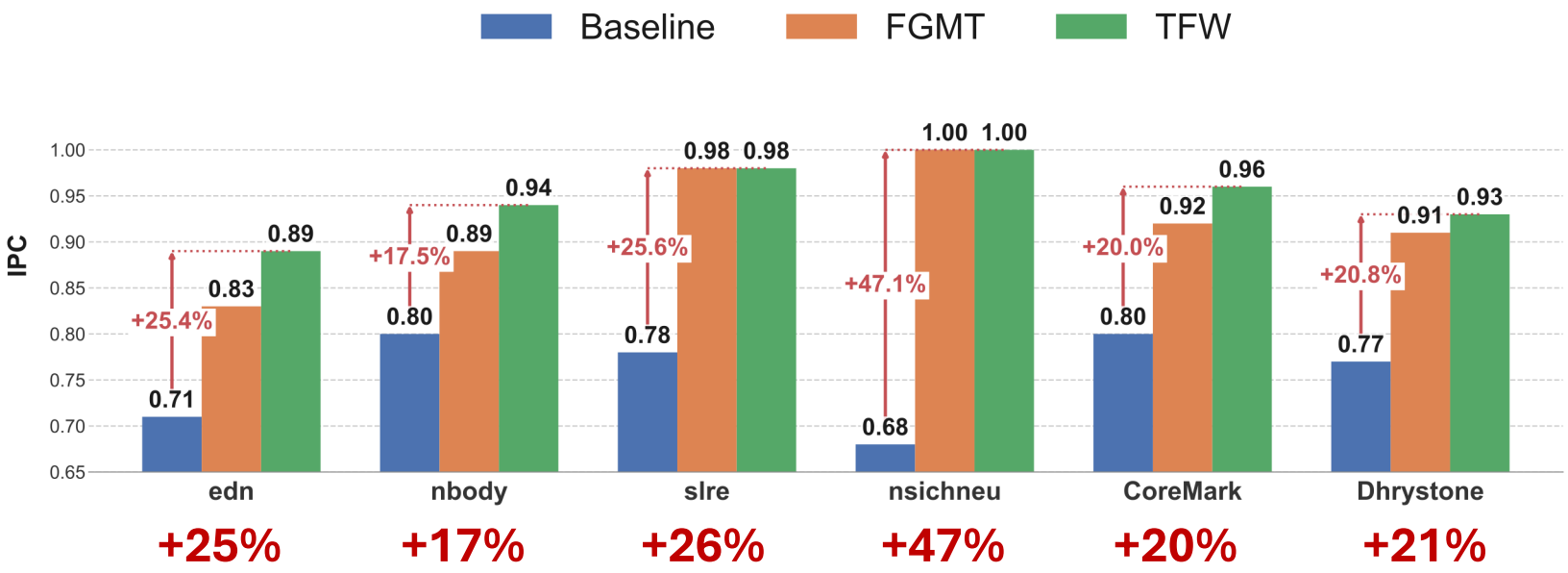

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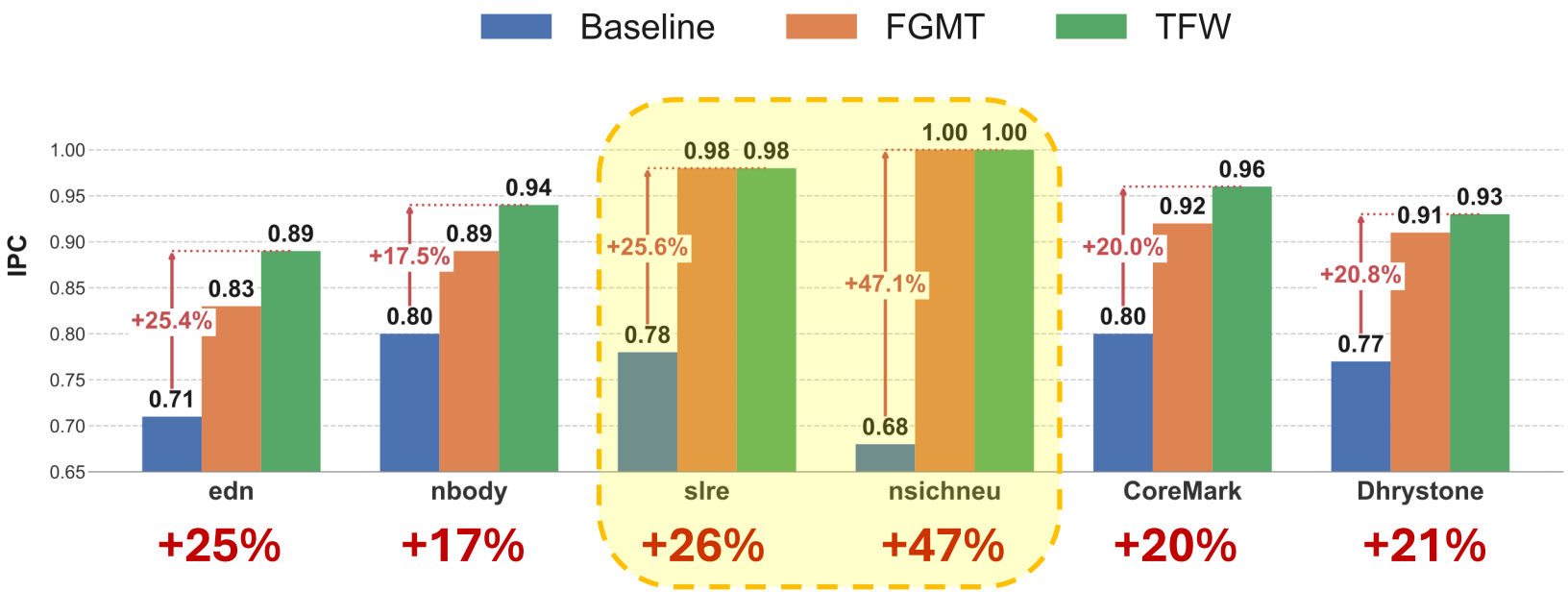

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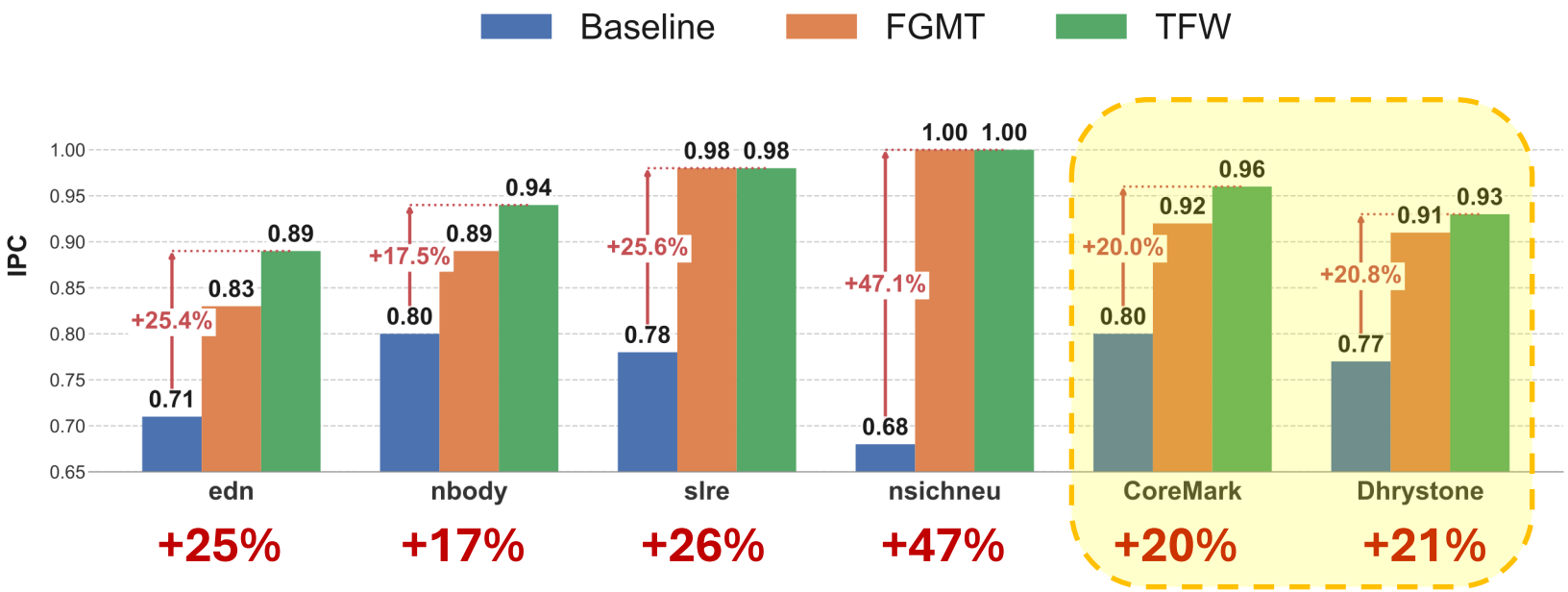

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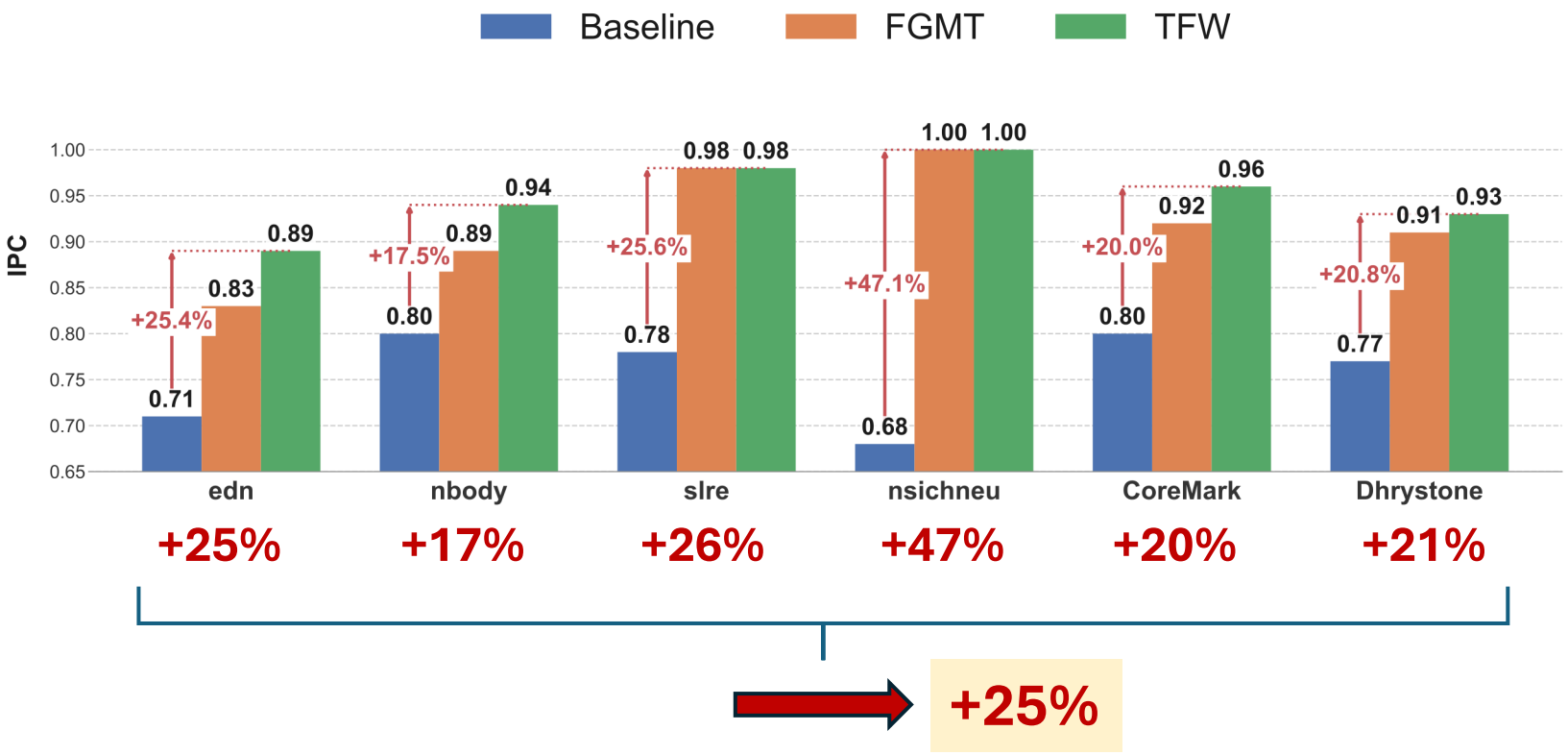
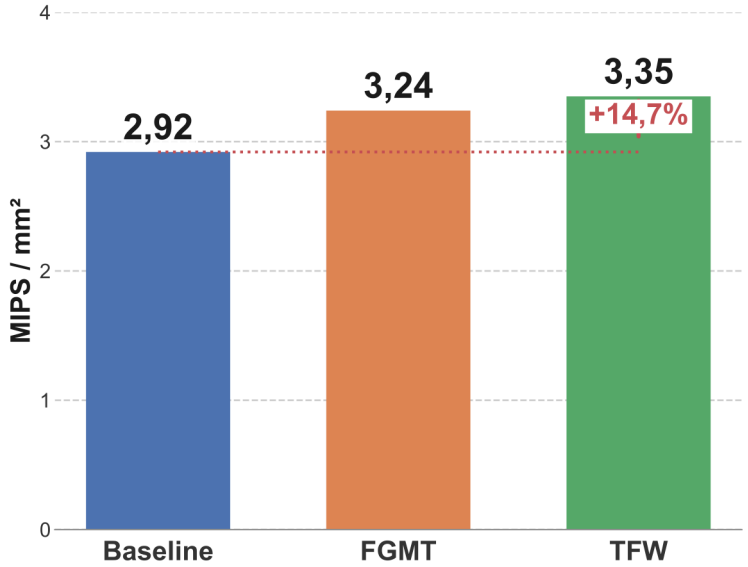


- Most improvement in **control heavy** workloads
- Robust improvement in more **comprehensive workloads**
- Mean uplift of **+25%**

Efficiency Metrics

Area Efficiency



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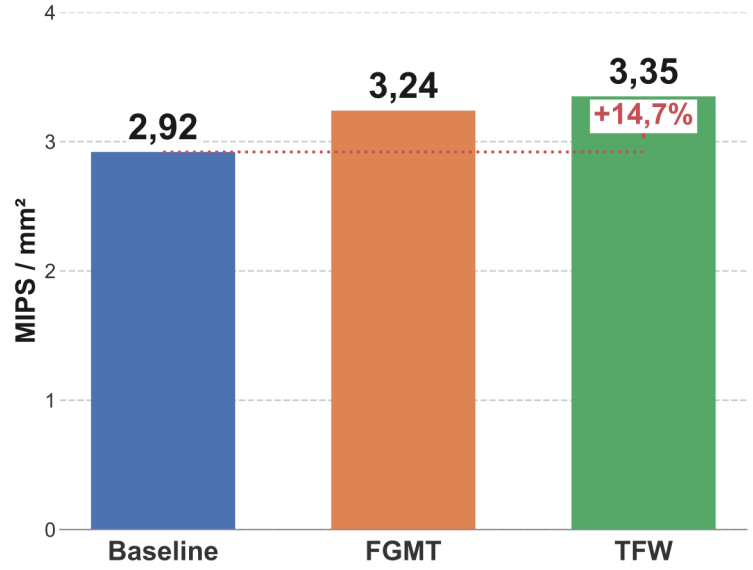

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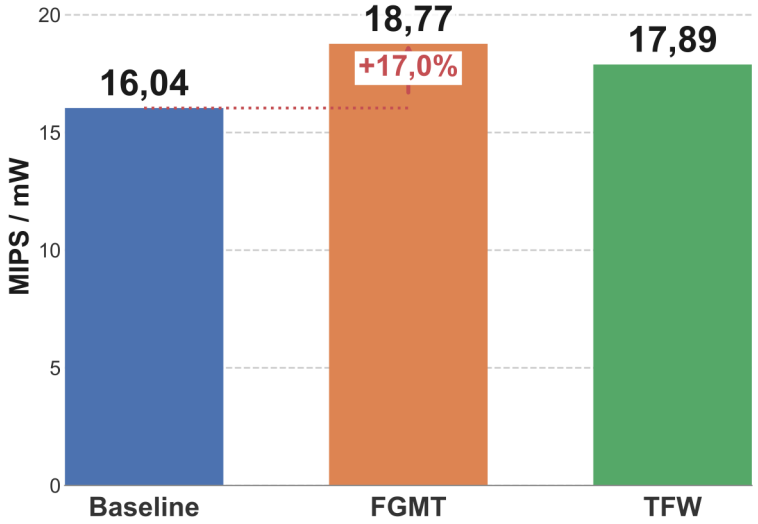

+17%

- **Trade-off:** **+21%** IPC vs. **+4%** SoC Power
- **Peak Model:** FGMT → **18.77 MIPS/mW (+17.0%)**
- **TFW Note:** Drops to +11.6% due to concurrent execution power

Temporal Predictability

Structural Masking of Control Hazards

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Elimination of Variable Flush Penalties

Removes **data-dependent** pipeline **flushes**:

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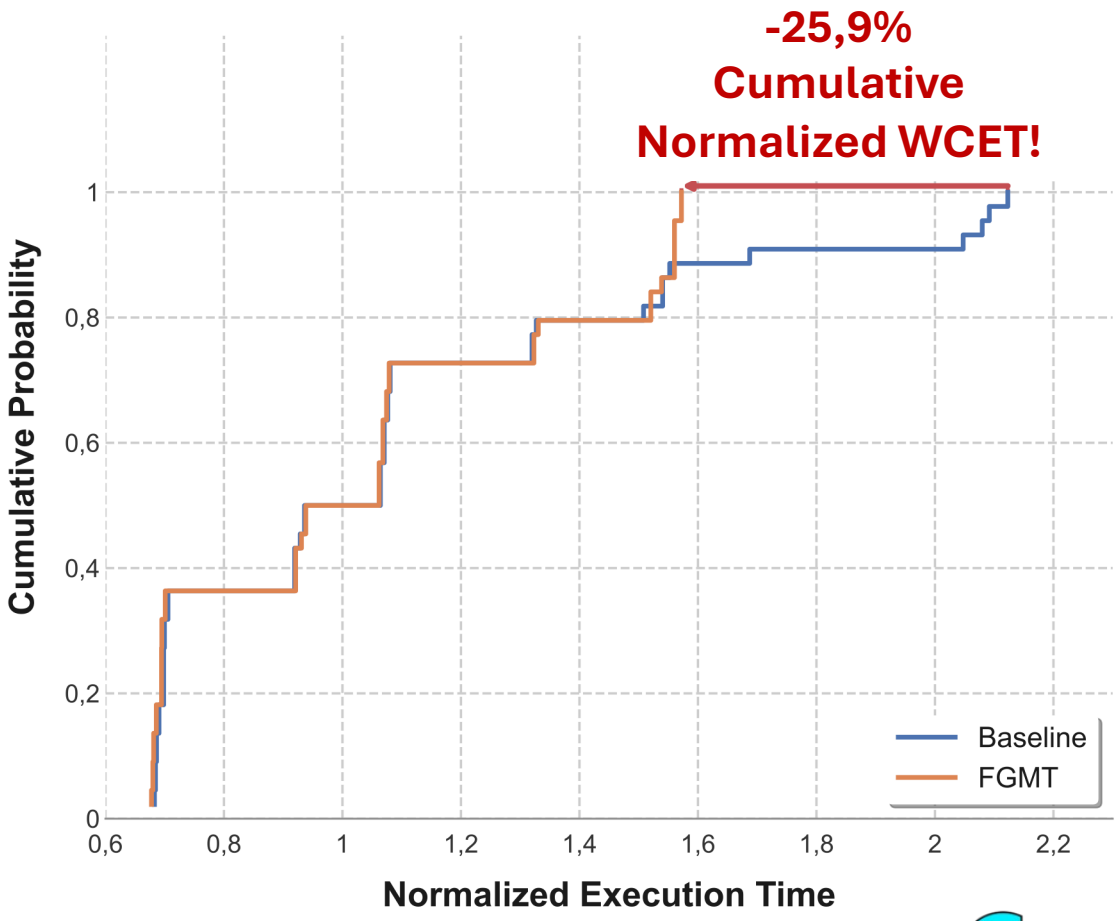

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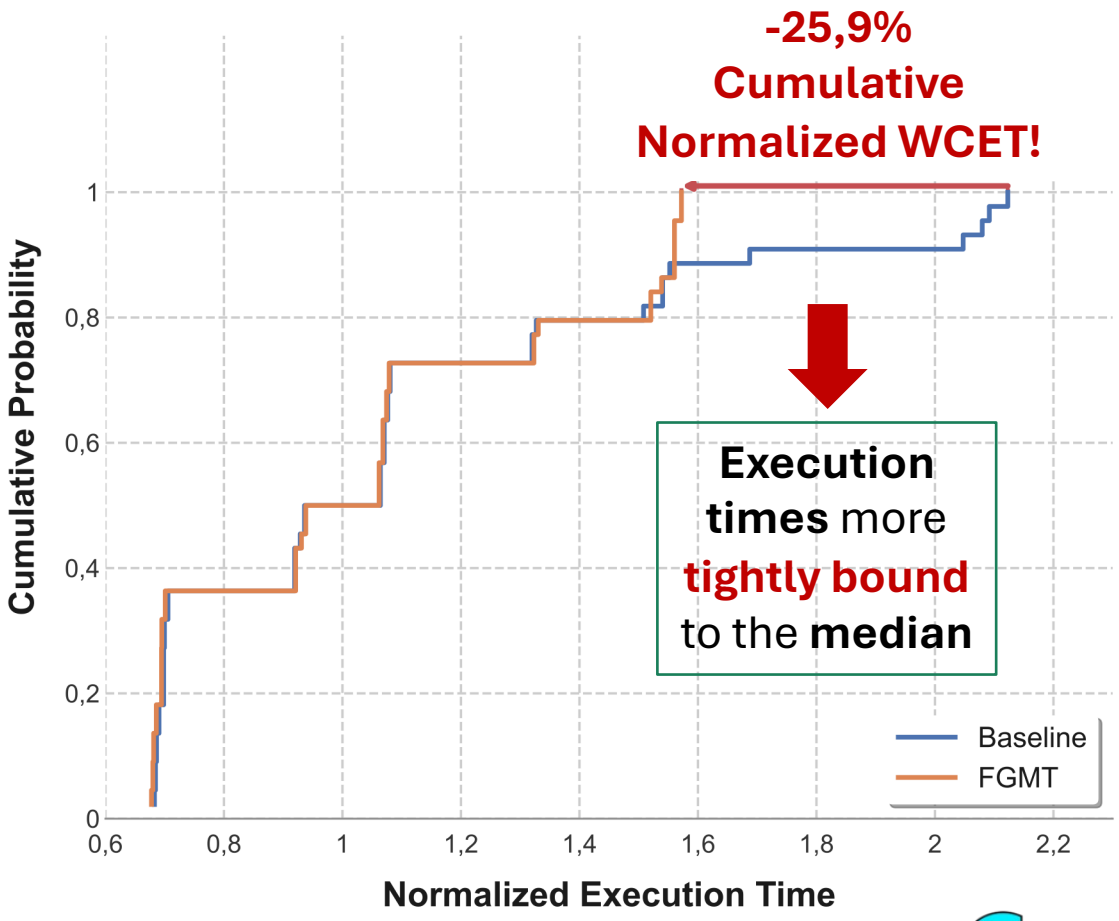

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- **Enhanced System Efficiency:** The architecture achieves **+14.7% area efficiency** (MIPS/mm^2) and up to **+17% energy efficiency** (MIPS/mW).


Thank you!
Questions?