Special Session on RISC-V and open source hardware

Part1 - 11:00-12:30

- **Frank Gürkaynak (ETHZ)**
  - This talk ☺
- **Yvan Tortorella (UniBo)**
  - Redundancy schemes for PULP systems
- **Michael Rogenmoser (ETHZ)**
  - Practical implementations and cooperations for reliable architectures using open source hardware
- **Markus Ulbricht (IHP)**
  - Building a Resilient and Dependable RISC-V System

Part 2 - 14:00-15:30

- **Ilia Polian (U. Stuttgart)**
  - System-level Fuzzed Testing for RISC-V
- **Carles Hernandez (UPV)**
  - SELENE: A RISC-V Platform for safety-related Applications
- **Nele Mentens (U. Leiden)**
  - RISC-V for Security Applications

Supported by FRACTAL project

https://fractal-project.eu/

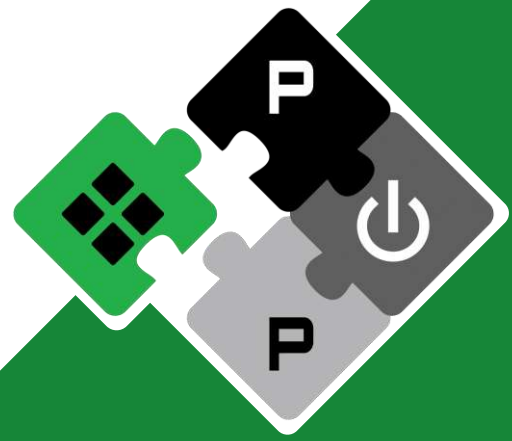
This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 877056. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Italy, Austria, Germany, Finland, Switzerland.

ETH zürich ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

The first 10 years of PULP Platform and open source HW

Integrated Systems Laboratory (ETH Zürich)

Frank K. Gürkaynak kgf@iis.ee.ethz.ch



@pulp_platform

pulp-platform.org

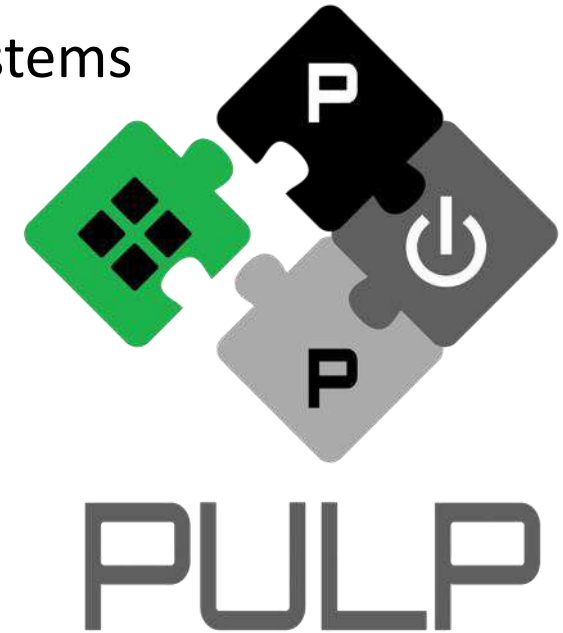
youtube.com/pulp_platform

PULP Platform

Open Source Hardware, the way it should be!

We started almost excatly 10 years ago (April 2013)

- **Investigating new computing architectures**
  - Efficient over a wide range from IoT applications to HPC systems
- **Key points**
  - Parallel processing
  - Near threshold computing
  - Efficient switching between operating modes
  - Making best use of technology
  - Heterogeneous acceleration
- **Parallel Ultra Low-Power (PULP) platform was born**



You need a 'core' to build computer architectures

- **Initially we did not want to design our own processors**
  - Wanted to use available processors (ARC, ARM..)
  - It proved difficult to design systems that we could share with our collaborators
- **Then we used OpenRISC cores (2013-2015)**
  - We had to completely redesign and optimize these cores
- **We moved to RISC-V starting in 2015**
  - Adapted the decoder of our optimized OpenRISC core
  - Make use of a growing SW development environment
  - ETH is one of the founding members of the RISC-V foundation

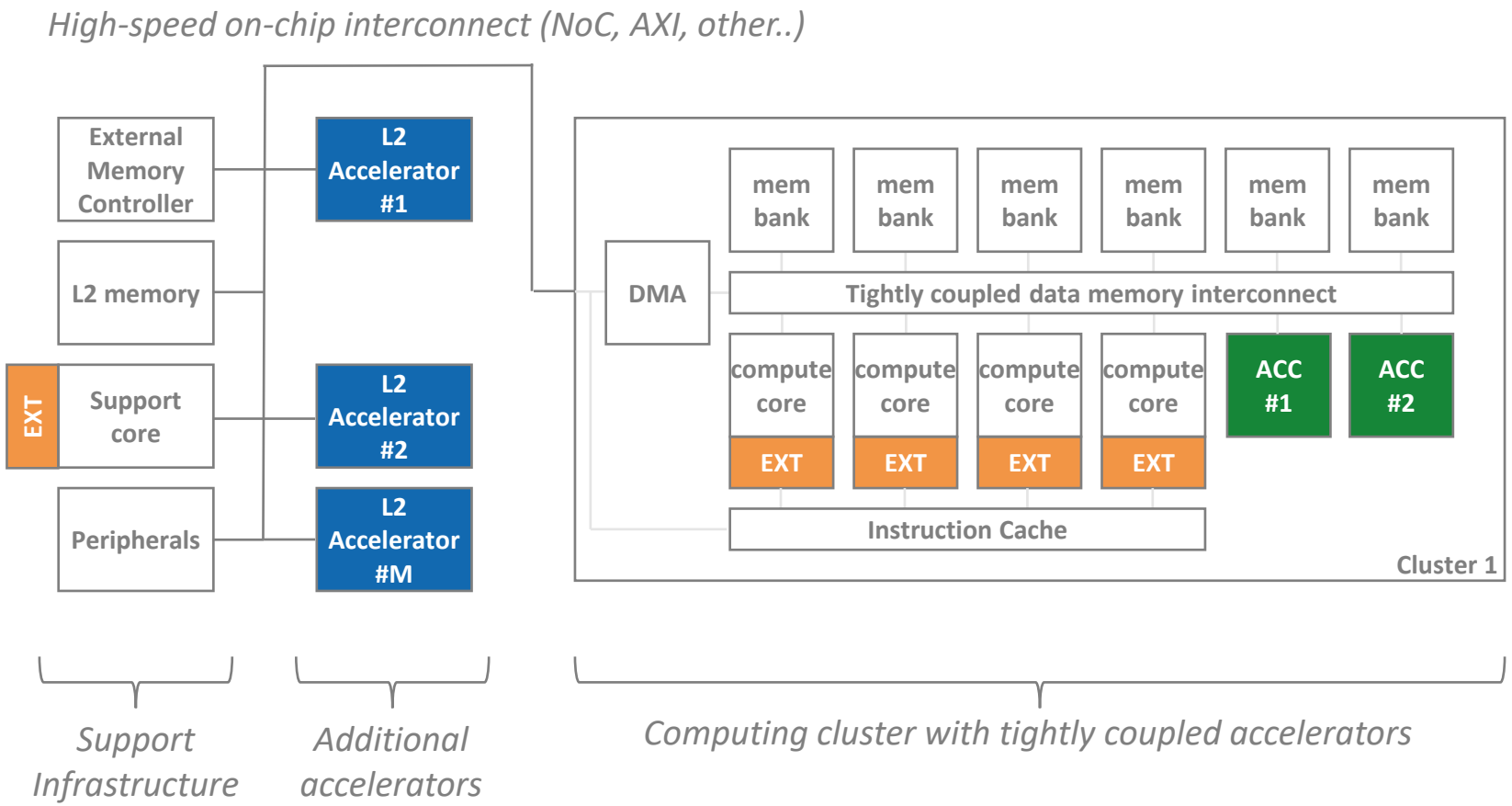
Our research focus: cluster-based many-core accelerators

Innovation factors

Extensions to processor cores
- Explore new extensions
- Efficient implementations

Shared-memory Accelerators
- Domain specific
- Local memory

Multiple computing clusters
- Communication
- Synchronization

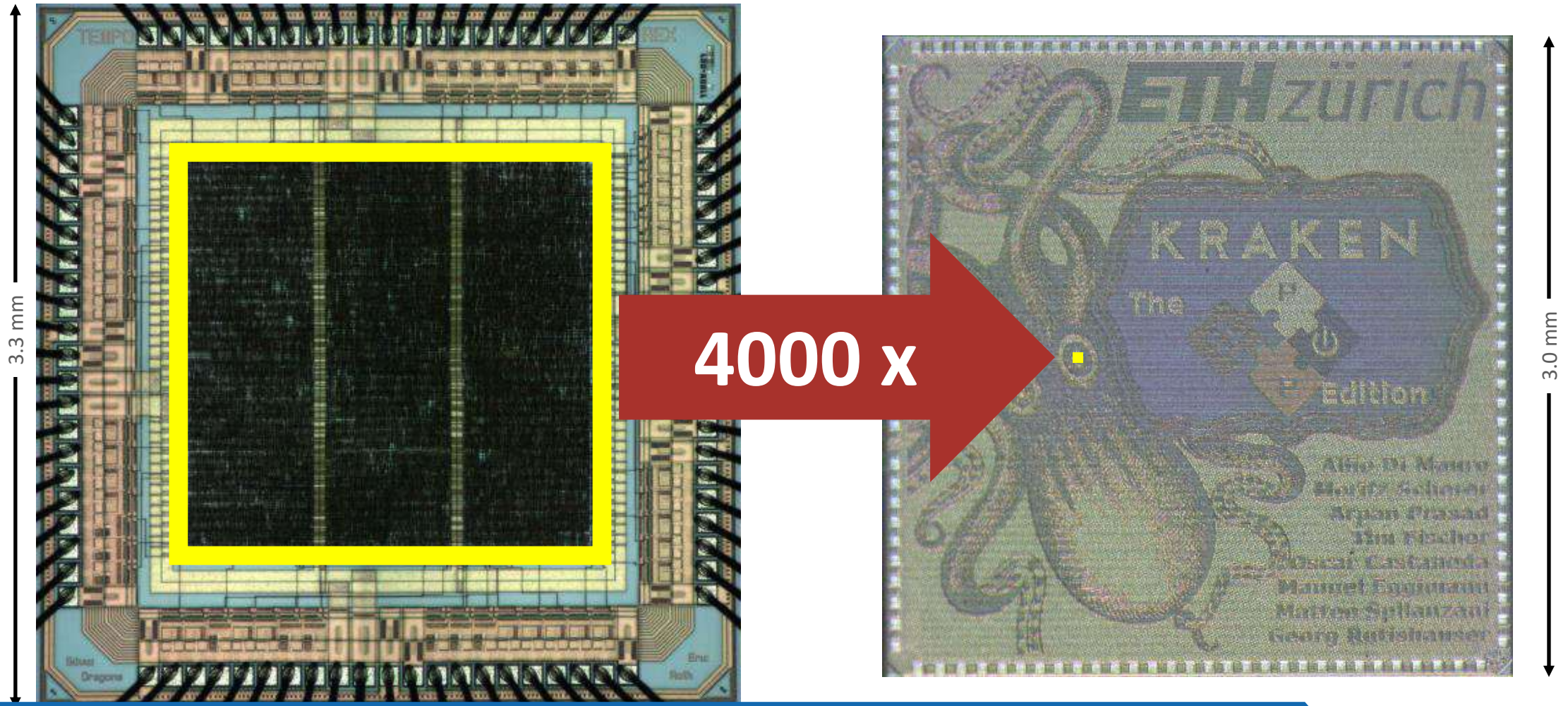


Today the PULP team has grown to more than 70 people

- **Headed by Luca Benini**
- **Teams in both ETH Zürich and University of Bologna**

... and Bianca the Bear

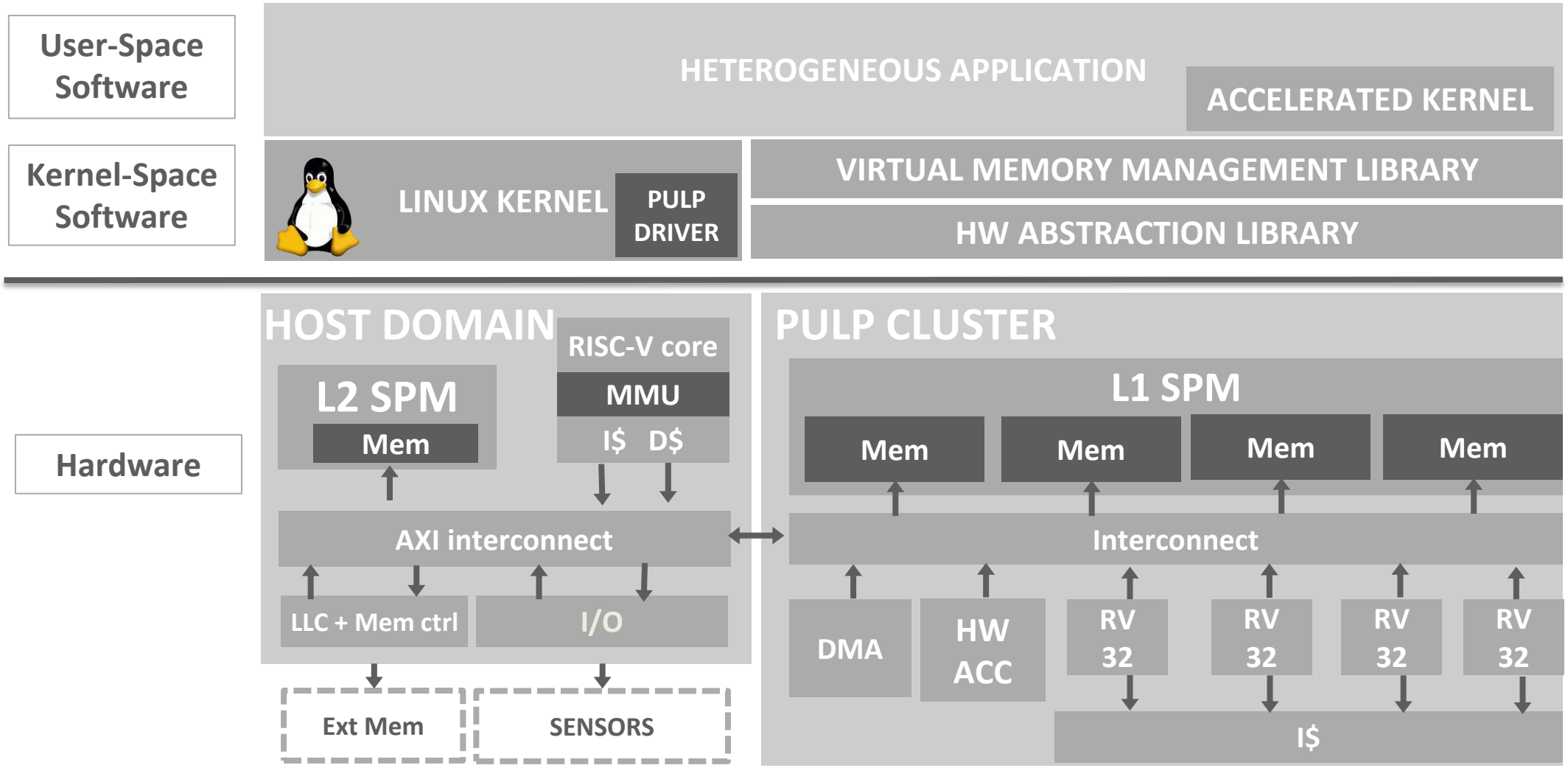
In the last 20 years IC Design has changed a lot



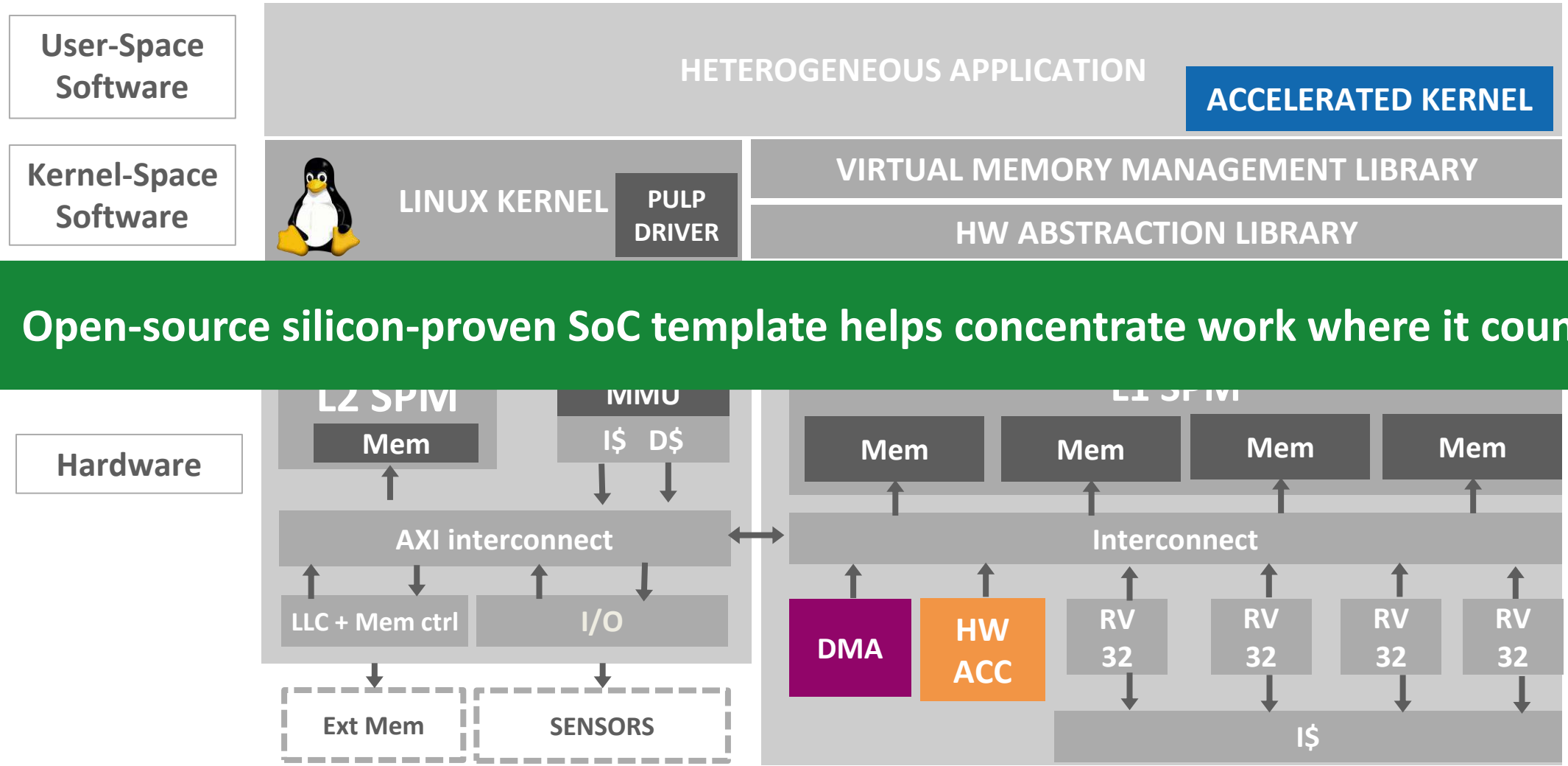
80 MGE

What used to be a complete chip is now a small part of a SoC !

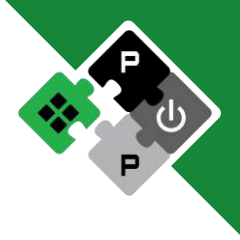
There is so much that makes up a modern SoC



In a typical design, innovation is only in a limited scope



For us open source is a necessity to manage our projects!



- **Modern IC design is complex and expensive**
  - We need partners to help and collaborate
  - We need support (IPs, donations) to realize designs

Open Source to the rescue

- **Makes it easy to collaborate with external partners (both industrial and academic)**
  - Less paperwork/NDAs to get started
  - Partners see/are aware of what we provide
- **What we do can be re-used (permissive licensing) by our partners**
- **Results can be more easily verified**

RISC-V has been a game changer for computer research

- **RISC-V Foundation established in 2015**
  - ETH Zürich is a founding member
  - More than 3’000 members
  - Headquarters in Zurich
- **Nice ISA design, patent troll safe, extensible**
  - Huge momentum
- **ISA is essentially a document**
  - Defines 32/64/128 bit architectures
  - What are the instructions, what effect do they have
- **ISA divided into several extensions**
  - Working groups decide and work on the definitions
  - Several are ratified, work continues on others

Name	Description
I	Integer
E	Integer with 16 registers
C	Compressed Instructions
M	Multiplication
F	IEEE 32b floating point
D	IEEE 64b floating point
Q	IEEE 128b floating point
A	Atomic instructions
V	Vector extensions
P	Packed SIMD extensions
B	Bit manipulation
…	and more

RISC-V is a game changer

It's the Software, stupid!

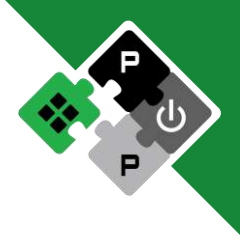
- Toolchains → GCC, LLVM
- System tools → Emulators: QEMU, TinyEMU, Spike, Renode
  Bootloaders: Coreboot, U-boot, BBL, OpenSBI
  BINUTILS, GDB, OpenOCD, Glibc, Musl, Newlib
- Language Runtimes → C, C++, Fortran, GO, Rust, Java, Ocaml,
- Operating Systems → Linux: Fedora, OpenSUSE, Gentoo,
  OpenEmbedded/Yocto, Buildroot, OpenWRT, FreeBSD
  FreeRTOS, Zephyr, RTEMS, Xv6, HelenOS

https://wiki.riscv.org/display/HOME/RISC-V+Software+Ecosystem

Are RISC-V processors better than XYZ?

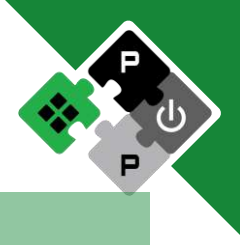
- **Actual performance depends on the implementation**
  - RISC-V does not specify implementation details (on purpose)
- **It is a modern design, should deliver comparable performance**
  - If implemented well, it should perform as good as other modern ISA implementations
  - In our (ETH Zürich) experiments, we see no weaknesses when compared to other ISAs
  - It also is not magically 2x better
- **High-end processor performance is not much about ISA**
  - Implementation details like technology capabilities, memory hierarchy, pipelining, and power management are more important.

RISC-V foundation only defines the ISA



- **The ISA is free, implementations can be done by anyone**
  - ETH Zürich specializes in efficient SystemVerilog based open source implementations
    - **RI5CY/CV32E40P**: 32bit Micro-processor with DSP extensions (maintained by OpenHW)
    - **Ibex**: 32bit minimal processor (maintained by LowRISC)
    - **Snitch**: 32bit small core specialized for cluster based systems
    - **Ariane/CVA6**: 64 bit Linux capable core (maintained by OpenHW)
  - There are many others (SiFive, Codasip, Andes, Frontgrade, IIT-Madras,.. and more)
  - Implementations can also be commercial, it is only the ISA that is open
- **The foundation is working on a set of compliance tools**
  - Only foundation members are allowed to officially call their implementations RISC-V

What PULP provides is a box of building blocks



RISC-V Cores

RI5CY	Ibex	Snitch	Ariane
32b	32b	32b	64b

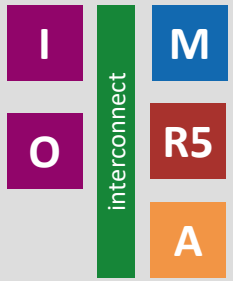
Peripherals

JTAG	SPI
UART	I2S
DMA	GPIO

Interconnect

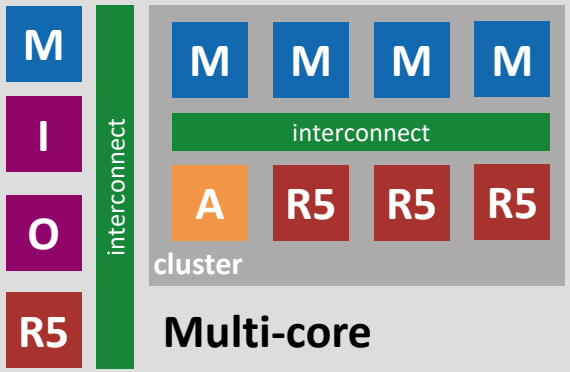
- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

Platforms



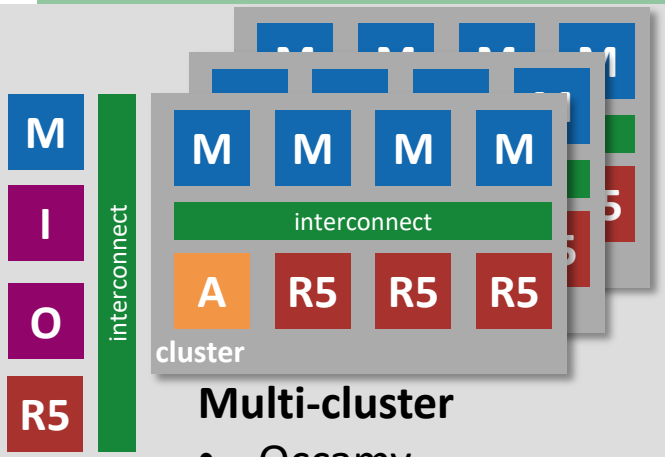
Single Core

- PULPino
- PULPissimo



Multi-core

- OpenPULP
- Mr. Wolf



Multi-cluster

- Occamy
- Hero

IOT → **HPC**

Accelerators

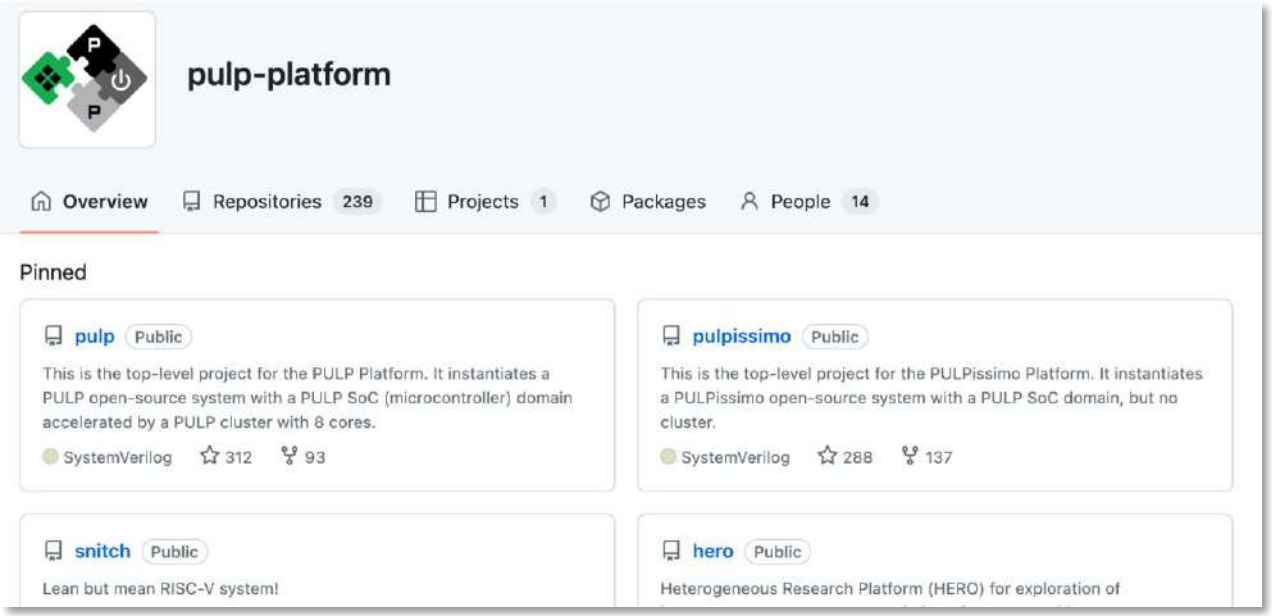
HWCE (convolution)	Neurostream (ML)	HWCrypt (crypto)	PULPO (1st order opt)

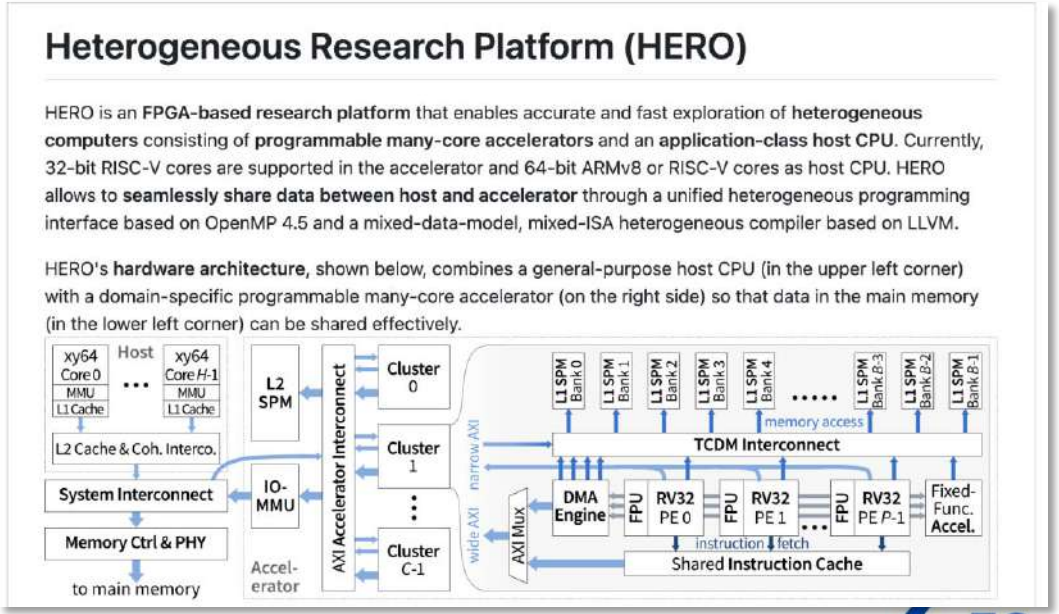
PULP uses a permissive open source license

- **All our development is on GitHub**
  - HDL source code, testbenches, software development kit, virtual platform

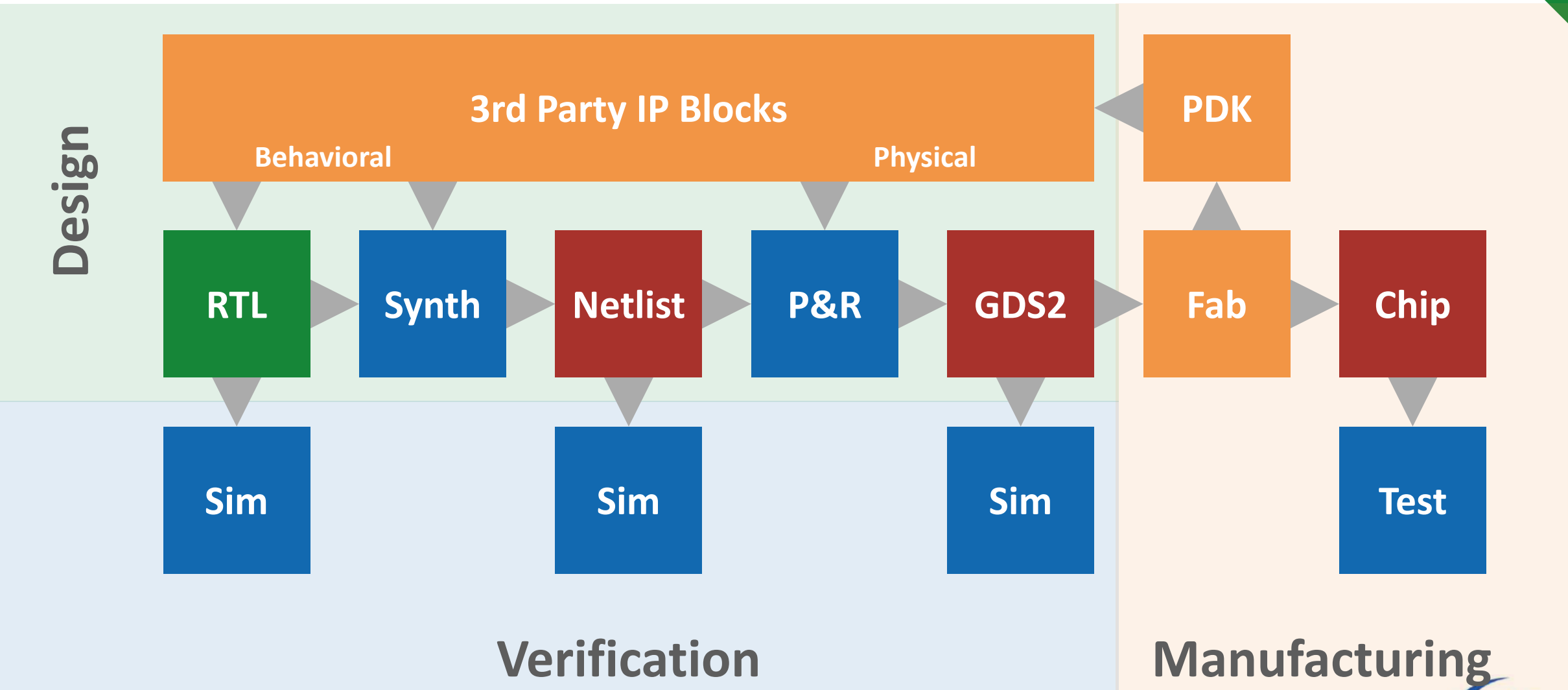
https://github.com/pulp-platform

- Allows anyone to use, change, and make products without restrictions.

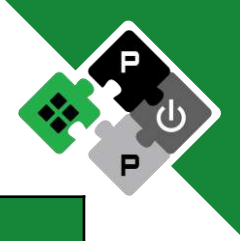




Most of our Open Hardware is still *only* RTL



State of Open Source for Hardware: Rapid Developments



TYPE	EXAMPLES	STATUS
Open Specifications	RISC-V	Established
Architectures	PULP	Quite mature
Implementations in RTL	Snitch, Hero	Many

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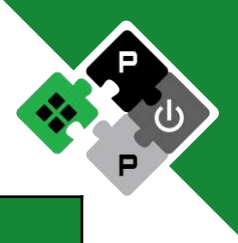

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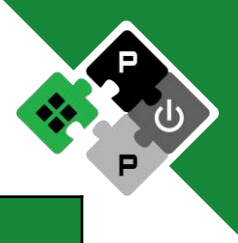

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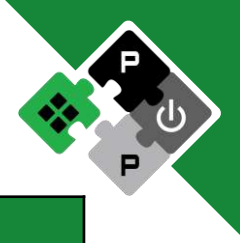
Process Design Kits	Skywater 130nm	Just Started

State of Open Source for Hardware: Rapid Developments



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Process Design Kits	Skywater 130nm	On its way
Open Source Tools	Open Lane	Quite usable

What is PULP doing to maintain our cores?

- **We (ETHZ and University of Bologna) are research groups**
  - Motivated to develop new architectures and systems
  - We needed efficient RISC-V cores (and peripherals) for our work
  - Not so good (or interested) in providing industrial level support for these cores
- **We need help to**
  - Provide support
  - Develop industrial verification
  - Governance of open source repositories
- **Happy to receive this help from**
  - Open HW group (Ariane -> CVA6, RI5CY -> CV32E40P)
  - LowRISC (ZeroRiscy -> Ibex)
  - Others?

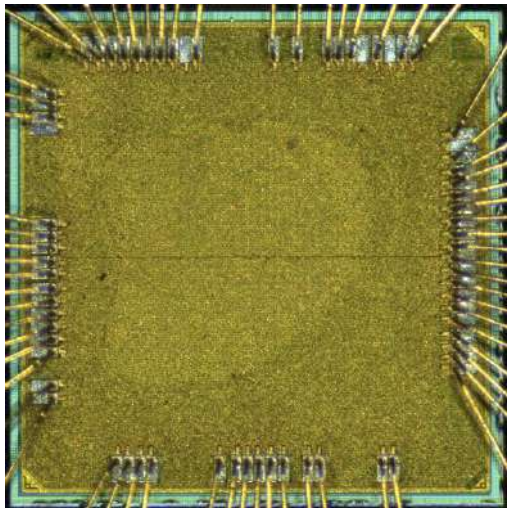
GROUP OPENHW PROVEN PROCESSOR IP

lowRISC

Academic open source → Industrial open source

- OpenHW Group is a not-for-profit, global organization (EU,NA,Asia) driven by its members and individual contributors where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the Core-V family of cores.
- OpenHW Group provides an infrastructure for hosting high quality open-source HW developments in line with industry best practices.

Industrial Collaborations



life.augmented

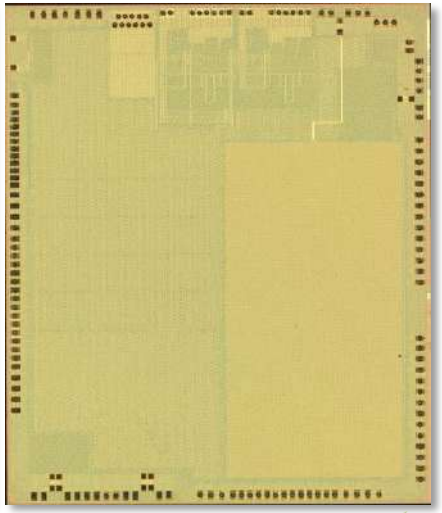
PULPv1,2,3 (ST28 FD)
Demonstrators of 28nm FD-SOI capabilities

Various publications ‘15 – ‘18

QuickLogic®

Arnold (GF22)
IoT SoC combining eFPGA with RISC-V core

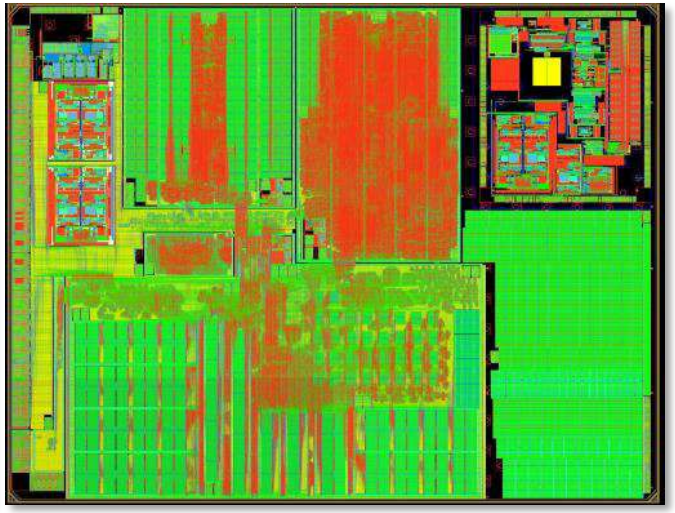
Schiavone et al TVLSI ‘19



GREENWAVES TECHNOLOGIES

Vega (GF22)
IoT Processor with ML acceleration

Rossi et al ISSCC ‘21
Rossi et al JSSC ‘22



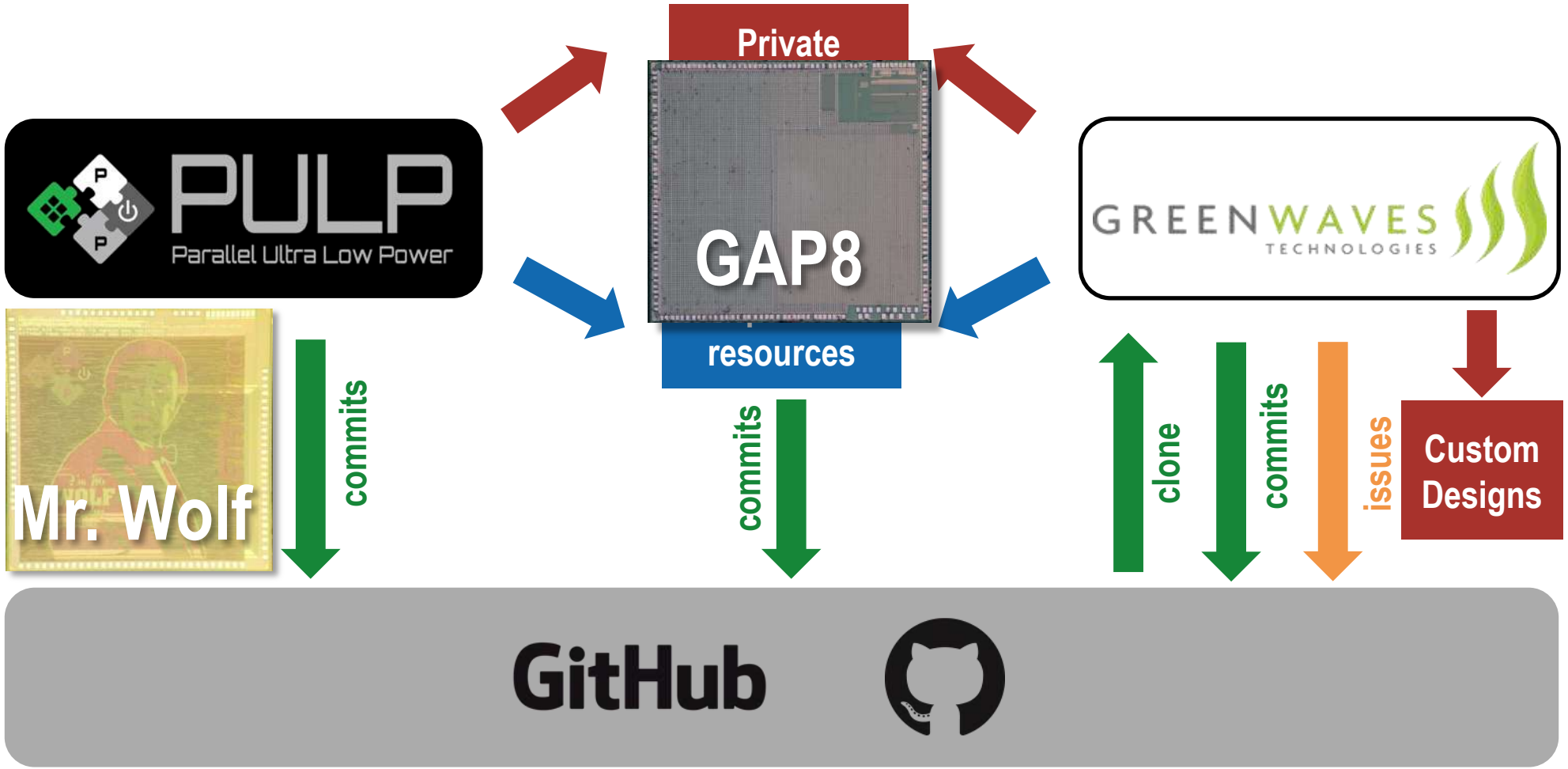
DOLPHIN INTEGRATION
The enabler of low-power Systems-on-Chip

Marsellus (GF22)
IoT Processor with low power modes and AI Accelerators

Conti et al ISSCC ‘23

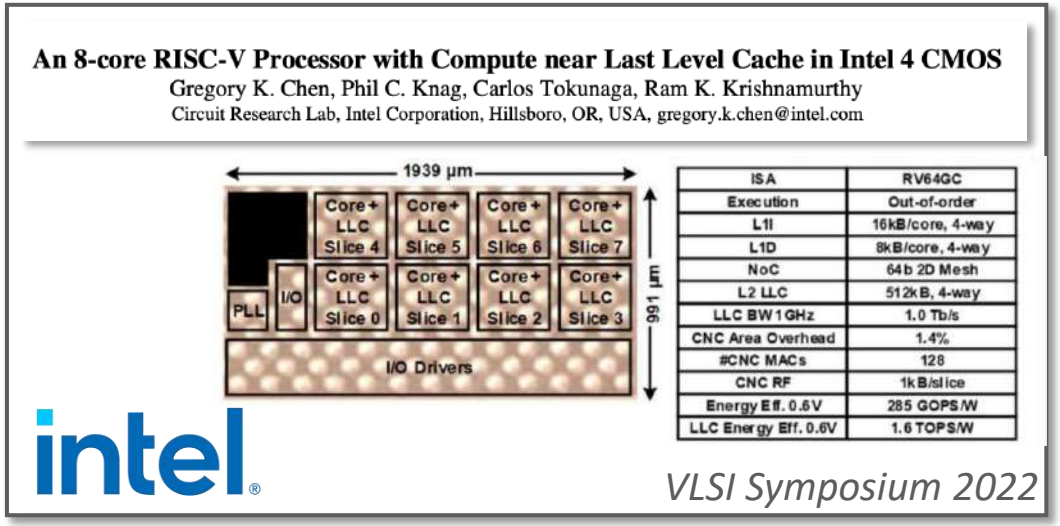
Currently working with Meta, Intel, GF, IHP, PragmatIC, IIT

Open source collaboration scheme explained

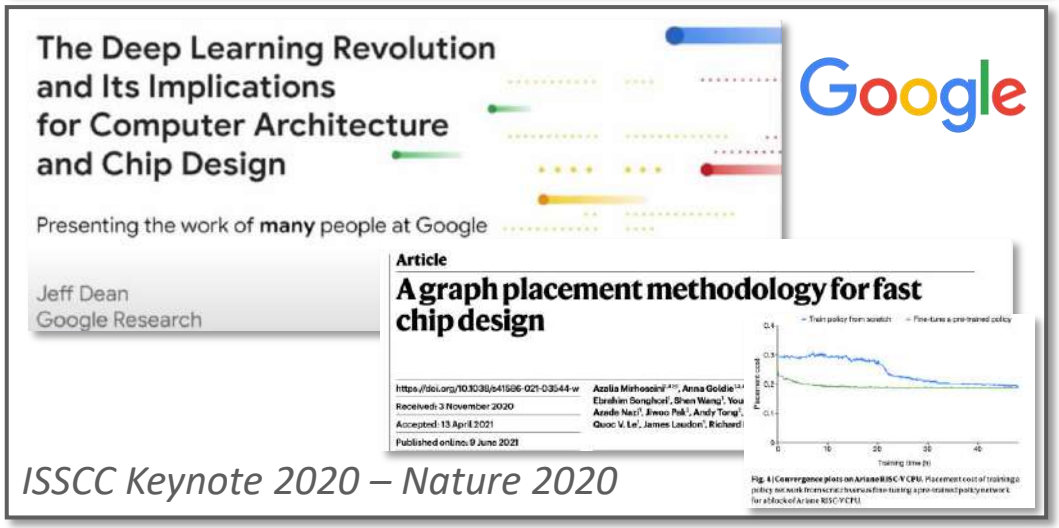


So proud to have supported others in their research

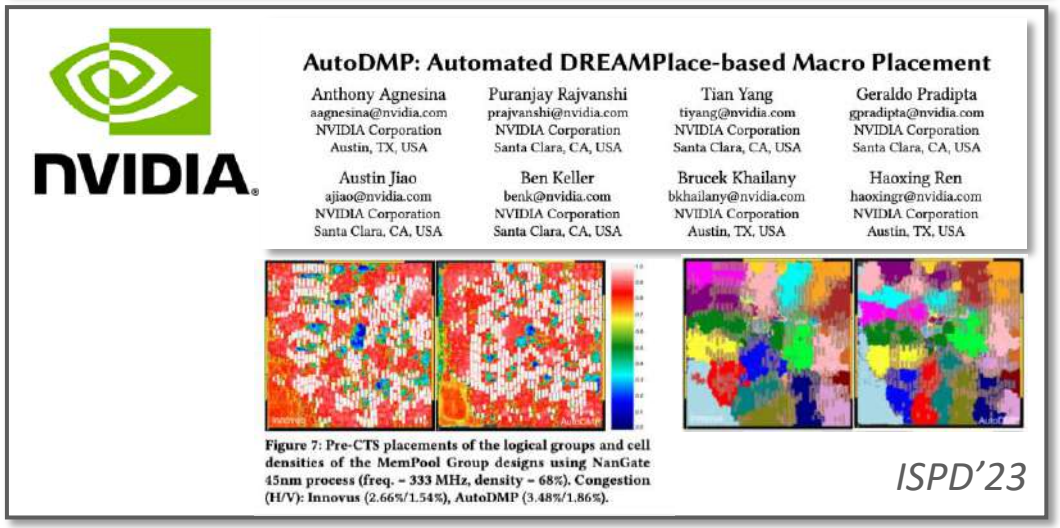
RISC-V week Barcelona 2018



VLSI Symposium 2022

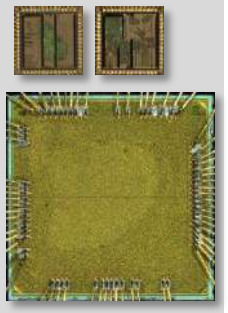
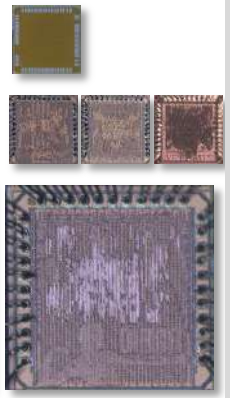
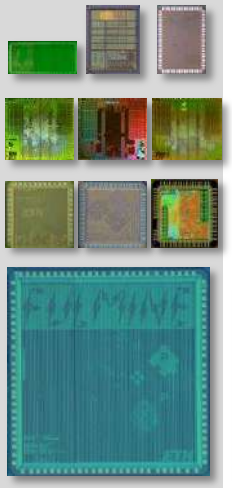
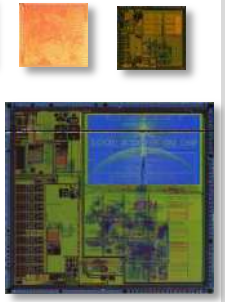
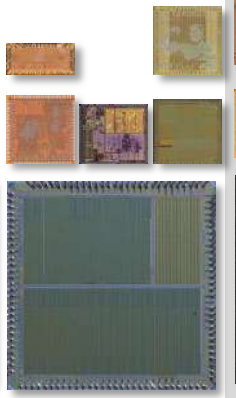


ISSCC Keynote 2020 – Nature 2020



ISPD'23

PULP chips until now – 55 manufactured – 5 on the way

2013 (3)	2014 (5)	2015 (10)	2016 (3)	2017 (2)	2018 (6)	2019 (7)	2020 (3)	2021 (7)	2022 (7)
									
PULPv1 *STM 28FDSOI* Multi-core processor	**Diana** *UMC 65* 4-core system with approximate FPUs	**Fulmine** *UMC 65* 4-core system with ML and Crypto accelerators	**VivoSoC 2.001** *SMIC 130* Mixed signal system for biosignal acquisiton	**Mr. Wolf** *TSMC 40* 8+1 core IoT processor	**Poseidon** *GF 22FDX* 64bit RISC-V core, 32bit Microcontroller system, ML rator	**Baikonur** *GF 22FDX* Dual 64bit RISC-V core, 3x 8core snitch clusters, Body biasing test vehicle	**Dustin** *TSMC 65* IoT processor with 16 cores and QNN enhancements	**Kraken** *GF 22FDX* IoT processor with Spiking Neural and Ternary Inference Engines	**Occamy** *GF 12LPP* ML accelerator with 216 + 1 cores and HBM interface

Check http://asic.ethz.ch for all our chips

Coming soon from the PULP team

FlexIBEX

IoT processor with a twist
a kHz range design

Pragmatic

Iguana

Going all the way in
open source

ihp

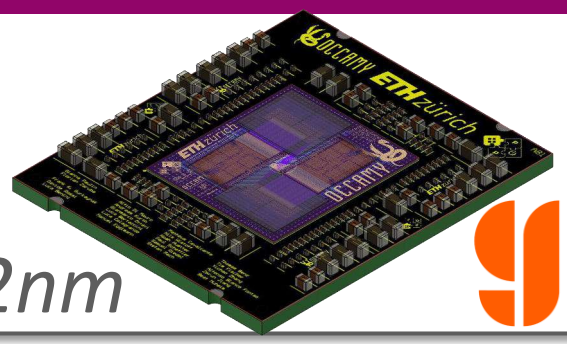
Carfield

Cars (and cats) can also use
a bit of PULP

intel

Occamy

Bringing up
432 core
chiplet in 12nm



A bit of a public service announcement

PULP

Parallel Ultra Low Power

There is much more to come …

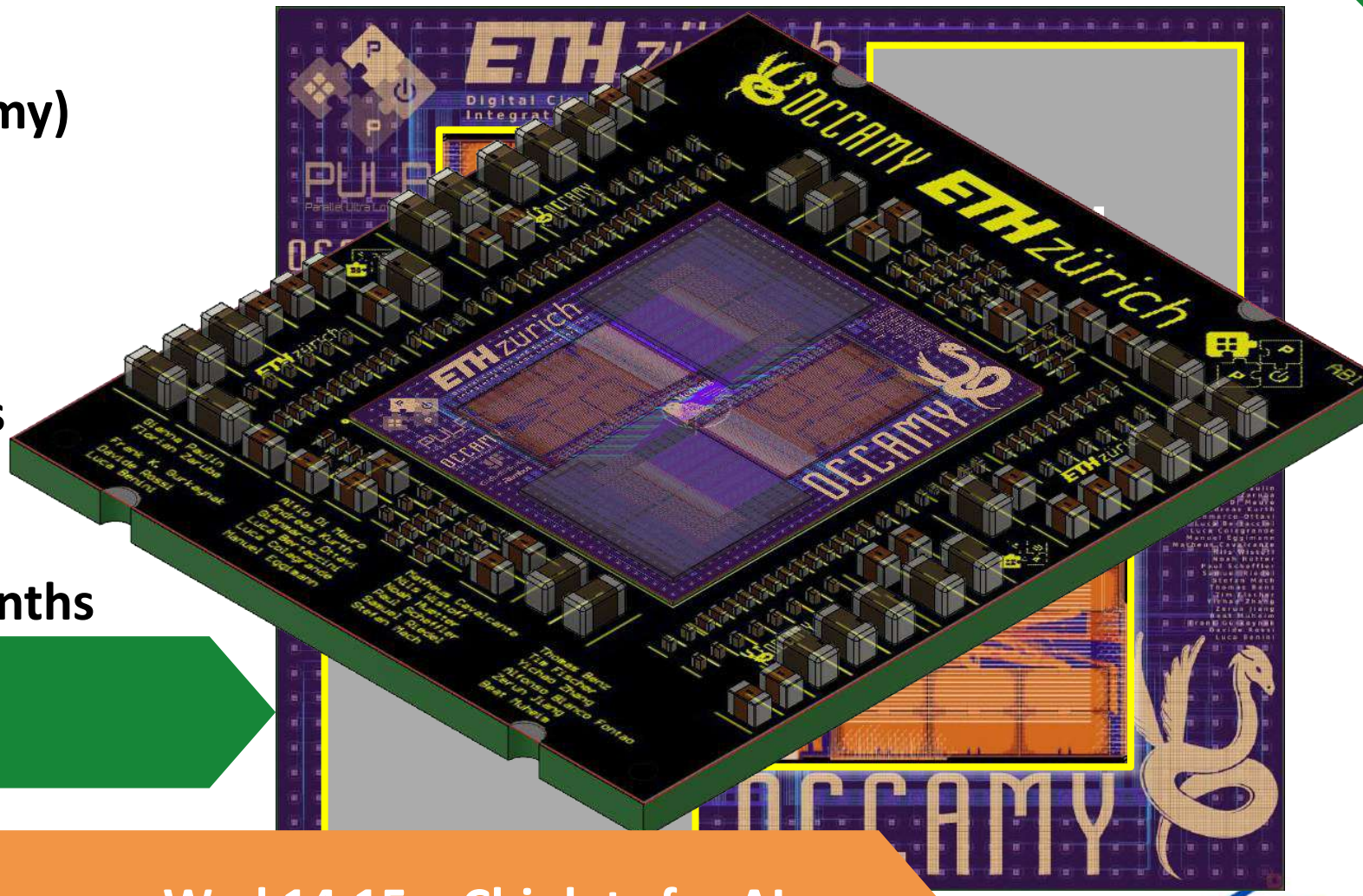
http://pulp-platform.org

@pulp_platform

Additional Slides

Our latest design Occamy: 0.75 TFLOP/s, 400+ cores

- **Chiplet based design**
- **2x Compute chiplets (Occamy)**
  - 216+1 RISC-V cores
  - GF12LPP
  - Running at 1 GHz
- **2x 16GByte HBM memories**
- **Silicon Interposer (Hedwig)**
- **Finished in less than 15 months**

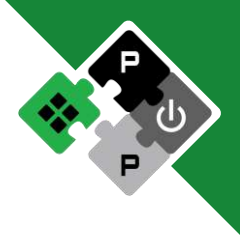


How did we manage this?

- Taped out on 1st of July 2022

More on Occamy – talk by Gianna – Wed 14:15 – Chiplets for AI

Flipside of RISC-V extensions: Many many extensions



https://wiki.riscv.org/display/HOME/Specification+Status

Zacas, Smaia, Ssaia, Zfbfmin, Zvfbfmin, Zvfbfwma, Ssqosid, Zicond, Zxmctr, Smcntrpmf, Sdext, Sdtrig, Smclic, Ssclic, Suclic, Smclicshv, Smclicconfig, Svadu, Zjid, Zimop, Zihintntl, Zbpbo, Zpn, Zpsfoperand, Zjpm, Smrnmi, Zfa, Zisslpcfi, Sscdeleg, Smcdeleg, Sspmp, Zvbb, Zvbc, Zvkg, Zvkn, Zvkned, Zvkng, Zvknha, Zvkbnhb, Zvks, Zvksed, Zvksg, Zvksh, Zvkt, Zvknf, Zvfh, Zvfhmin, Zca, Zcb, Zcd, Zce, Zcf, Zcmp, Zcmt, Zicntr, Zihpm, Shcounterenw, Shvstvala, Shtvala, Shvstvecd, Shvsatpa, Shgatpa, Sscounterenw, Ssstateen, Sstvala, Sstvecd, Sstvecv, Ssu64xl, Svade, Svbare, Za128rs, Za64rs, Ziccamoa, Ziccif, Zicclsm, Ziccrse, Zic64b, Ztso, Zmmul, Zawrs, Zve32x, Zve32f, Zve64x, Zve64f, Zve64d, Zba, Zbb, Zbc, Zbs, Zfinx, Zfh, Zfhmin, Smepmp, Zbkb, Zbkc, Zbkx, Zknd, Zkne, Zknh, Zksed, Zksh, Zkn, Zks, Zkt, Zk, Zkr, Sm1p12, Ss1p12, Sv57, Zicbom, Zicbop, Zicboz, Smstateen, Sstc, Sscofpmf, Svinval, Svnapot, Svpbmt, Zihintpause

Open Source Hardware licensing still a critical issue

- **Two main flavors, divided opinion**
  - **Permissive** (Apache, MIT, BSD..): Favored by the industry, minimum obligations
  - **Reciprocal** (GPL, LGPL,..): Feared by industry
- **In theory, it should be possible to have reciprocal licensing for open hardware**
  - For example text of LGPL problematic for IC Design use.
  - Cern OHL (https://cern-ohl.web.cern.ch/), comes in many flavors (reciprocal, permissive)
  - Still more work needed, not many people understand issues of IC Design
  - Lawyers (in companies) prefer well-known licenses (less work for them).
- **PULP uses Solderpad (http://solderpad.org/licenses/)**
  - Permissive license based on Apache
  - Clarifications for hardware use added by Andrew Katz
  - Had no issues (so far) neither with academic nor industrial collaborations

Timeline of Parallel Ultra Low Power (PULP) project