FOUNDATION

OPENHW™

PROVEN PROCESSOR IP

Revolution in Chip Design

Enabling Open Source RISC-V Designs For Commercial Use

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Agenda

- Which problem OpenHW solves

  Why do we need OpenHW anyway

- Who is OpenHW
- Who is using open source IP
- What is coming

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THANK YOU PULP TEAM!

Thank you for open sourcing your work
Thank you for pushing the boundaries
Thank you for all the amazing work around Chip Design and especially RISC-V
Thank you for being an amazing OpenHW Member

FOUNDATION OPENHW™ PROVEN PROCESSOR IP

Semiconductors: A Global Industry

The Oil of the Digital Age

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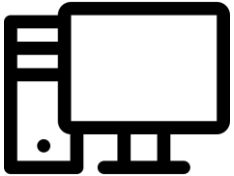
Why do we need semiconductors?

Automation



Computing

Communications

Energy Management

Healthcare

Sensing

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Semiconductor global market

$790 Billion
2025

$1 Trillion
2026

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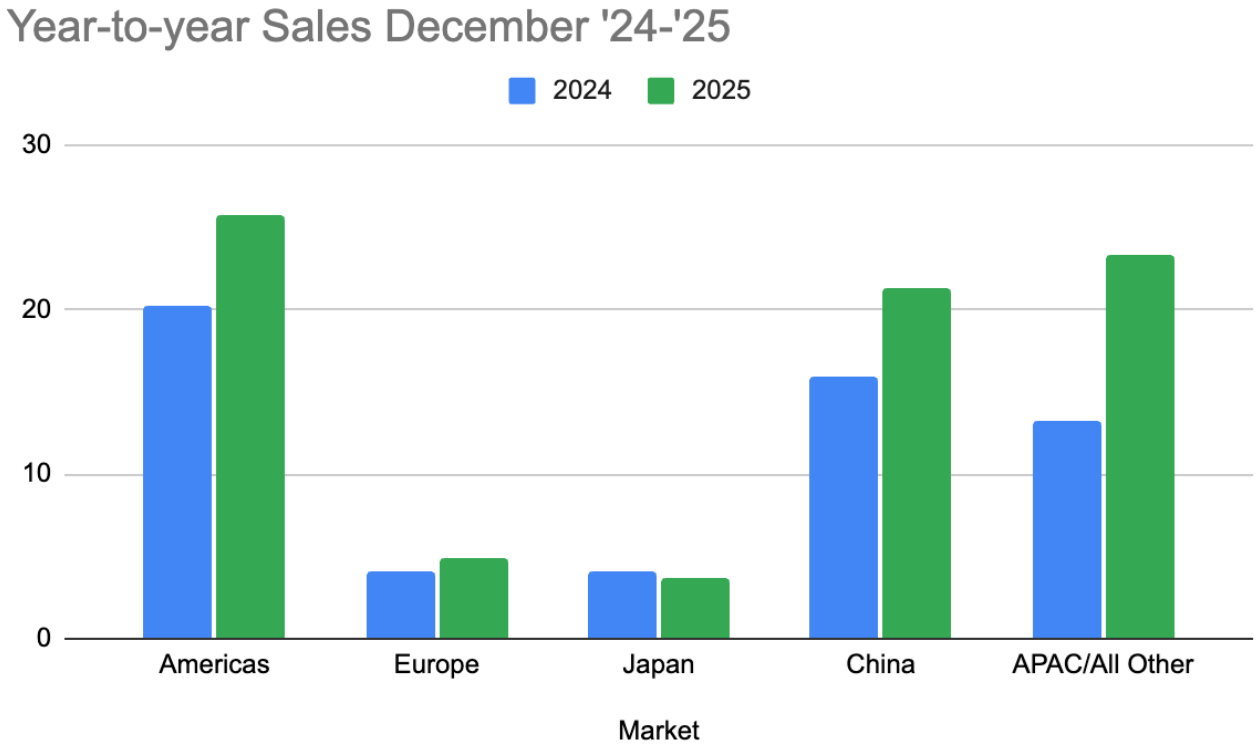
Semiconductor global market



SIA/WSTS Global Semiconductor Sales Table

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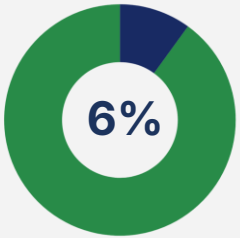
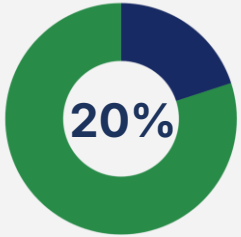
Why do we need RISC-V in Europe?

$790B

Semiconductor Market Value 2025



EU Market Share Today



EU Market Share by 2030

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Why Open Source Hardware? Why OpenHW?

Democratizing access and the production of state-of-the-art systems-on-chip (SoC) for commercial, reserch and training applications on a global scale.

Commercial

Fast changing world
Need for faster adoption
Need for greater flexability

Research

Real world Code
Open Exchange with others
Bringing research into Industry

Everyone

Enable a revolution of chip design by democratizing IP access

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The OpenHW Foundation accelerates the development and adoption of verified, open source RISC-V processor cores and related IP. Being part of the OpenHW Foundation gives you direct access to a vibrant community that is building industrial-grade RISC-V cores and more that meet the demands of modern commercial applications like HPC, automotive, FPGAs, edge, embedded systems and IoT.

Industry-aligned Standards

Industrial-grade Cores and IP

Global Innovation Ecosystem

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OpenHW Business Model

And Who we are

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The Eclipse Foundation Advantage

OpenHW Foundation is part of the Eclipse Foundation

For over 20 years, the Eclipse Foundation has provided a trusted home for open source projects of all sizes, from small developer communities to global enterprises. Our proven vendor-neutral governance and processes help projects and industry collaborations grow, thrive, and deliver real-world impact.

Governance & Stewardship

Guiding vendor-neutral development & ensuring sustainability

IP Management & Licensing

Delivering IP confidence through due diligence & commercially-friendly OSI licenses

Community Development & Participation

Building diverse communities & driving contributions

Branding, Marketing & Events

Building project brands, driving awareness, and hosting developer conferences and community events

Infrastructure & Security

Providing reliable IT services and implementing supply chain security best practices

Fundraising & Ecosystem Development

Through Working Groups, raising funds and recruiting member organisations

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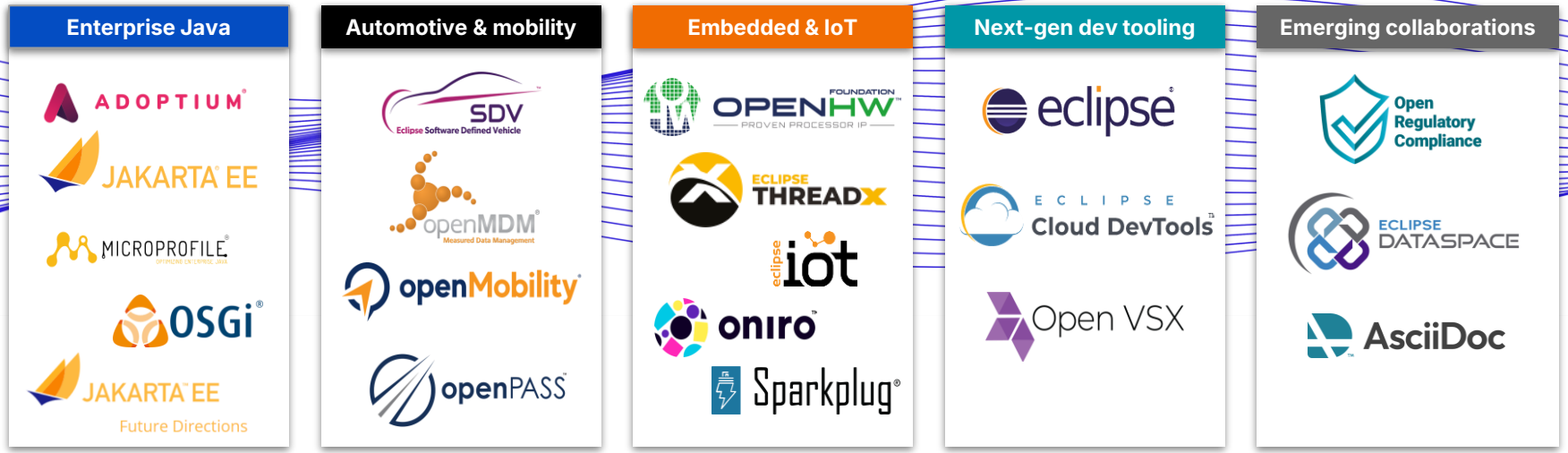
A trusted home for global collaboration

The Eclipse Foundation exists to empower global open source collaboration and innovation. As a vendor-neutral home to 400+ projects, we provide the governance, infrastructure, and community support needed to build sustainable technologies and thriving ecosystems.



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Global collaborations at OpenHW

1

The Eclipse Foundation

Empowering a global community with a mature, scalable, and business-friendly environment that drives collaboration around expanding the RISC-V software ecosystem

2

The Rigoletto Research Project

Supporting the transition from classical automotive Electronic Control Units (ECUs) to fully programmable Domain Control Units (DCUs) or Zonal Control Units (ZCUs)

3

The Tristan Research Project

Delivering high quality, industrial-grade, open source RISC-V cores as a base for SME in Europe to build upon for improved sovereignty, time-to-market, and focus on innovation

4

RISC-V International

Working hand in hand to drive adoption of the open standard RISC-V Instruction Set Architecture (ISA), related specifications, and stakeholder community

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A global community of innovation

The **OpenHW Foundation** member community is democratizing the production of state-of-the-art systems-on-chip (SoC) for commercial applications on a global scale. Join us!

Chat with the OpenHW community on Mattermost

Attend our technical Working Group calls

Explore the OpenHW Foundation repository

Stay informed via the Community Newsletter

Collaborate with the community on mailing lists

Visit the team at industry events

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OpenHW Background & Business Model

- Founded 2019
- Mission “make Open Source RISC-V Cores industrial grade”

- Many Open Source Cores, but ready to use?
- Verification and open bugs is an issue
  - OpenHW: If everyone comes together and does a little, we get robust Cores for everyone

- Since Jan 2025 part of Eclipse Foundation

- Financed via Member fees
  - Eclipse member fee https://www.eclipse.org/membership/#tab-fees
  - OpenHW member fee https://www.eclipse.org/org/working-groups/openhw-foundation/charter/
  - Member fees are based on company revenue

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OpenHW Foundation Membership

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The OpenHW Foundation team

Core Team

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Verification Engineer

Junchao Chen
Verification EE

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Verif EE

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Davide Schiavone
Director of Engineering Cores

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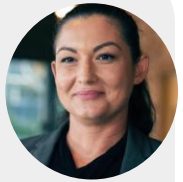
Sr. Content Manager



Thea Aldrich
Sr. Manager Product Marketing

Extended Team

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Michael Plagge
VP, Ecosystem Development

Clark Roundy
Director, Head of Outreach & Engagement

+90 staff globally

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Use Cases of OpenHW

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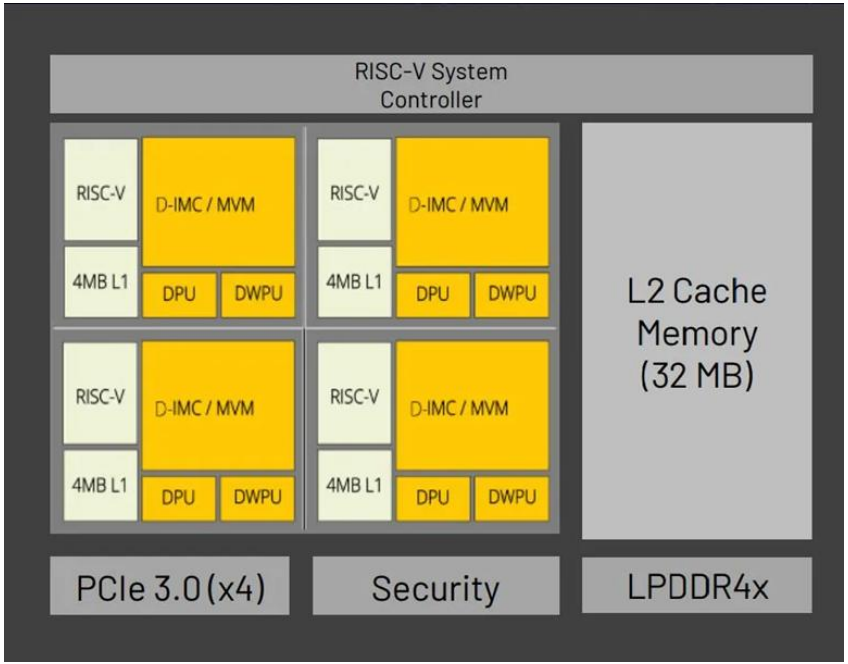
AI at the Edge

AXELERA ARTIFICIAL INTELLIGENCE **edge AI**

- Low-power
- Suitable for deeply embedded applications
- Available in M.2 form factor
- Leveraging OpenHW RISC-V IP
  - Shipping in volume
  - Used in real world
  - European UniCorn



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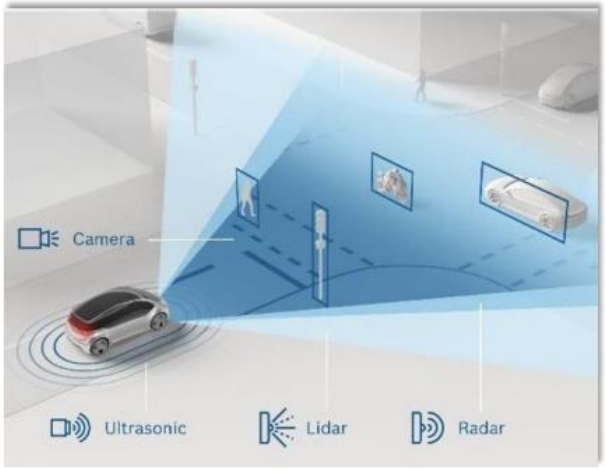
RISC-V in Automotive

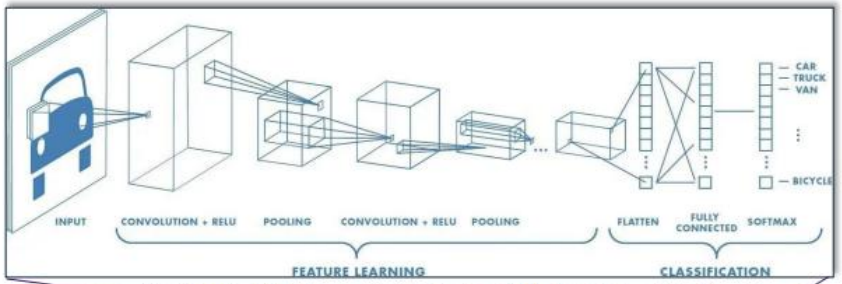
Bosch in Tristan (a Europe Chips JU consortium)

ADAS for object detection powered by OpenHW CVA6 RISC-V

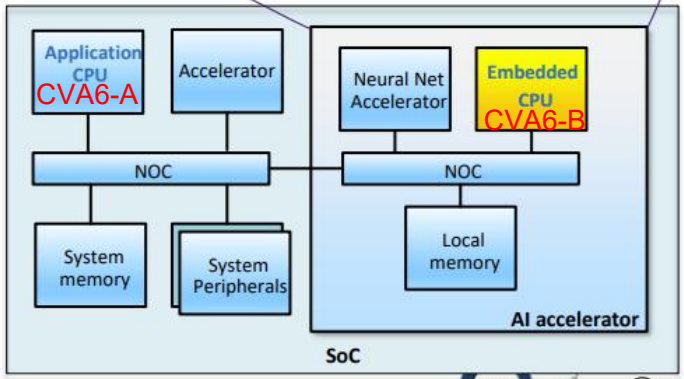
2 Cores, different config.

ADAS* A.I : Camera/Radar Image classification





https://saturncloud.io/blog/a-comprehensive-guide-to-convolutional-neural-networks-the-eli5-way/



* : ADAS : Advanced Driver Assistance Systems

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TRISTAN

BOSCH

Source: https://www.youtube.com/watch?v=Hfj7wsad1tA

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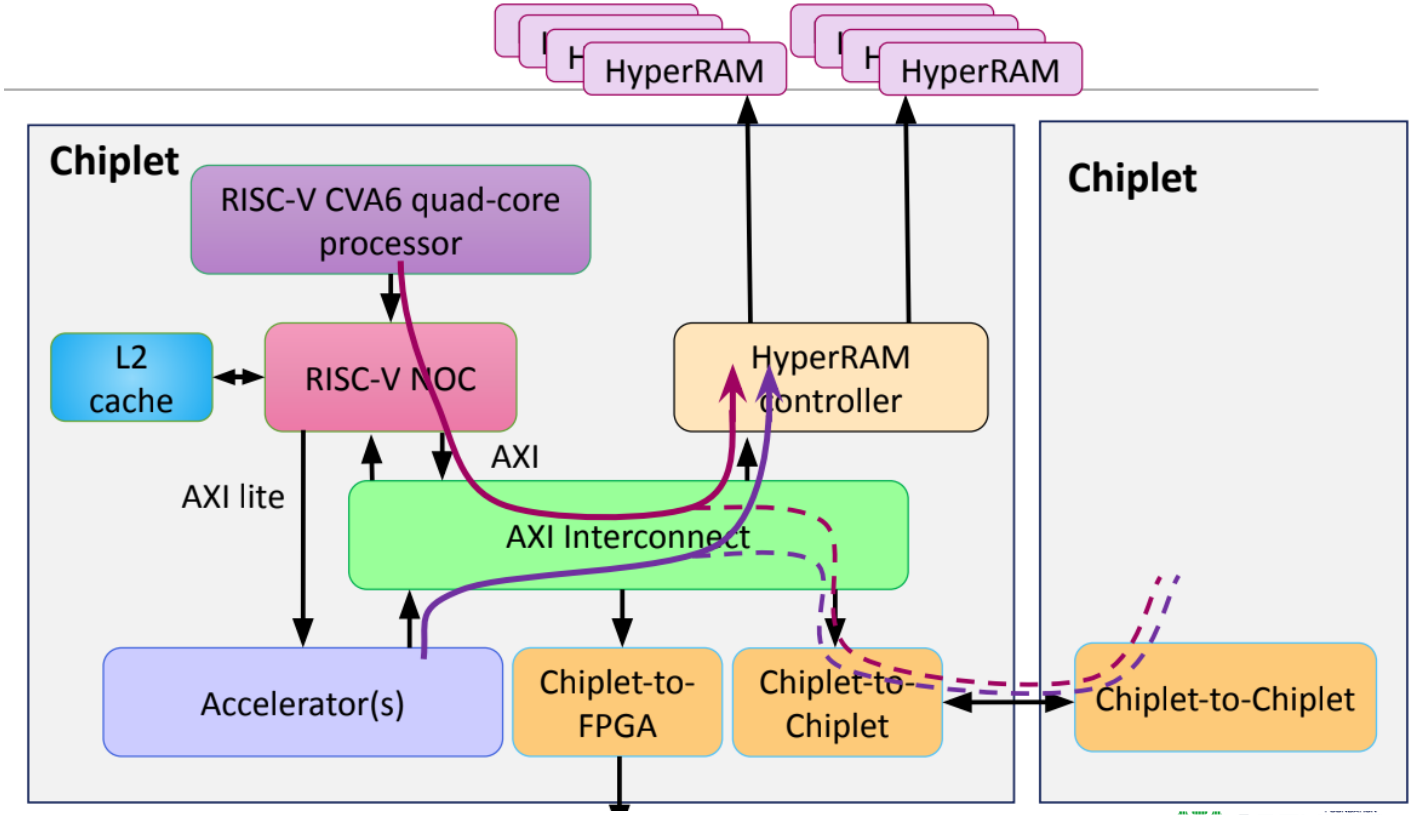
OpenHW CVA6 in Chiplet's – REBECCA

- EU Project REBECCA

Hardware Global Routing
- Chiplet-to-Chiplet
- CVA6 for Linux
- 2 HyperRAM channels

Software Device Driver
- Memory allocation
- Non cacheable or flashcache
- Physical addresses to accelerators



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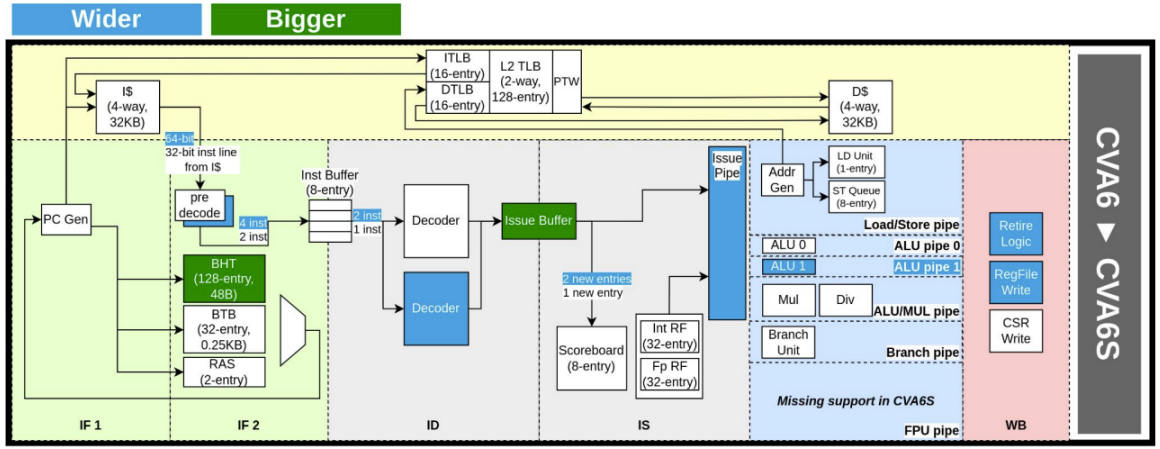
Collaboration CVA6 -> CVA6S -> CVA6S+

- CVA6 IPC (Instructions Per Clock) is constrained by its simple, scalar in-order front-end microarchitecture
- CVA6S is the superscalar dual-issue version of CVA6 by Thales, making the core suitable for more demanding workloads (×2 instruction fetch width, ×2 decoding and issue logic, Secondary ALU)



- Enhance to CVA6S+ by adding:
  - ➔ Register renaming
  - ➔ Improved branch predictor
  - ➔ ALU-ALU forwarding
  - ➔ FPU integration in superscalar mode
  - ➔L1 HDPCache

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OpenHW Products/Roadmap

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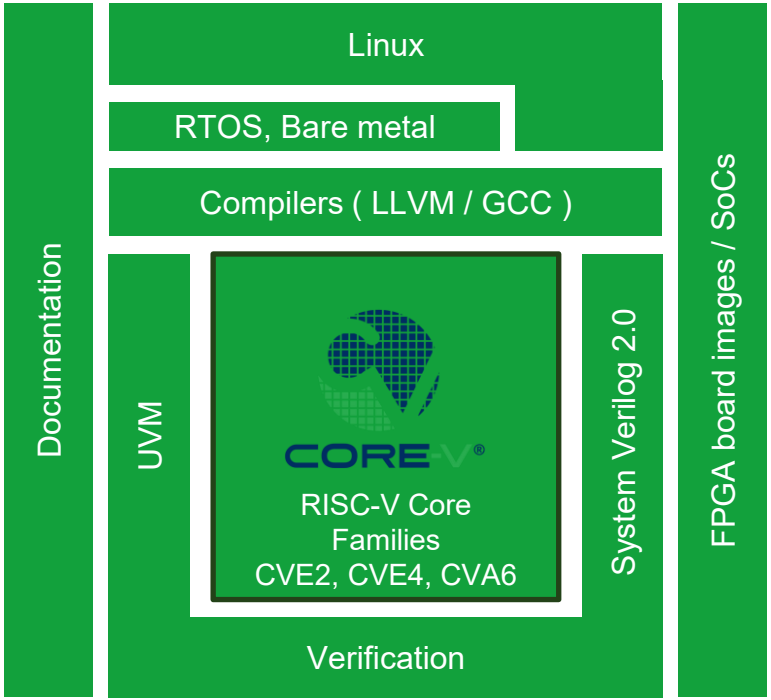
OpenHW Foundation Deliverables

- **License**
  - Apache 2.0/Solderpad
- **Cores**
  - SystemVerilog
- **Test benches**
  - UVM, System Verilog, a little python and tcl
- **Tools**
  - Siemens Mentor Questa, Cadence, Synopsys,
  - Verilator, Yosys,…
- **Support software**
  - Compilers (LLVM, GCC)
  - RTOSes (FreeRTOS, Eclipse ThreadX)
- **Documentation**
- **FPGA Board Images / SOCs**



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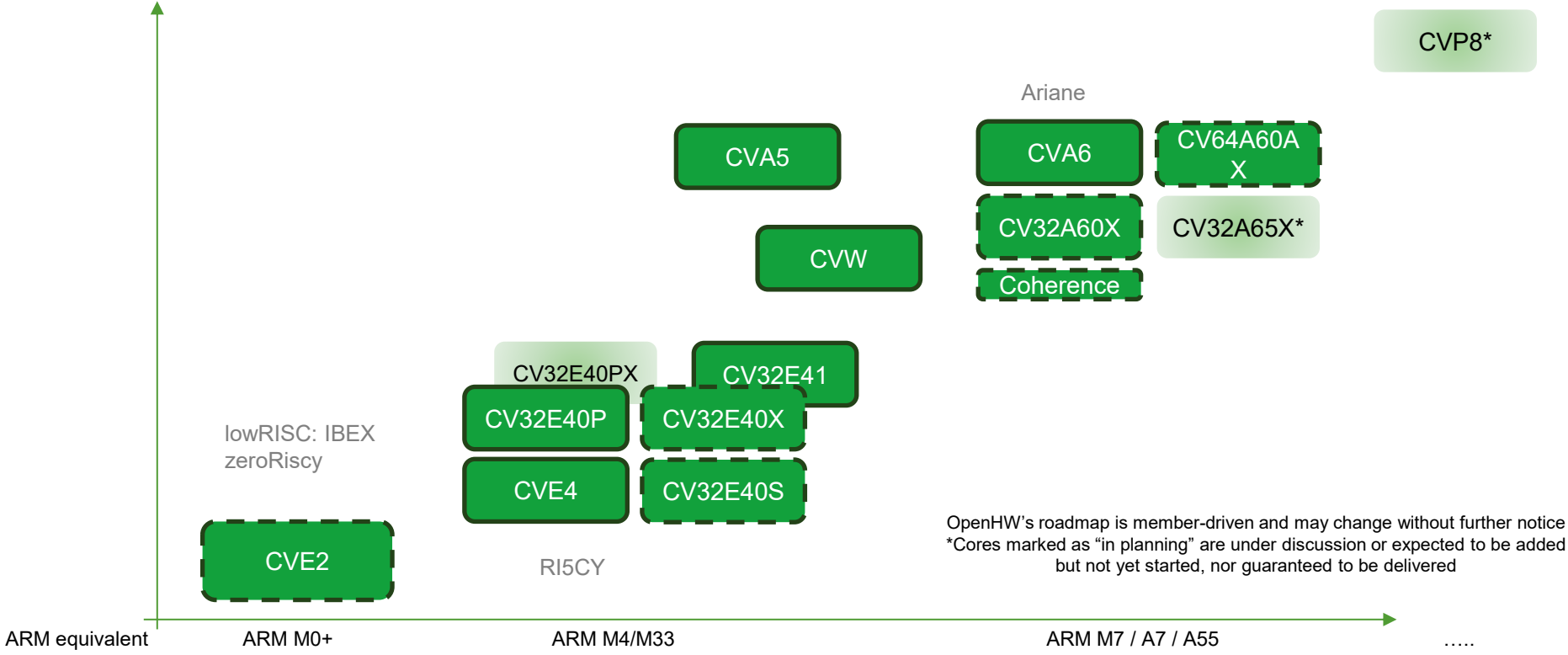
OpenHW RISC-V Roadmap



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Product details

Cores and more

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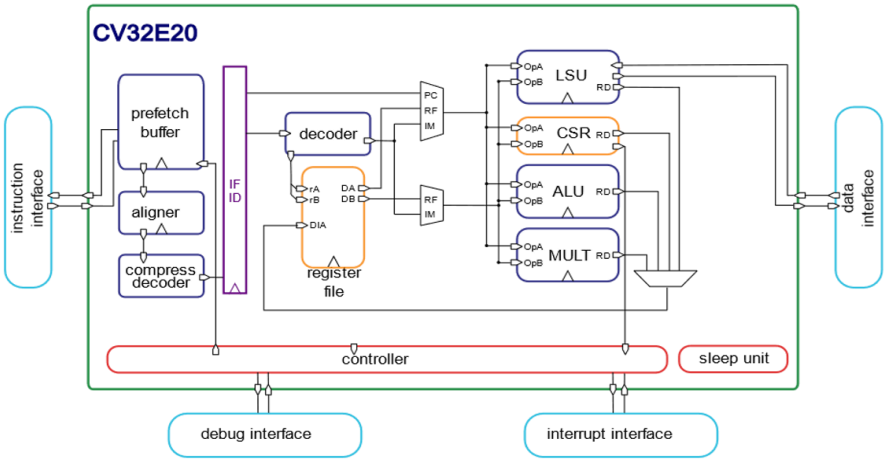
CV32E20 – 2 Stage Deeply Embedded

- 2-stage, in-order, single-issue
- RV32[I|E][M]CZicount_Zicsr_Zifencei[_Zce]
- M-mode, CLINT, OBI

- Low area core
  - Optimized power and area for control-oriented applications
  - Starting point lowRISC Ibex (which started from ETH zero-riscy)
    - Clean-up parameters
    - Aligning IP interface with CV32E40* cores

- Project goal: industrial grade (TRL 5)



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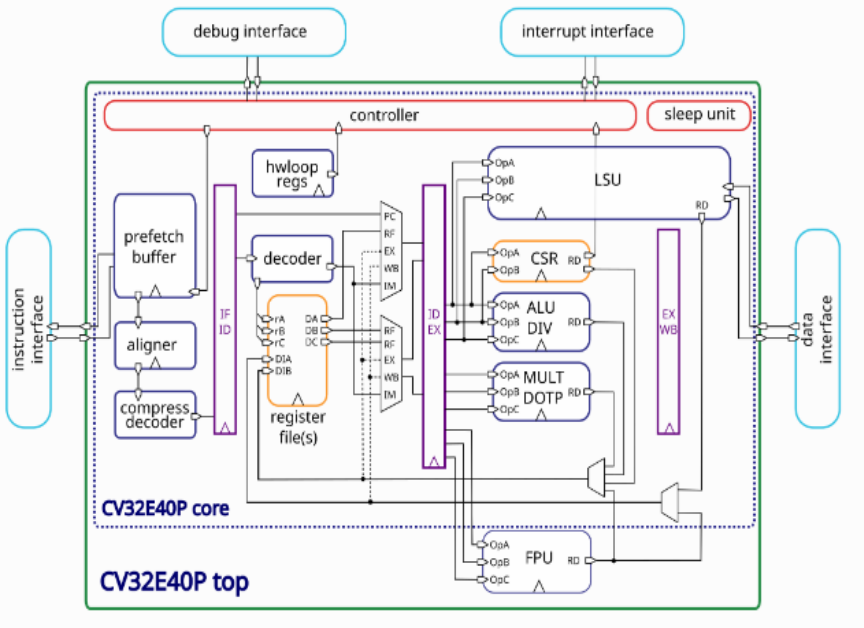
CV32E40P:v2 - MCU with custom DSP extension

- RV32[I|E][M| XPULP
- RV32PULP_XPULP extensions
  - Verification and Reference Model with RVFI
  - Moving the existing instructions to the RISC-V custom space
  - SW support with upstream GCC and LLVM compiler
  - LEC to v1 when PULP_XPULP=0
- RV32F extensions
  - Verification
- Project goal: industrial grade (TRL 5)
  - Status: 5 missing proofs for a custom module HW_loops missing



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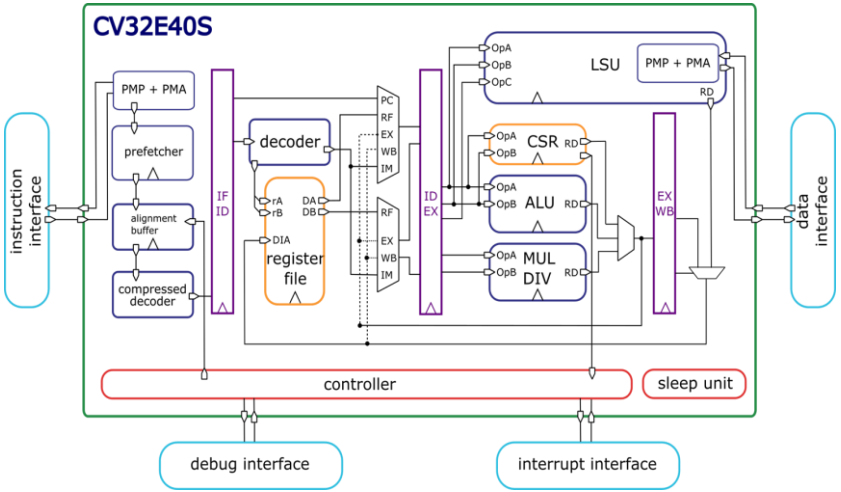
CV32E40S – MCU Style Security Core

- 4-stage, in-order, single-issue
- RV32[I|E][M|Zmmul]
- Zca_Zcb_Zcmp_Zcmt
  [Zba_Zbb_Zbc_Zbs_Zkt_Zbkc]
  ZicsrZifenceiXsecure

- M/U-mode, CLINT or CLIC, OBI,
  ePMP, PMA, bus error

- Xsecure: Custom Security Extensions

- Project goal: industrial grade (TRL 5)



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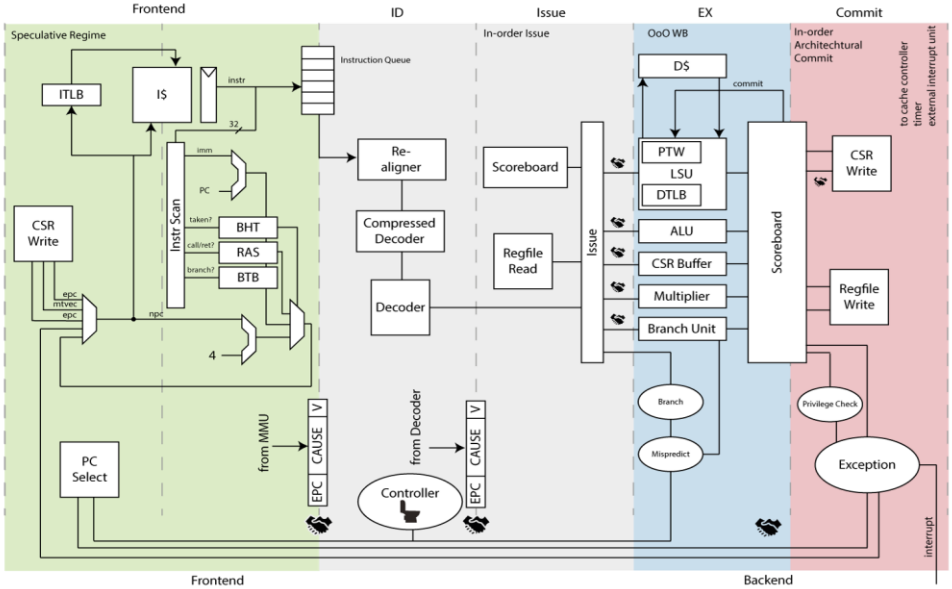
OpenHW CVA6 – old Engineers view

- 6-stage, in-order, single-issue
- RV{32|64}IMAC[FD][V]Zicsr
- M/S/U-mode, CLIC, AXI

- Flexible application core
  - Linux-compatible thanks to MMU
  - 32 or 64 bit (CV32A6, CV64A6) from same RTL (64b from ETH, 32b from Thales)
  - L1 caches

- Project goal: industrial grade (TRL 5)
  - CV32A60X by Thales a 32bit Core has rached TRL5



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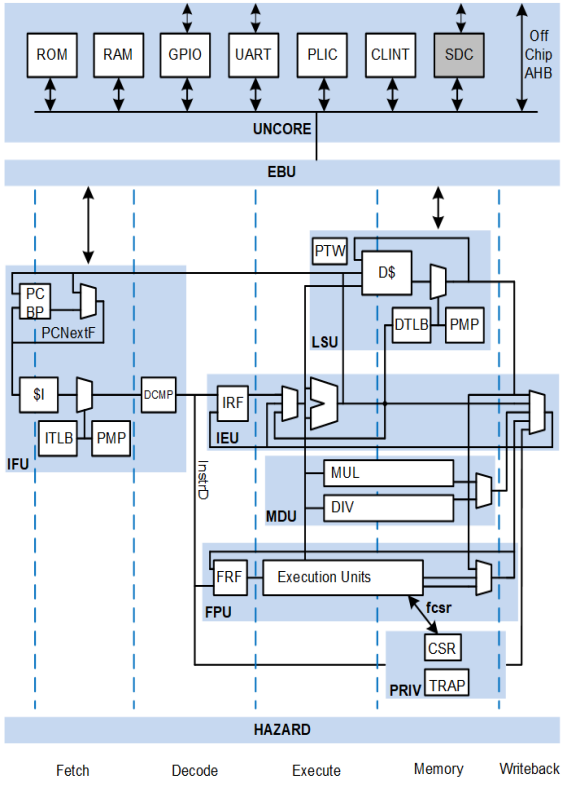
CVW / CV-Wally – Application ready Core

- 5-stage, single-issue, in-order
- RV{32,64}{I,E}[M][F[Zfh][D][Q]][A][C]
  - Cache
    - none, associativity, capacity
  - Branch Prediction
    - none, 2b BHT, GSHARE
  - MMU and TLB
    - entries, sv32/sv39/sv48



- M, S, U Privileged support
- CLIC (and PLIC support)
- Targets both FPGA and ASIC

- Expect first RVA23 Profile compliant open source CPU by Q4,'26

- Project goal: industrial grade (TRL5)

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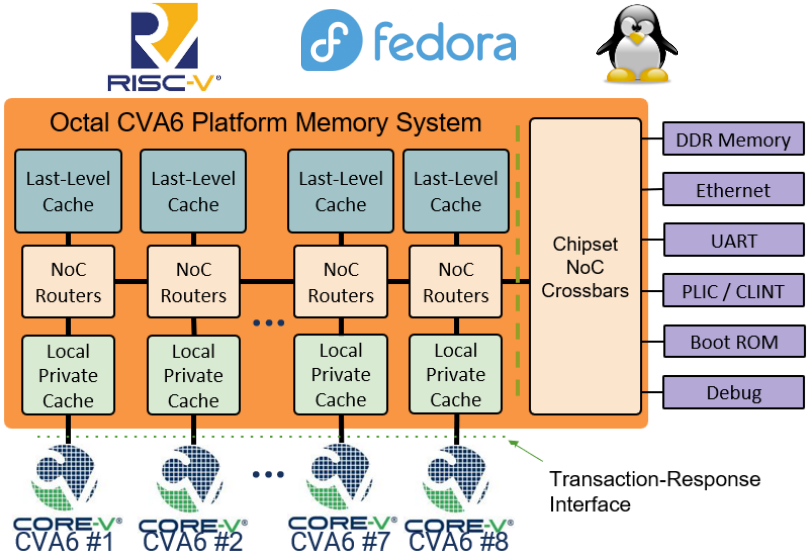
CORE-V CVA6 Platform

- Pre-built, open-source, vendor neutral, RISC-V systems built on bench top Digilent Genesys2 FPGA boards and FPGA-based Amazon EC2 F1 instances, for dual & octal CORE-V CVA6 coherent clusters
- SW CI environment running on Red Hat RISC-V Fedora Linux ”out of the box” (no bitstream generation or setup required)
- Community based, inherently updatable to address issues raised while keeping pace with RV Platform & Profile standard setting
- https://github.com/openhwgroup/cva6-platform



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Barcelona Supercomputing Center
Centro Nacional de Supercomputación

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THALES
Building a future we can all trust

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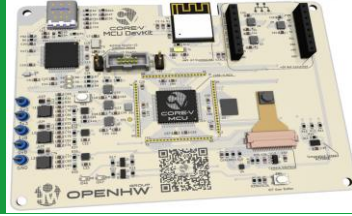
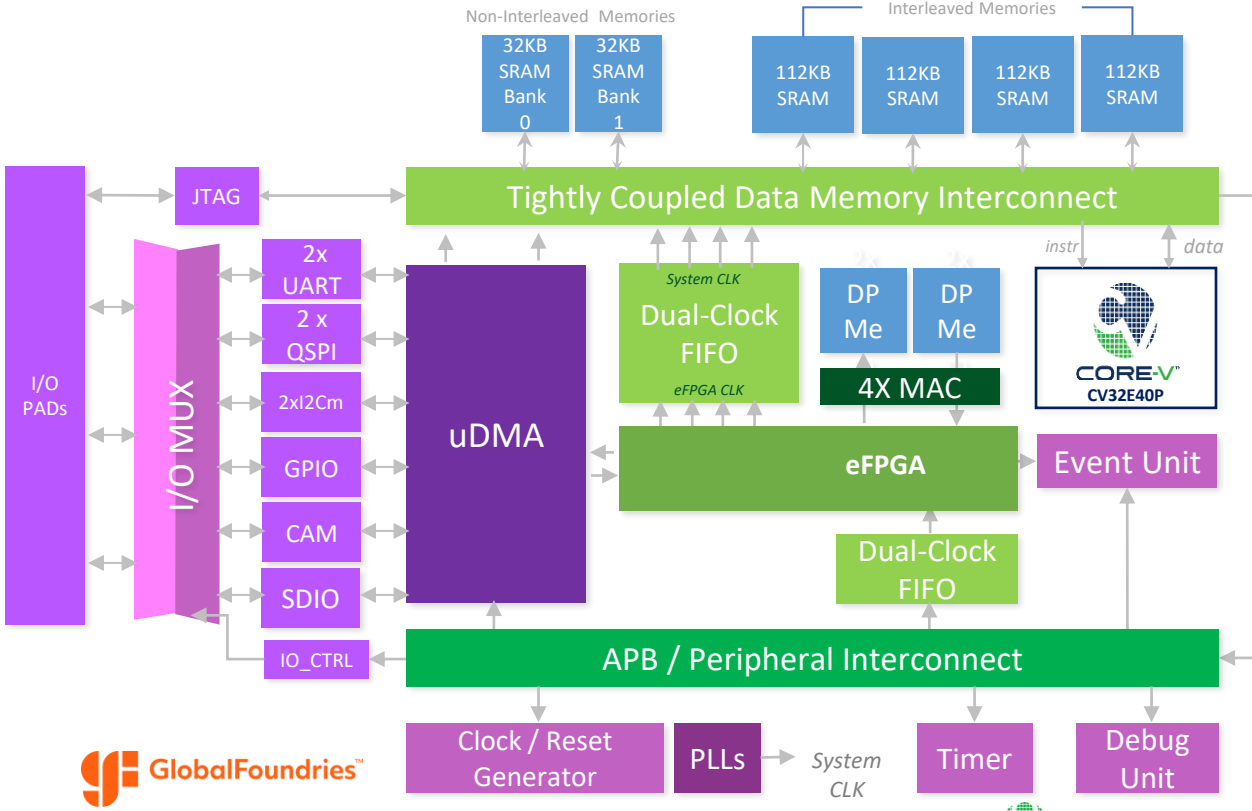
OpenHW CORE-V MCU - Example



- Real Time Operating System (e.g. FreeRTOS, ThreadX) capable ~400+MHz CV32E4 MCU
- Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc) for interfacing with sensors, displays, and connectivity modules
- Built in 22FDX with GlobalFoundries
- Full Project on Github



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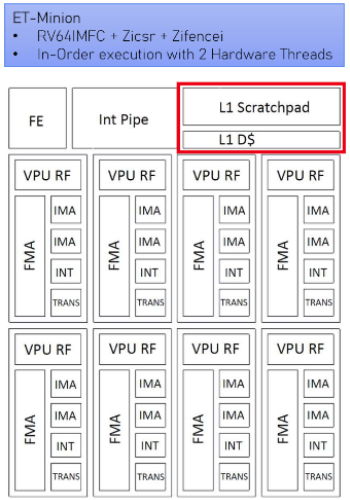
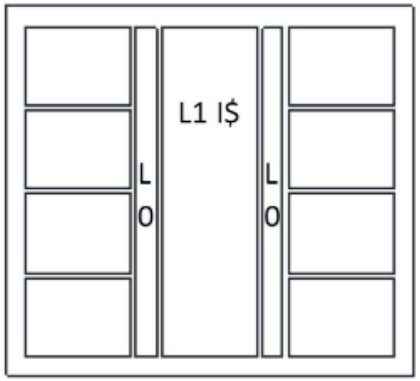
Coming: OpenHW CORE-ET Silicon Platform

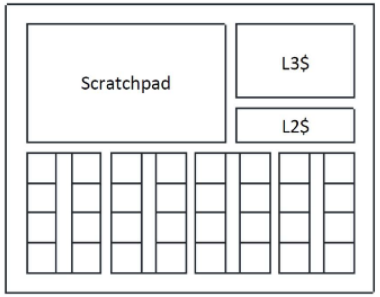
- Esperanto IP first commercial ManyCore 1024 RISC-V AI Chip
- AI Nekko is making the IP Open Source at OpenHW
- Tapeout in TSMC 16nm sheduled



Minion



8x Minion = Neigh



4x Neigh = Shire

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RISC-V in Europe

Building the Infrastructure for European Success and making it accesible

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EU Success Story #1: Tristan Research Project

- EU-funded via Chips JU
- SME-first strategy
- CVA6, CVE4 & CVA6 used in real European designs
- OpenHW: Core provider and project enabler

ETH zürich

THALES

cea

SIEMENS

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

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EU Success Story #2: Rigoletto Research Project

- **Business Goal**: Supporting the transition from classical automotive Electronic Control Units (ECUs) to fully programmable Domain Control Units (DCUs) or Zonal Control Units (ZCUs)
- **Technical Goals** (from the proposal document):
  - “Establish the foundation for a next-generation Automotive Hardware Platform based on the open RISC-V instruction set architecture (ISA).”
  - “Developing RISC-V intellectual property (IP) components, including processor cores, accelerators, interconnects, memory hierarchy and peripheral subsystems.”

64 partners	€67.3M est. Cost	€19.3M EU funding	~3 FTE EF

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EU Success Story #3: Turandot Research Project

- **Business Goal**: Develop in-vehicle high-performance automotive RISC-V reference hardware platform capable of PetaOPS computing taped-out on leading-edge processes
- **Technical Goals** (from the proposal document):
  - “develop RISC-V–based high-performance and real-time microprocessors for Automotive, including application processor solutions, AI accelerators and IP’s library, validated and benchmarked against state-of-the-art competition”
  - “deploy the next-generation E/E architectures in future digital vehicles to make them most competitive in terms of performance vs. non-RISC-V alternatives”

34 partners	€272.3M est. Cost	€78.6M EU funding	~2 FTE EF

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RISC-V in Europe – making it accesible

The Silo Problem

Europe has world-class IP, but it's hidden in silos:

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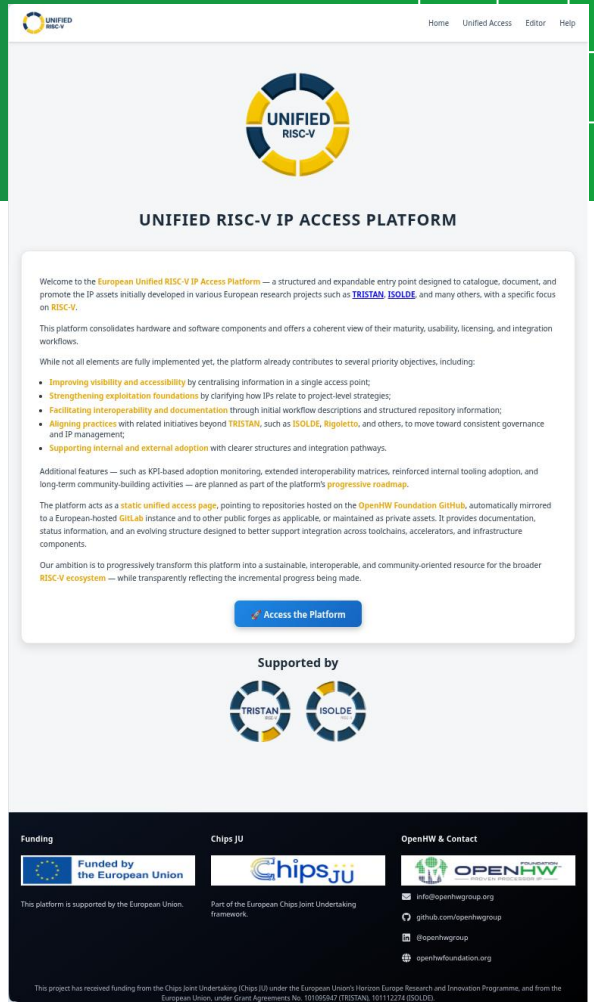
Unified RISC-V IP Access Platform

- **Available at** https://openhwgroup.github.io/tristan-isolde-unified-access-page
- **Embedded at** TRISTAN web page at https://tristan-project.eu/uap

Overview

- **Welcome page** – welcome page encompassing the role of the UAP as the reference for developed RISC-V IPs developed under EU projects (TRISTAN, ISOLDE and others).
- **Platform page** – comprising a dynamic table, with the latest IPs information as available under the Virtual Repository.
- **Editor page** – to edit or update IP and project entries.
- **Help page** – guide on how to contribute to the UAP or its Virtual Repository catalogue of IPs, *currently under construction*.



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Unified RISC-V IP Access Platform

Name	Category	License	Status	Description	Project
Compression and decompression of digital waveforms	Core	TBD	In progress	Custom instructions for CV32E40X core to improve the performance of real-time compression and decompression of digital waveforms	
CVA6	Core	Solderpad	In progress	A configurable family of RISC-V application/embedded cores targetting FPGA and ASIC technologies	
CVE2	Core	Solderpad	In progress	A single-issue 2-stage pipeline embedded class of RISC-V CPUs	
Extensions to the micro-architecture of CV32E40P core	Core	Solderpad	In progress		
Hypervisor	Core	Solderpad	Released	Hypervisor support for CVA6 complying with the RISC-V hypervisor extension specifications	
Riviera: RISC-V ISA Extensions for NFC Applications	Core	LA_OPT_NXP Software License	Design and Verification completed	CV-X-IF compliant RISC-V Co-processor for a NFC Receiver decoder custom DSP acceleration	
RVB / RVP Standard Extensions support for CV32E40P core	Core	Solderpad	In progress	Development of light-weight RISC-V Instruction Set Architecture (ISA) extensions to improve the energy efficiency of low-bit-width mixed-precision integer arithmetic	
RVV coprocessor for CVA6	Core	Solderpad	Released	RVV (vector) co-processor for CVA6 with support for low precision integer arithmetic (down to 8-bit vector data types) and multi-precision floating-point operations	
SCAIE-V custom instruction interface for CVA6	Core	Apache 2.0	In progress	SCAIE-V is a portable and scalable hardware interface for easily adding custom instructions to processors ranging from microcontrollers to application-level cores	

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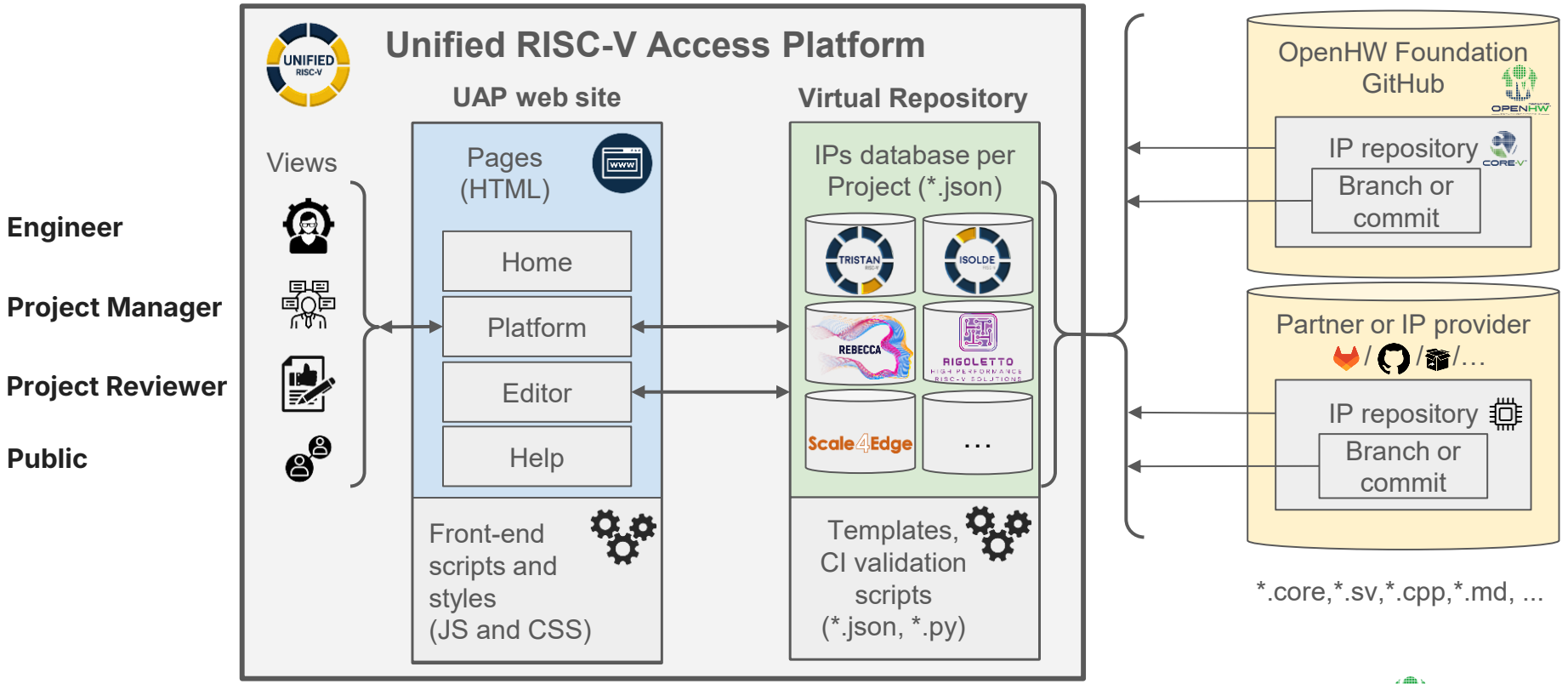
Unified RISC-V Access Platform infrastructure



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FOUNDATION
OPENHW™
PROVEN PROCESSOR IP

OpenHW

Where we are heading from here

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Call for action - Build Your Own Chip With Open Source IP

Lets innovate together at OpenHW – the place to build open source SoC's

1) Evaluate our Cores: https://github.com/openhwgroup

2) Join our Community, collaborate: https://openhwfoundation.org/get-involved/

3) Become a Member: https://openhwfoundation.org/membership/become-a-member/

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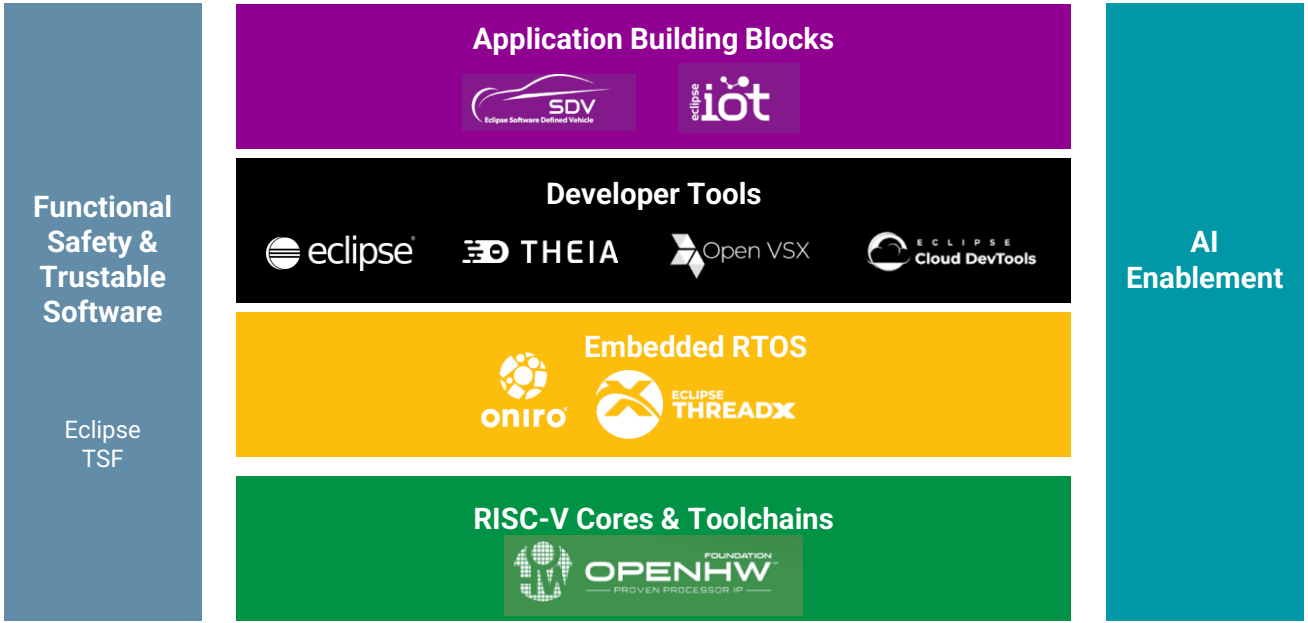
A Vision for the Future

Toward an Autonomous, Trustable & Scalable RISC-V Stack



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Chip Design Happens at OpenHW

The place to design open compute platforms
MCUs, SoCs, AI accelerators, chiplets, and future architectures are developed collaboratively at OpenHW.

The collaboration hub for open silicon
Industry, Academia, and the Developer Community work together on shared CPU innovation.

The path from open IP to real silicon
OpenHW designs power research platforms, silicon tapeouts, and commercial products.

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Thank you

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