FlooNoC-QoS: Enhancing a RISC-V-based FPGA Overlay with an AXI4-compliant NoC featuring QoS Control Capability

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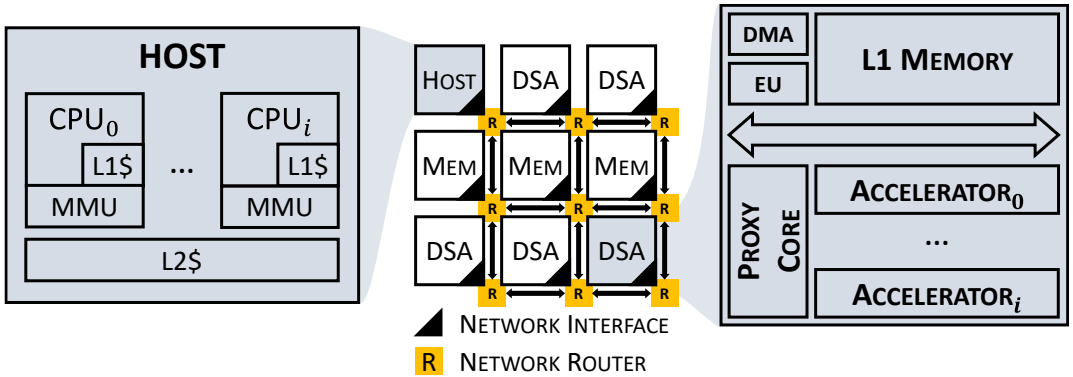
Motivation and Problem Identification

- **HETEROGENOUS SYSTEMS-ON-CHIP (HESOCS):**
  - General-purpose processor (HOST): programmability, legacy SW
  - Domain-Specific Accelerators (DSAs): high performance, energy efficiency
  - Memory subsystem (MEM): *shared*, distributed
  - **NETWORK-ON-CHIP (NOC)**: system scalability, high bandwidth
- **REAL-TIME APPLICATIONS** impose strict requirements for **timing predictability**:
  - **Memory sharing interference**: *unpredictable timing behaviour*
  - **Memory-intensive workloads**: *high latency* toward the off-chip memory
  - **Heterogeneous traffic**: HOST (cache-line sized) vs. DSA (bulk transfers)



About FLOONOC-QOS

- Based on **FLOONOC**, part of the open-source PULP PLATFORM
- *Wormhole NoC fabric* with multiple physical channels (w/o virtual links)
- *Full **AXI4** compliance*:
  - Decoupled link-level protocol (flit-based) for better scalability
  - Support of **multiple burst-based outstanding transactions**
  - Streamlined on-chip integration of heterogeneous components
- QOS CONTROL: *memory bandwidth regulation (monitoring + throttling)*
- Implementation: **FPGA** (focus of this work), ASIC

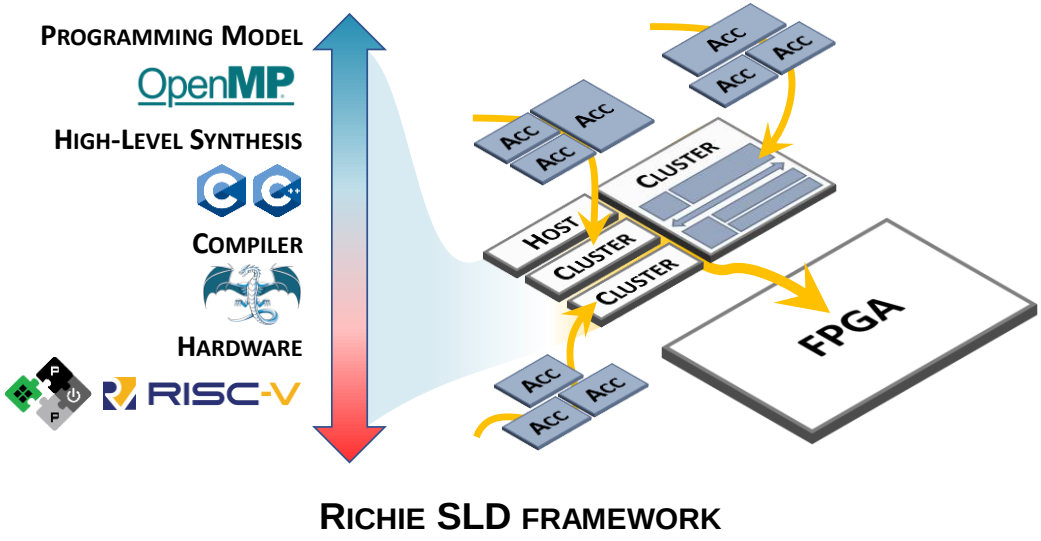
T. Fischer et al., "FlooNoC: A 645 Gbps/link 0.15 pJ/B/hop Open-Source NoC with Wide Physical Links and End-to-End AXI4 Parallel Multi-Stream Support"

FLOONOC
Fully AXI4 NoC implementation

Preliminary results

- Porting of *2D mesh* to COTS FPGA-based HeSoC (**ZU9EG, fck=100MHz**):
  - *Integration and deployment* exploiting the **RICHIE SLD FRAMEWORK** (under review)
  - *Full-stack emulation* of a **RISC-V-based FPGA overlay**

G. Bellocchi et al., "A RISC-V-based FPGA Overlay to Simplify Embedded Accelerator Deployment"

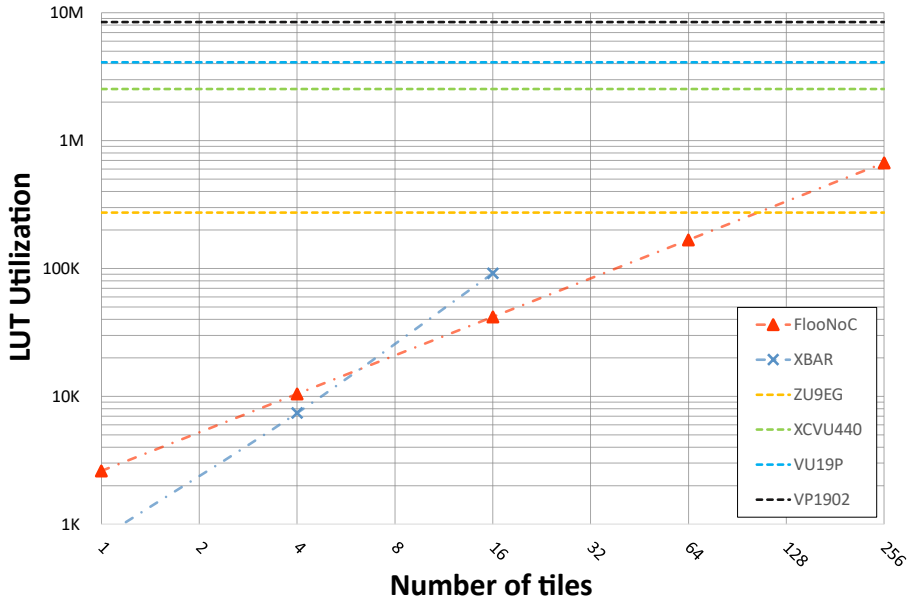


RICHIE SLD FRAMEWORK

RICHIE
SLD framework for
RISC-V-based HeSoCs

Preliminary results

- Characterization of *FPGA resource utilization* (LUT, FF):
  - NoC more beneficial over FPGA-optimized XBAR when $N_{tiles} \geq 7$



Conclusions and Future Works

- Investigation *of flexible and runtime configurable* **QoS MECHANISMS**:
  - **Master-controlled**: tightly-coupled monitoring and throttling

    G. Valente et al., "Fine-Grained QoS Control via Tightly-Coupled Bandwidth Monitoring and Regulation for FPGA-based Heterogeneous SoCs"

  - **Network-controlled**: fragmentation of outstanding transactions

    T. Benz et al., "AXI-REALM: A Lightweight and Modular Interconnect Extension for Traffic Regulation and Monitoring of Heterogeneous Real-Time SoCs"

- Design of massively-parallel HeSoCs—accelerator-rich and many-core—for *safety-critical real-time platforms*, e.g., autonomous cars and robots

FLOONOC
Fully AXI4 NoC implementation

RICHIE
SLD framework for RISC-V-based HeSoCs

PULP
HW/SW exosystem of RISC-V-based IPs

Q&A

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