34 mm² **End-to-End Open-Source** 64-bit **Linux-Capable** RISC-V SoC in 130nm BiCMOS

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Motivation

Open-source as enabler

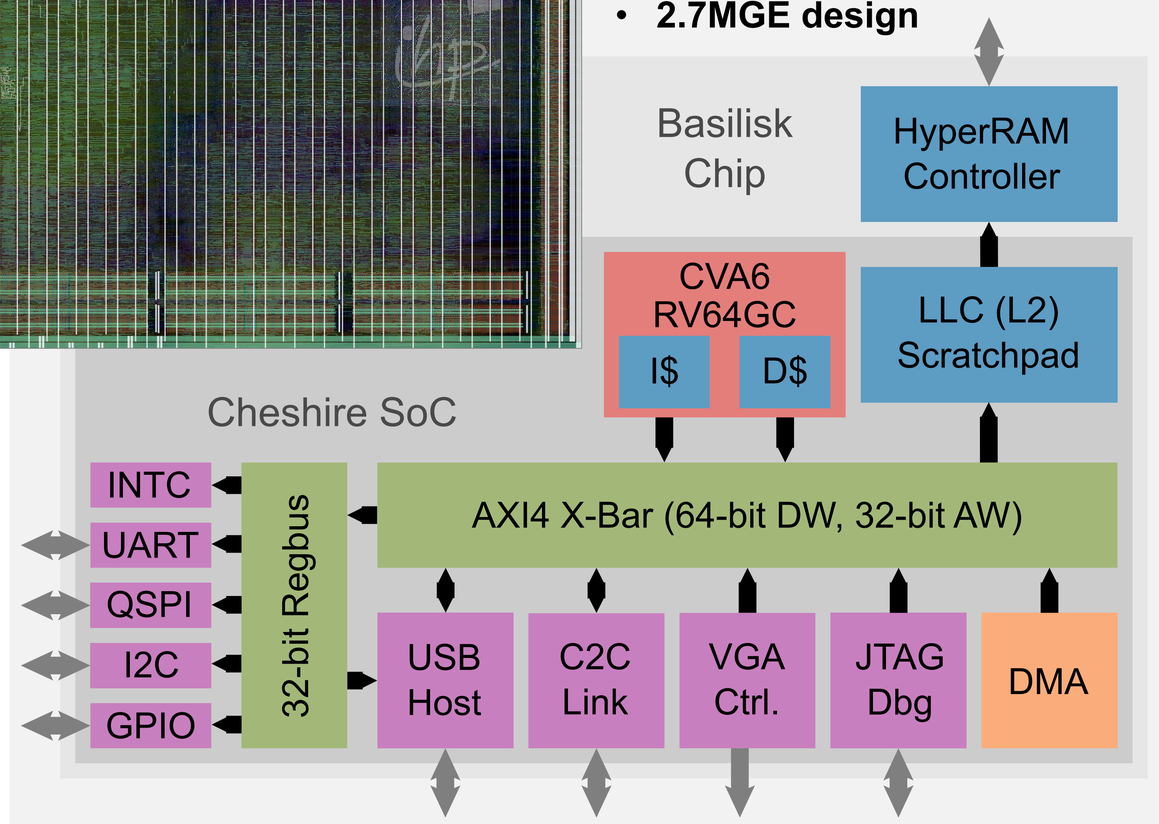
- **Academia:** NDA-free collaboration on designs and tools
- **Education:** Widely accessible hands-on chip design
- **Industry:** Zero-trust verification, license-free deployment

Explore feasibility for larger Linux-capable SoCs

- **Previously:** OS EDA tools used for tapeout of small designs
- **Now:** 4.8× larger than largest previously published design
- **Novelty:** Significant improvements in QoR and performance of open-source EDA tools and flow

Our Design

- 4-way 16KiB L1I and L1D
- 64KiB LLC/Scratchpad
- **Hyperbus DRAM** (124MB/s)
- **2.7MGE design**



End-to-End Open-Source EDA flow

RTL written by PULP (Cheshire, AXI, ...), OpenTitan (SPI, I2C) and OpenHW (CVA6 core)

Yosys-Slang: Newly developed frontend

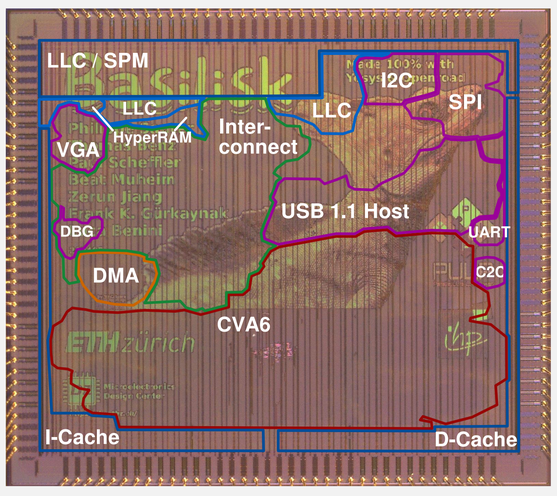
- Supports industry-grade SystemVerilog

Improved Yosys synthesis

- Lazy man's synthesis for high effort optimization
- Improved bit-select operator to multiplexer mapping
- Optimized critical multiply-add implementation
- **Improved timing (2.3×), area (1.6×) and runtime (2.5×) vs reference open-source flow**
- 51 logic level **critical path: Competitive** with 46 LL in previous commercial implementations

Tuned backend: -12% die area vs open reference flow

- Based on OpenROAD-flow-scripts flow
- Flow and Hyperparameters **tuned to design**
  - Strength of routing driven placement
  - Per-layer routing resource reduction
  - Per-module density reduction via cell padding

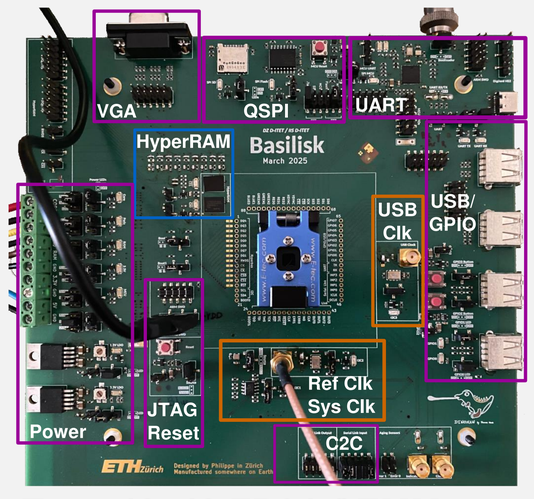


Yosys New Frontend / Synthesis

OpenROAD Place & Route

KLayout GDS Editing

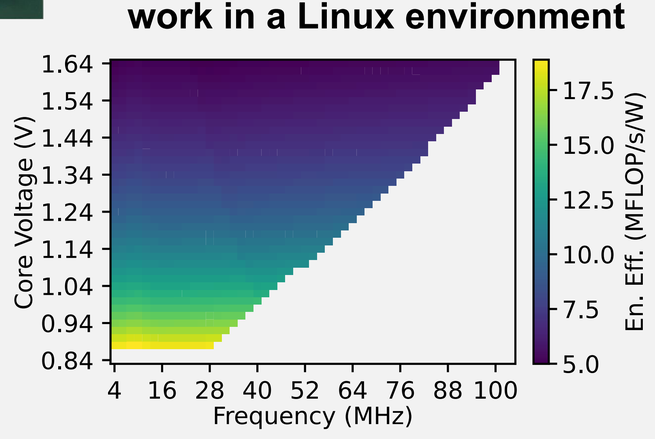
Silicon Testing on Demo Board



- PCB designed in open-source PCB EDA **KiCAD**
- Autonomous boot selection
- Open-source **framework to orchestrate** stimuli application and **measurement**
- On-board configurable clock
- All peripherals (VGA, USB…) **work in a Linux environment**

Test: 48x48 FP64 GEMM

- **62 MHz** at nominal **1.2V** matching OpenROAD timing analysis
- **102 MHz peak** frequency (1.64V)
- Peak efficiency of **18.9 MFLOP/s/W**



Conclusion

- First end-to-end permissive, free and open-source **Linux-capable SoC** with an **application-class** core and **rich peripherals**
- Newly developed **Yosys-Slang** enables synthesis of complex, **industry-grade SystemVerilog** RTL
- **Reproducible** and **sharable** high-quality designs for collaboration and research