ETH zürich

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

vCLIC: Towards Fast Interrupt Handling in Virtualized RISC-V Mixed-criticality Systems

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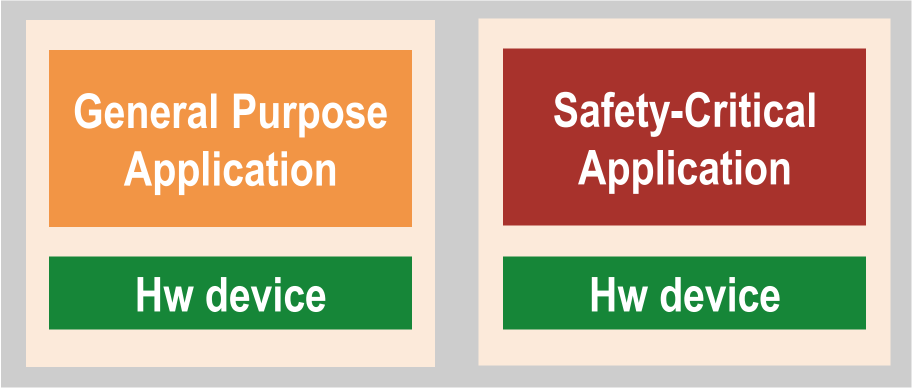
Motivation

- **MCS integrate applications with different criticality levels**
  - Widely spread (e.g., automotive, space)
  - Modern MCS have high computational demands (e.g. autonomous driving cars)
  - **Challenges**: scalability, cost, connectivity of 100s of components



Partitioned MCS

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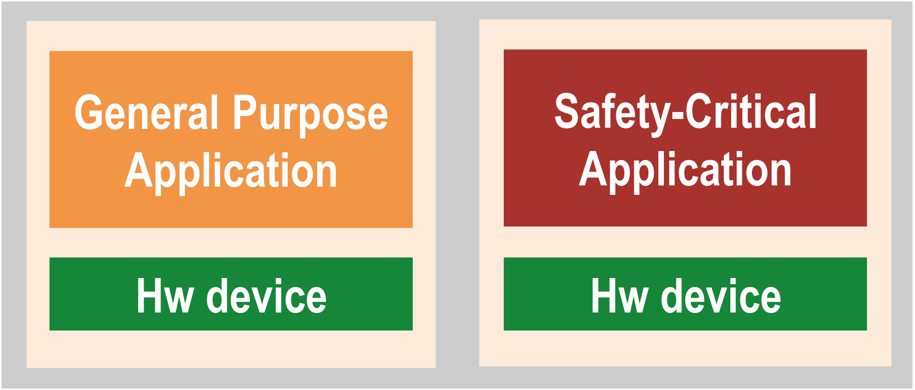
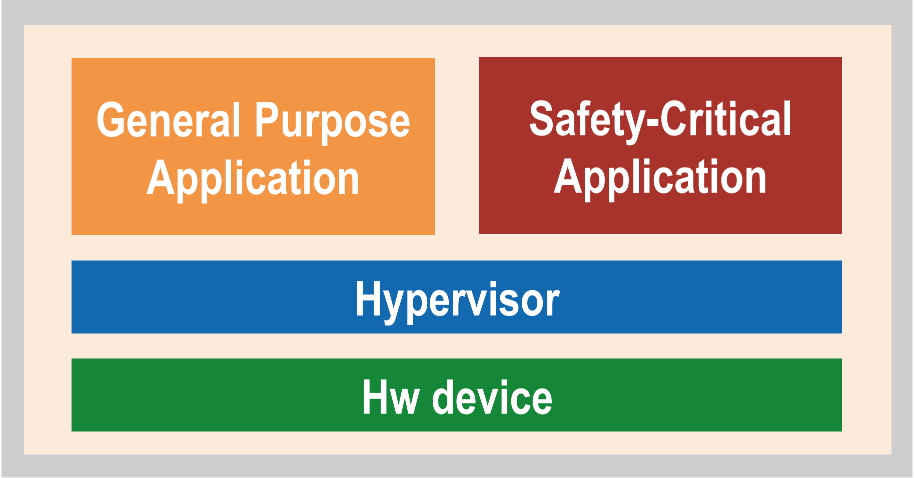


Partitioned MCS

- ***Virtualization* is key**
  - Improves efficiency by sharing hardware resources
  - Hardware support required to reduce performance overhead
  - **Challenges**: isolation, **real-rime responsiveness**



Virtualized MCS

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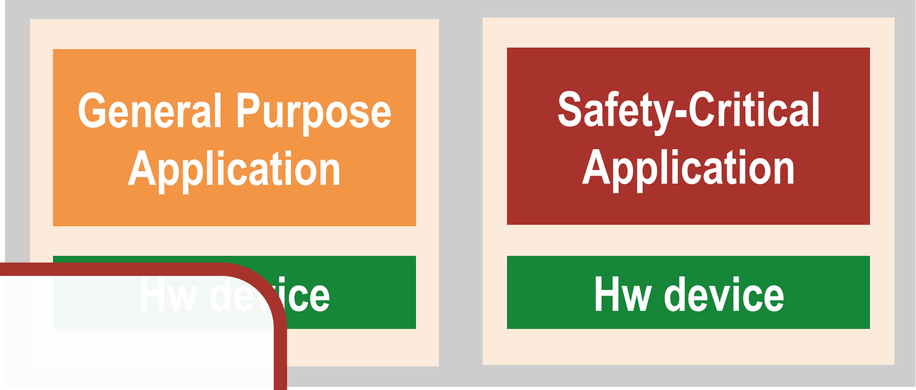
Research Question

How to guarantee real-time **responsiveness** of **safety-critical** components in **virtualized MCS**?



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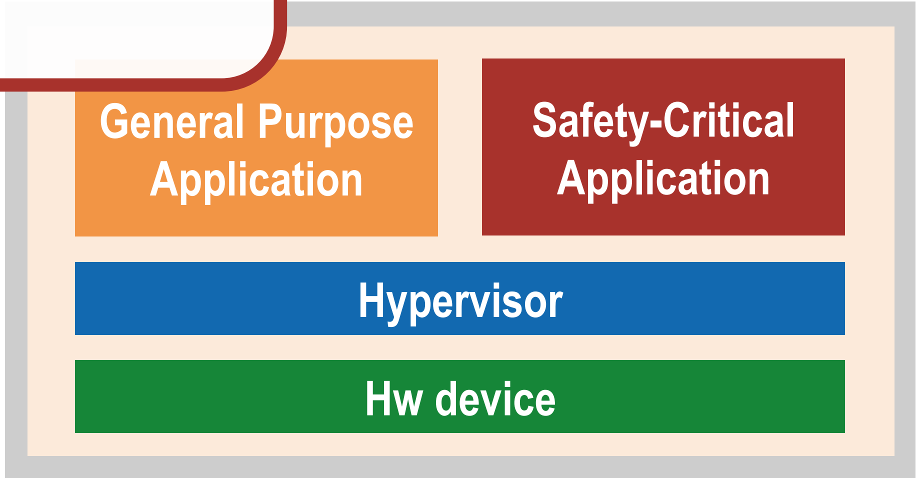
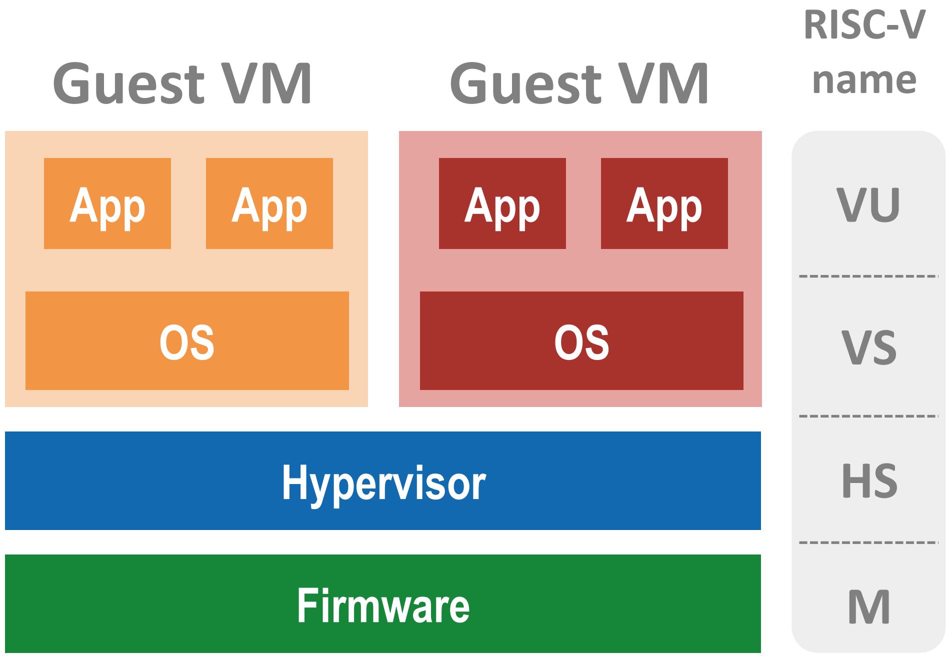


Virtualized MCS

Background

- **RISC-V Mixed-Criticality Systems**
  - Open, modular ISA with wide range of applications
  - Supports virtualization through dedicated **Hypervisor extension**
  - Drives research in safety, security, real-time processing



RISC-V Privilege Modes

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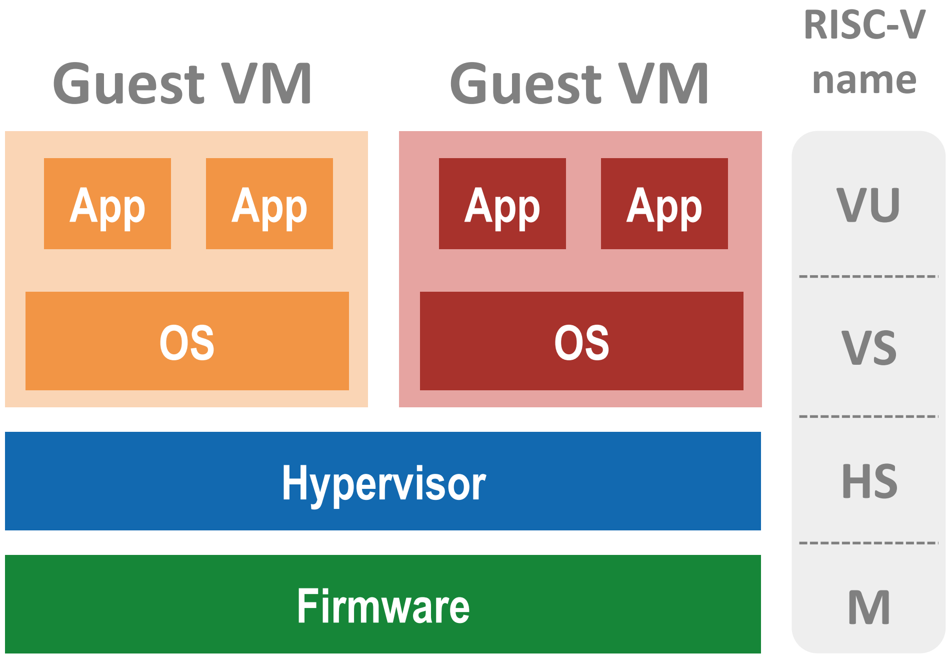
- **Interrupt virtualization**
  - Extends *hardware support* for virtualization to interrupt controller
  - Enables direct injection of interrupts to VMs
  - Reduces **interrupt latency** by minimizing hypervisor intervention



RISC-V Privilege Modes

RISC-V Interrupt Controllers

	Designed for Real-time	Supports Virtualization
RISC-V base interrupt architecture [1] • Original spec of interrupt • Core-local + platform-level interrupt controllers	✗	✗

[1] RISC-V Privileged Specification
[2] RISC-V AIA Specification
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RISC-V fast-interrupts (CLIC) • Designed for fast interrupt response • Interrupt vectoring, nesting, tail-chaining	✓	✗

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Our Work: vCLIC “Enable fast interrupt response in RISC-V virtualized MCS”	✓	✓

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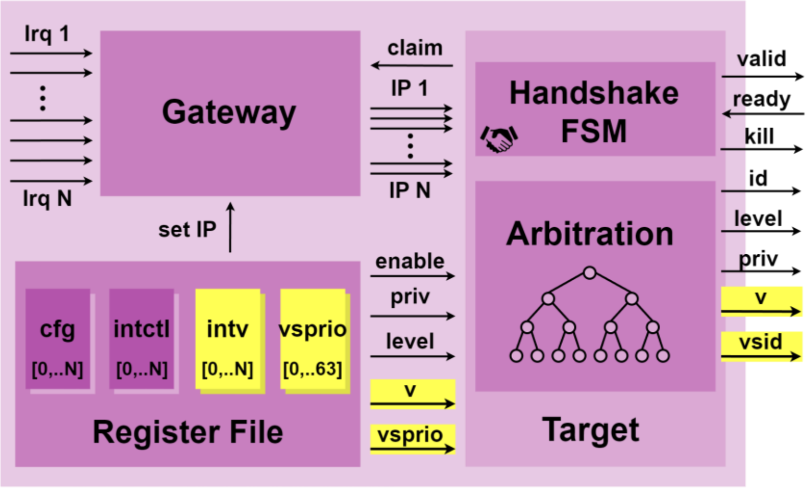
vCLIC: design and architecture

- **Design principles**
  - **Modularity**
    - *VSCLIC*: direct injection of interrupts
    - *VSPRIO*: prioritization based on VM criticality
  - **Configurability**
    - Fine-grained tuning of resource utilization
  - **Compatibility**
    - Minimal deviation from CLIC spec*



vCLIC

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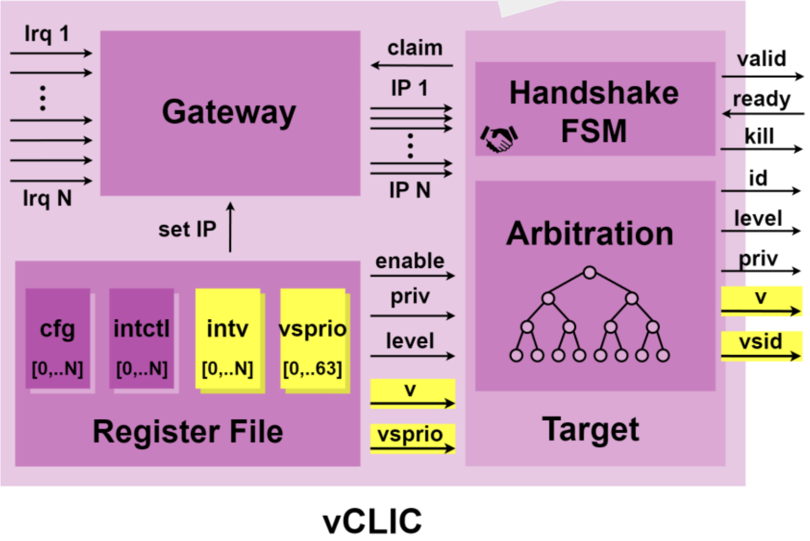
RTL available open-source



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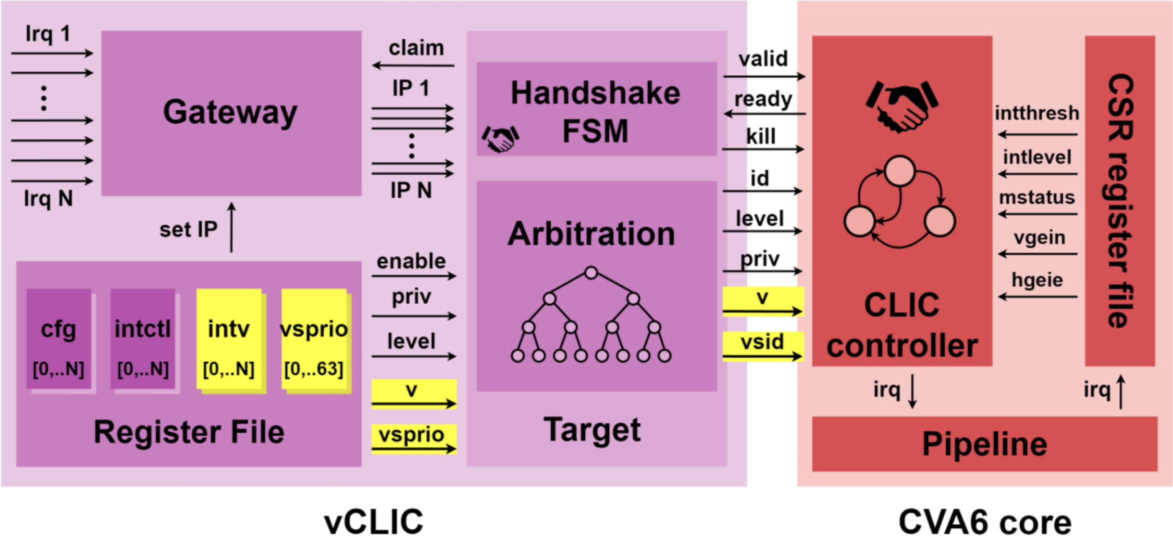

- **System integration**
  - Coupled to CVA6 core
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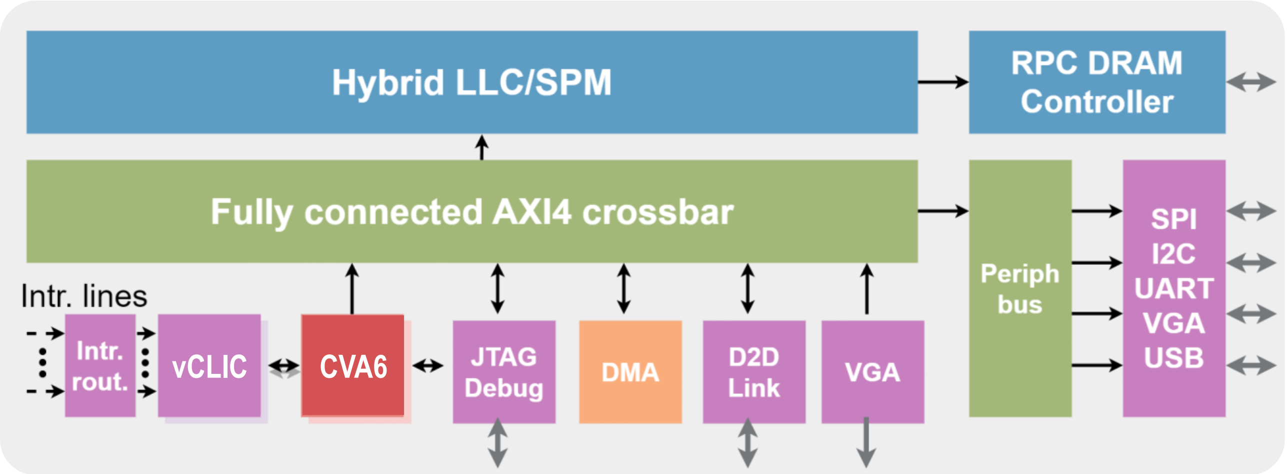
Cheshire SoC



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- **Software stack**
  - OpenSBI firmware
  - *Bao hypervisor* [1], *Xvisor* [2]
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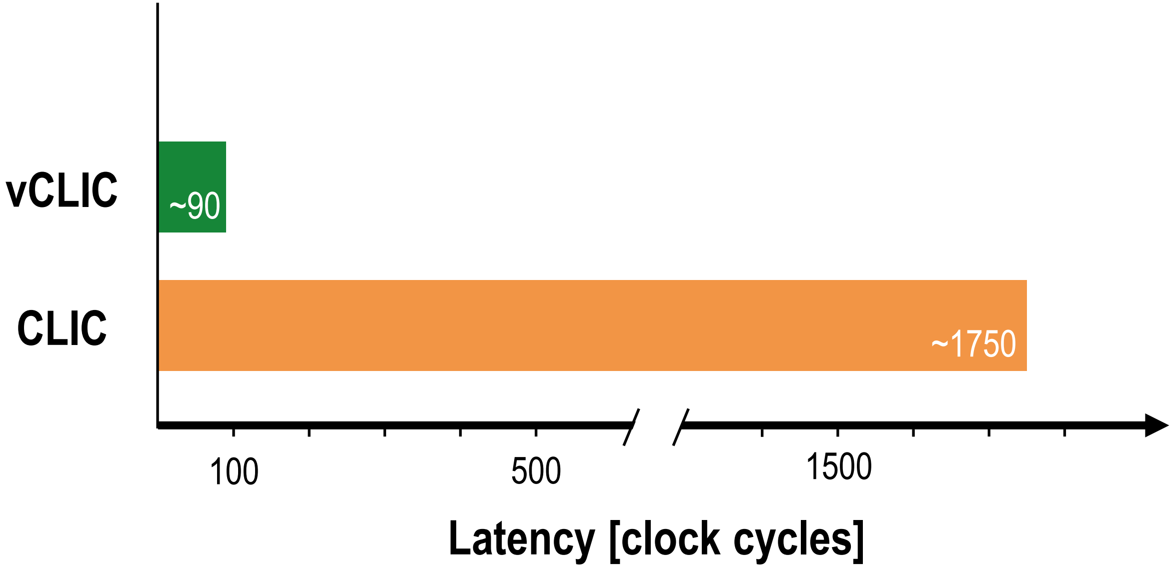

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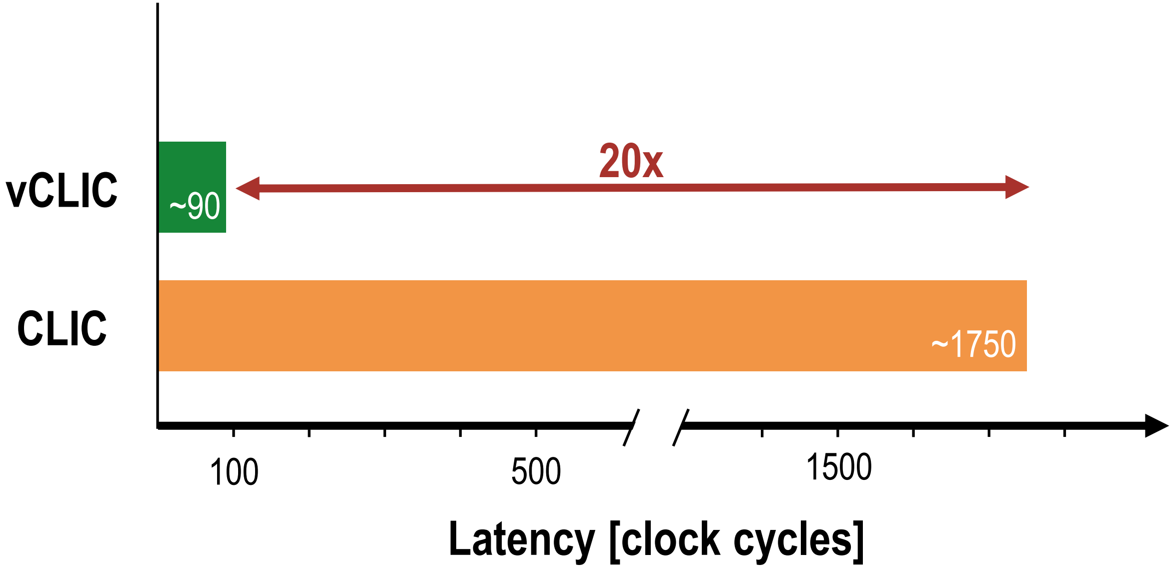

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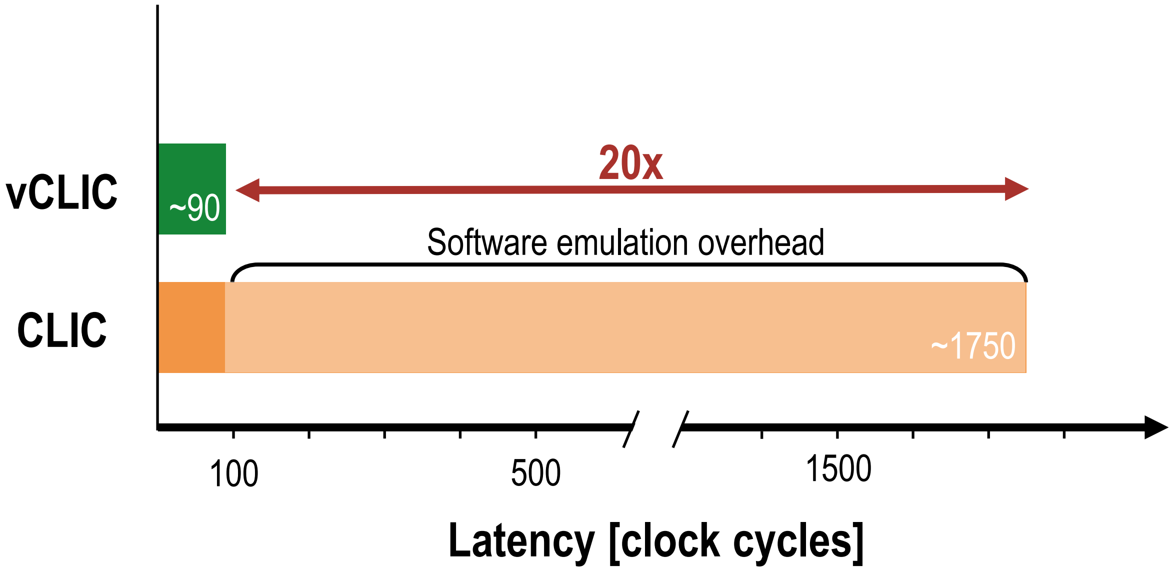

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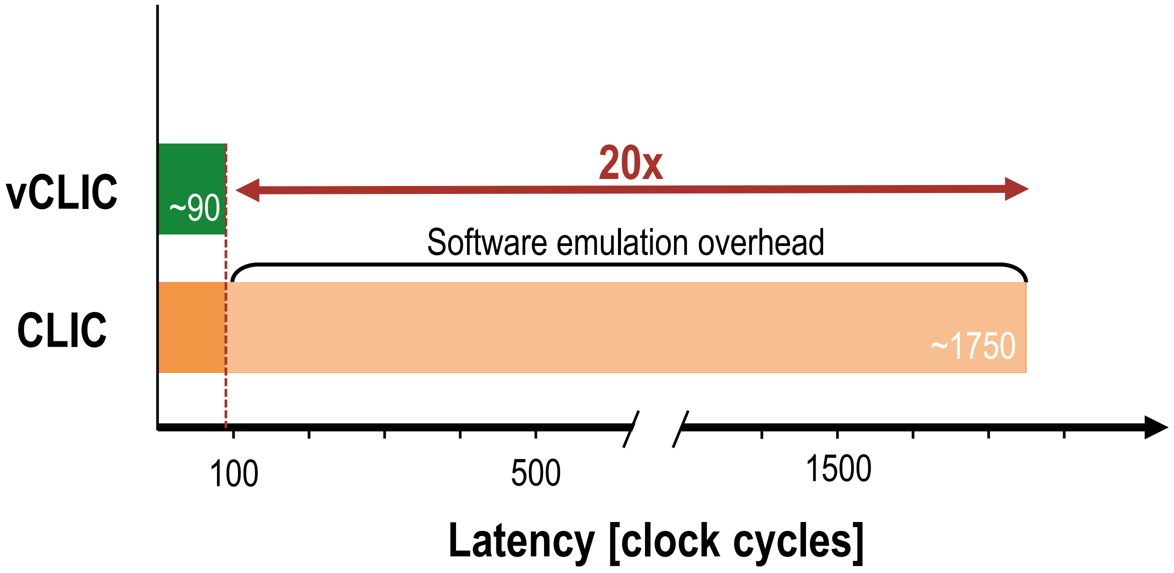

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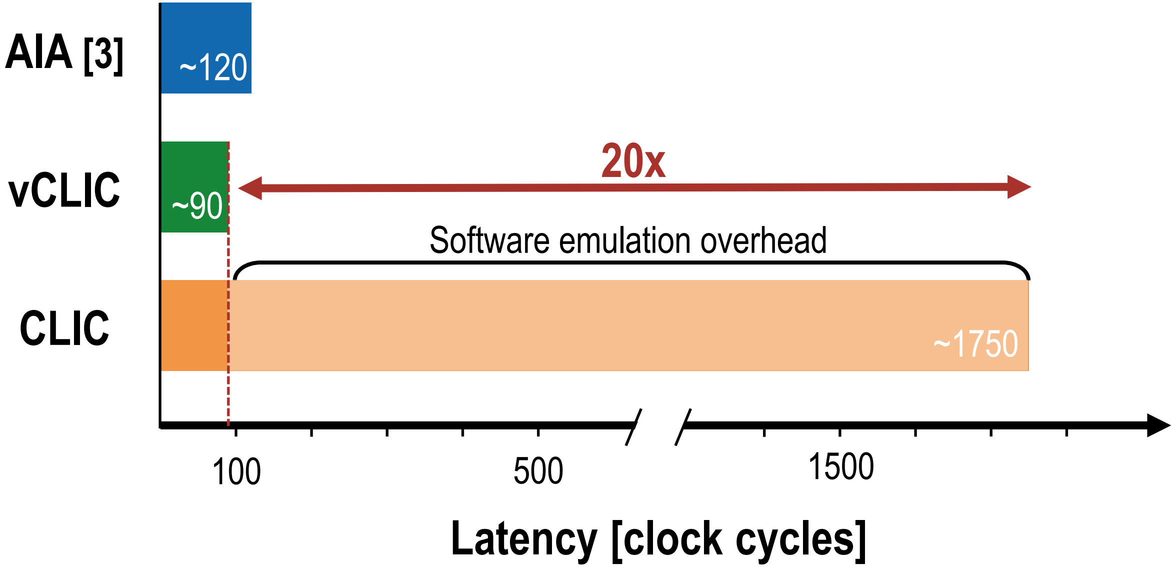

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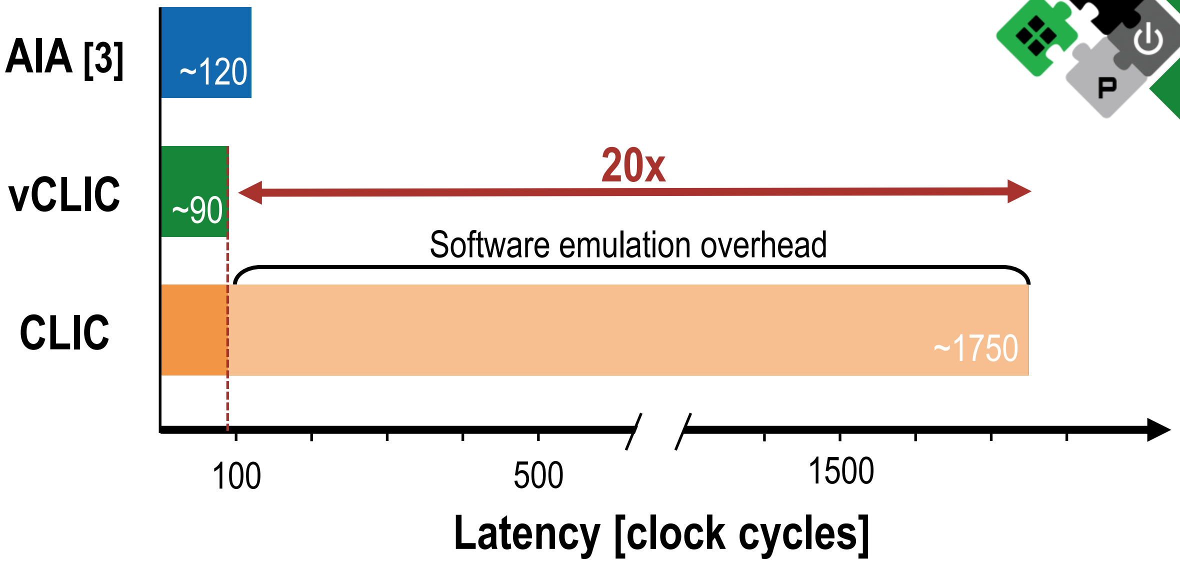

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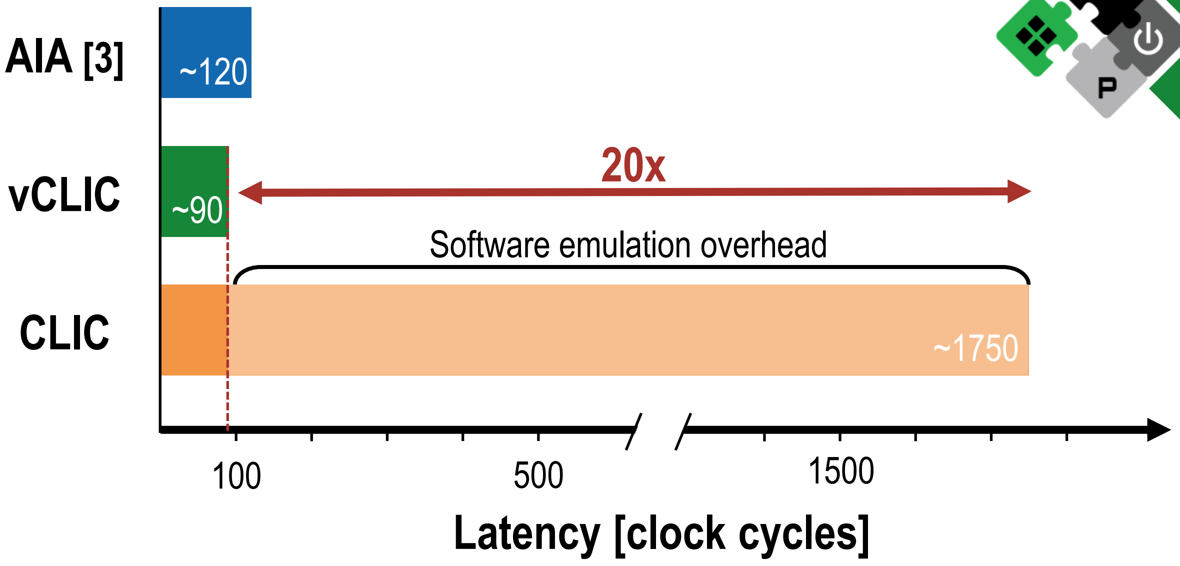
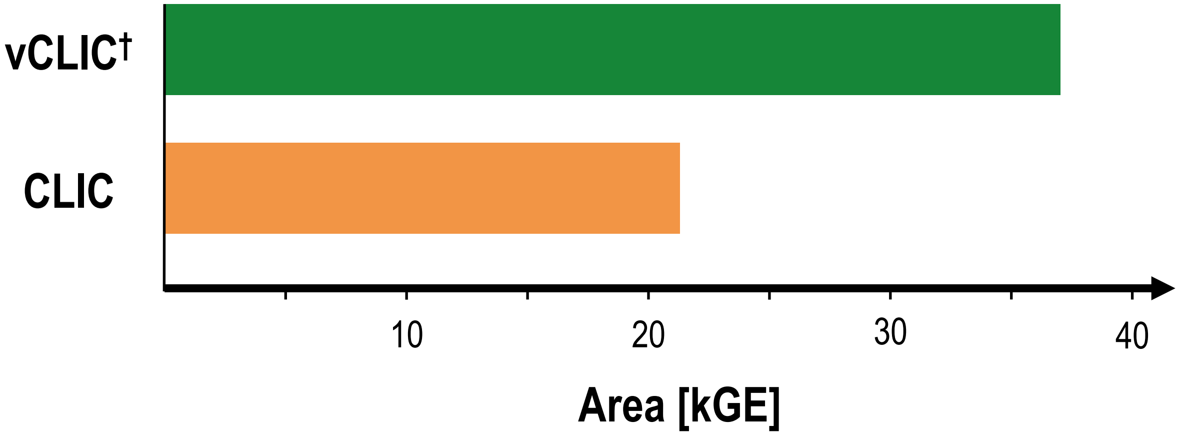
  - Minimal area overhead (**<20kGE**)
  - Iso-frequency with existing CLIC (>1GHz)





* Implemented in 16nm Intel technology

† Configuration: VSCLIC + VSPRIO bits = 1

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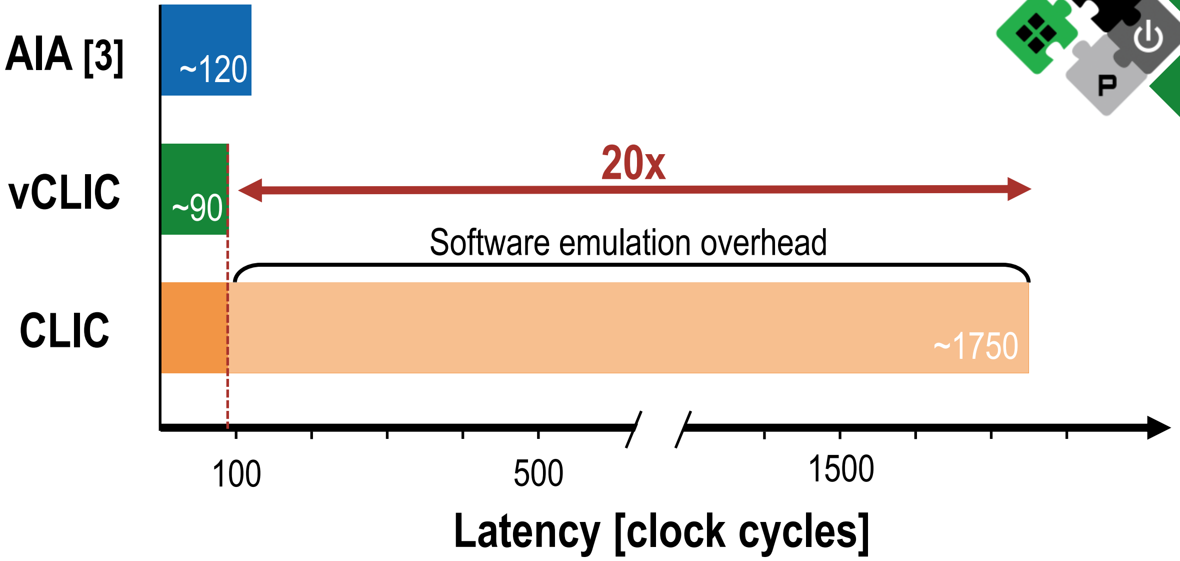

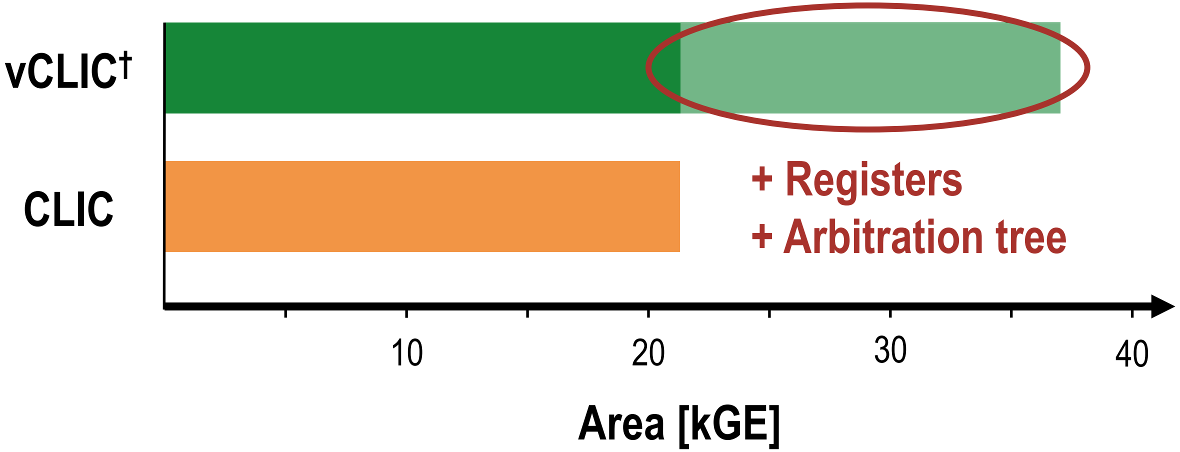

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Conclusion

- **We propose vCLIC:**
  - Virtualization extension of CLIC
  - Up to **20x** reduced interrupt latency wrt software emulation
  - Limited area cost (<20kGE)
  - First RISC-V interrupt controller designed for fast-interrupt response in virtualized systems

Our work is open-source at:

https://github.com/pulp-platform/clic

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Q&A

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