Trikarenos

A Fault-Tolerant RISC-V-based Microcontroller for CubeSats in 28nm

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PULP Platform
Open Source Hardware, the way it should be!
CubeSats & Micro Satellites

- Small satellites becoming more popular
- Very low power envelope
- Increasing processing requirements
- Existing space-ready processors based on old technologies

Source: https://www.esa.int/var/esa/storage/images/esa_multimedia/images/2016/04/cubesats_orbiting_earth/15950521-1-eng-GB/CubeSats_orbiting_Earth.jpg

Leverage modern, open-source Microcontroller SoC!
Open-Source Microcontroller – PULPissimo

This is the top-level project for the PULPissimo Platform. It instantiates a PULPissimo open-source system with a PULP SoC domain, but no cluster.

View license

294 stars 136 forks

Citing

If you are using the PULPissimo IPs for an academic publication, please cite the following paper:

@inproceedings{RSV04,
  author={Rogenmoser, Michael and Simecek, Christian and Rossell, Antonio and Vescovi, Paolo},
  title={PULPissimo: an Ultra-Low-Power PULP Microcontroller SoC in 22nm FDX2},
  year={2014},
  pages={t-0},
  doi={10.1109/S3ES.2014.6859743})

PULPissimo is the microcontroller architecture of the more recent PULP chips, part of the ongoing “PULP platform” collaboration between ETH Zurich and the University of Bologna – started in 2013.

github.com/pulp-platform/pulpissimo
PULPissimo Architecture

- Memory Bank
- Memory Bank
- Memory Bank
- Memory Bank
- Memory Bank
- Memory Bank

- Tightly Coupled Data Memory Interconnect

- JTAG
- SPI
- I^2C
- UART
- SDIO

- \( \mu \)DMA

- Peripheral Interconnect

- SoC Control
- Timer
- GPIO
- Debug
How do we tackle reliability of the RISC-V core?
Reliable Processing Cores

- Replicate Core
  → Triple-Core Lockstep
- Identical Inputs
- Voted Outputs
  - Directly connects any soft error
- Configurable for performance if reliability is not needed
  - 2.96x speedup
Software Recovery of Triple Modular Redundant Cores

- Radiation causes soft-error
- Error detected by voter
- Core state (RF, PC, CSRs) stored to memory
  - Corrected by voter
- Core state loaded back into cores
- Total procedure in ~600 cycles
Trikarenos – PULPissimo with Reliability

- Memory Bank
- Memory Bank
- Memory Bank
- Memory Bank
- Memory Bank
- Memory Bank

- JTAG
- SPI
- I²C
- UART
- SDIO

- μDMA

- RISC-V Core
- RISC-V Core
- RISC-V Core

- Interrupt Control

- Peripheral Interconnect

- SoC Control
- Timer
- GPIO
- Debug
How do we tackle reliability of the System Memory?
Byte-addressable Memory – ECC Load and Store

Byte Store

Byte Store with ECC
ECC Load-and-Store – Performance Impact

- 32-bit Hsiao ECC word protection
- Directly grant storage
  - Delay following transaction, not current transaction, to shift & reduce impact
- Results: <1% cycle increase
  - Various tests, such as 8-bit Matrix-Matrix Multiplication
ECC Scrubber

- Multiple errors in a single word lead to unrecoverable errors
- Scan Memory Bank
- Re-write faulty word if error is detected
- Defer permission to external accesses
- Log all corrections (and uncorrectable words)
Trikarenos – PULPissimo with Reliability
Trikarenos – ASIC implementation

- TSMC 28HPC+
  - Shown to have high TID tolerance
- 2 mm² @ 250 MHz
- 3 separate Ibex cores
- 256 KiB Memory in 8 word-interleaved banks
Internal structure

• Spatially separated cores with a keepout zone

• Legend:

- Red: Cores
- Pink: HMR Unit
- Blue: Memory (w/ ECC en-/decode)
- Green: Interconnect
- Brown: Debugger
- Orange: Logging & control registers, ROM, ...
- Light green: I/O
Power Consumption at max Frequency

- **Core Power [mW]**
  - Parallel Cores
  - Locked Core
  - Single Core
  - Idle

- **Core Voltage [V]**

- **Frequency [MHz]**

- **Locked Core**
  - 3x Core Power

- **Independent Cores**

- **Single Core Active Power**

- **Base Power**

- **Frequency**

- **Power Consumption at max Frequency**

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Efficiency vs. Performance

1.52x Efficiency using only one Core

2.96x Performance & 2.36x Efficiency when running in Parallel

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## How do we compare?

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of Cores</strong></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1(3)/3</td>
</tr>
<tr>
<td><strong>Instruction Set Architecture</strong></td>
<td>SPARC</td>
<td>ARMv7-R</td>
<td>RISC-V</td>
<td>RISC-V</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>0.250µm</td>
<td>180nm</td>
<td>65nm</td>
<td>28nm</td>
</tr>
<tr>
<td><strong>Performance (Dhrystone)</strong></td>
<td>240 DMIPS</td>
<td>90 DMIPS</td>
<td>520 DMIPS</td>
<td>2256 DMIPS</td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>133 MHz</td>
<td>50 MHz</td>
<td>311 MHz</td>
<td>800 MHz</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>5 W*</td>
<td>&lt;400 mW</td>
<td>781.9 mW</td>
<td>15.7 / 19.7 mW</td>
</tr>
<tr>
<td><strong>Efficiency [DMIPS/mW]</strong></td>
<td>-</td>
<td>0.225</td>
<td>0.665</td>
<td>14.3 / 33.8</td>
</tr>
<tr>
<td><strong>Configurable Core</strong></td>
<td>=&gt; 3x core count</td>
<td>=&gt; 2.6x reliable Performance vs. GR716</td>
<td>=&gt; 2.96x Performance</td>
<td></td>
</tr>
</tbody>
</table>

- **63x Efficiency vs. GR716**
- **21.5x (50x) Efficiency vs. ARM TCLS**
Conclusion

• Trikarenos: Efficient, Fault-Tolerant Microcontroller
  • Configurable Triple-Core Lockstep
  • 256 KiB low-latency ECC-protected Memory
  • Peripheral DMA

• Implemented in 28nm
  • Up to 330 MHz @ 32.5 mW

• Runtime Configurable
  • Reliable when needed
  • Performant when possible
Outlook – Radiation tests & SAGE CubeSat

• Currently ongoing: Functional test under radiation
• Future: Integration into demonstration CubeSat
Luca Benini, Alessandro Capotondi, Alessandro Ottaviano, Alessio Burrello, Alfio Di Mauro, Andrea Borghesi, Andrea Cossettini, Andreas Kurth, Angelo Garofalo, Antonio Pullini, Arpan Prasad, Bjoern Forsberg, Corrado Bonfanti, Cristian Cioflan, Daniele Palossi, Davide Rossi, Florian Glaser, Florian Zaruba, Francesco Conti, Georg Rutishauser, Germain Haugou, Gianna Paulin, Giuseppe Tagliavini, Hanna Müller, Luca Bertaccini, Luca Valente, Manuel Eggimann, Manuele Rusci, Marco Guermandi, Matheus Cavalcante, Matteo Perotti, Matteo Spallanzani, Michael Rogenmoser, Moritz Scherer, Moritz Schneider, Nazareno Bruschi, Nils Wistoff, Pasquale Davide Schiavone, Paul Scheffler, Philipp Mayer, Philip Wiese, Robert Balas, Samuel Riedel, Sergio Mazzola, Sergei Vostrikov, Simone Benatti, Stefan Mach, Thomas Benz, Thorir Ingolfsson, Tim Fischer, Victor Javier Kartsch Morinigo, Vlad Niculescu, Xiaying Wang, Yichao Zhang, Frank K. Gürkaynak, all our past collaborators and many more that we forgot to mention