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CVA6-CFI: A First Glance at RISC-V Control-Flow Integrity Extensions

Simone Manoni[*], Emanuele Parisi[‡], Riccardo Tedeschi[*], Davide Rossi[*†], Andrea Acquaviva[*], Andrea Bartolini[*]

[*]*University of Bologna, Italy*

[†]*Fondazione Chips-IT, Italy*

[‡]*Barcelona Supercomputing Center, Spain*

Introduction

- Software security is a first-class concern across the computing stack
  - Cloud & datacenters

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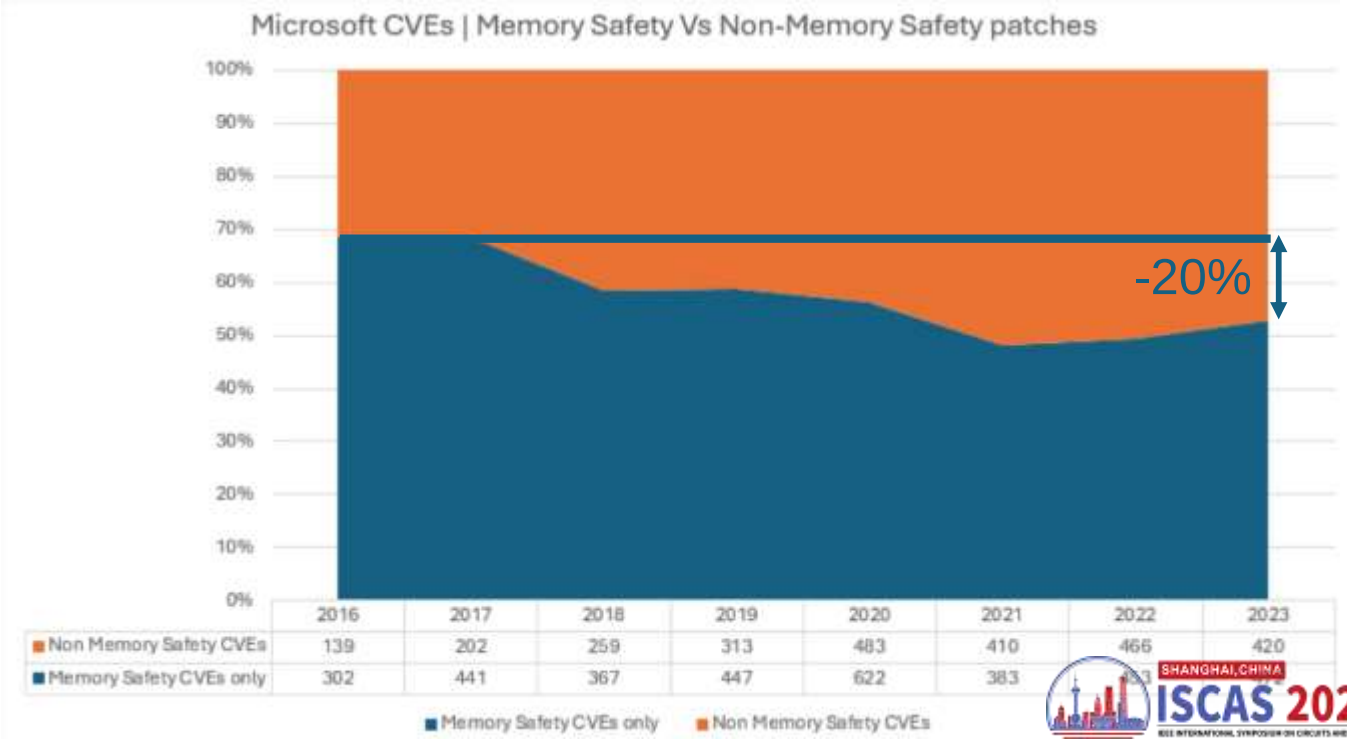
  - Safety-critical CPS (autonomous vehicles, robotics, medical, smart infrastructure)

- A compromise can lead to
  - data leaks
  - service disruption
  - financial loss
  - physical harm

- Yet defenses must fit tight performance, memory, and area budgets

Background: Memory safety

- Memory-safety bugs are the dominant attack vector against C/C++ SoC firmware
- In 2016, 70% of Microsoft *Common Vulnerabilities & Exposures* (CVEs) were memory-safety related
- Despite improvements, ~50% of Microsoft patches in 2023 still address memory-safety issues
- These bugs enable **control-flow hijacking** (code-reuse attacks) [NSA/CISA, 2025]



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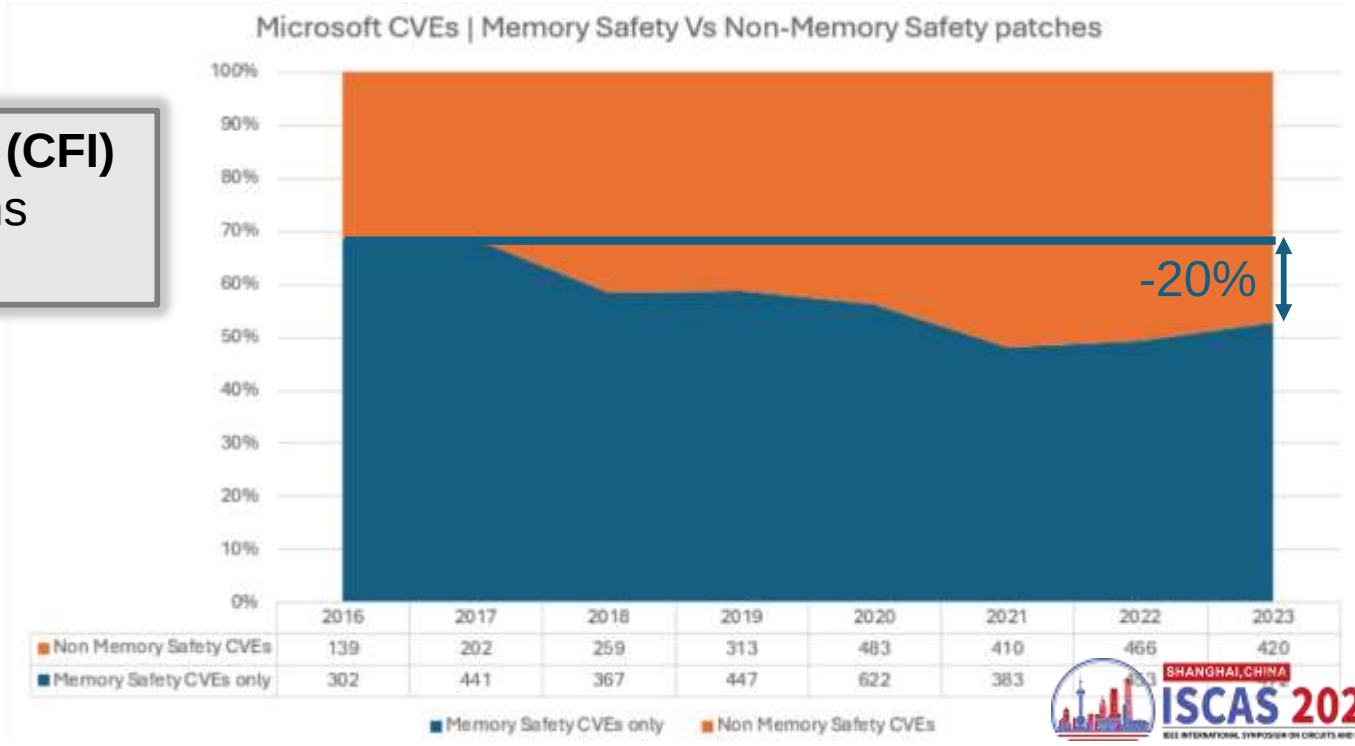
State-of-the-art defense: Control-Flow Integrity (CFI)
- Constrains program execution to legitimate paths
- Blocks code-reuse attacks at their root



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- A program can be represented by a Control-Flow graph (CFG)
  - **Nodes** = Basic blocks
  - **Edges** = Possible Control transfers

- CFI restricts control transfers to **valid edges** in the CFG

```
A: addi  sp, sp, -32
   [...]
   addi  sp, sp, 32
   ret
```

```
B: addi    sp, sp, -32
   [...]
   addi    sp, sp, 32
   ret
```

```
C: addi    sp, sp, -48
   [...]
   jalr    a1
```

```
   sw      a0, -32(s0)
   lw      a0, -28(s0)
   call    A
```

```
   sw      a0, -36(s0)
   [...]
   addi    sp, sp, 48
   ret
```

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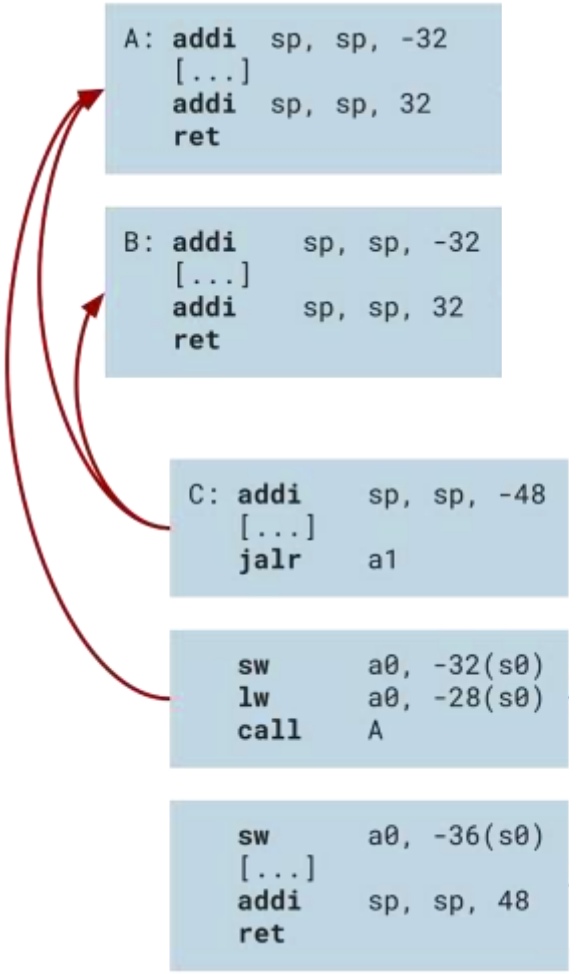
  - Backward edges:
    - Function `ret`
    - Possible protection mechanism: *Shadow Stack*
    - Store a copy of `ret` address in a protected memory region (s. stack)



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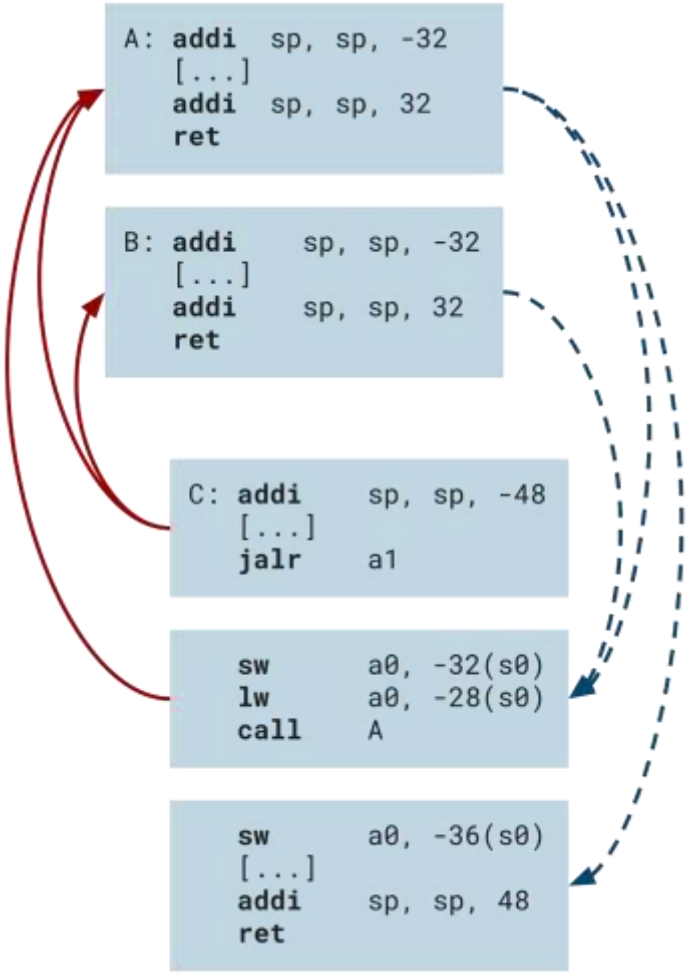
  - Forward edges:
    - Indirect calls and jumps
    - Possible protection mechanism: *Landing pads*
    - Mark valid targets in CFG



Background: CFI commercial solutions

- **Intel Control-flow Enforcement (CET)**
  - Shadow Stack – write protected memory region
  - Indirect Branch Tracking (IBT) – `ENDBRANCH` instr. marks valid indirect-branch targets (similar to LP)

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  - Branch Target Instruction (BTI) - Branch Target Instructions mark valid forward-edge targets

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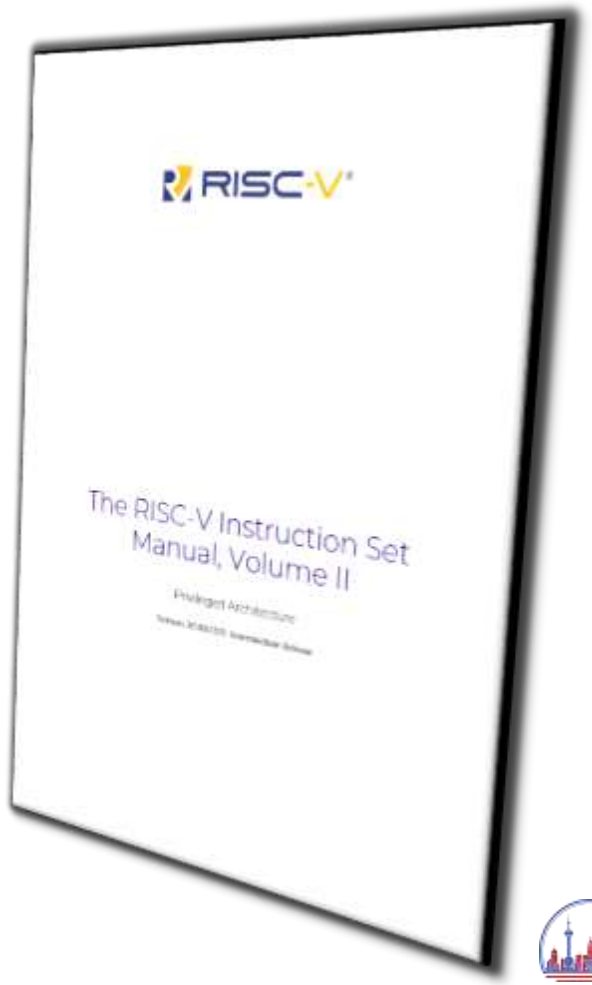
- **IBM POWER10**
  - *hashst* / *hashchk* – cryptographic hash of return address stored alongside stack frame

Background: CFI in RISC-V

- RISC-V: open, royalty-free ISA, modular and extensible by design
- Increasingly adopted: >10 billion cores shipped since launch in 2015
- June 2024, Unprivileged ISA release
  - CFI ISA extensions ratified
    - *Zicfiss – Shadow Stack*
    - *Zicfilp – Landing Pads*



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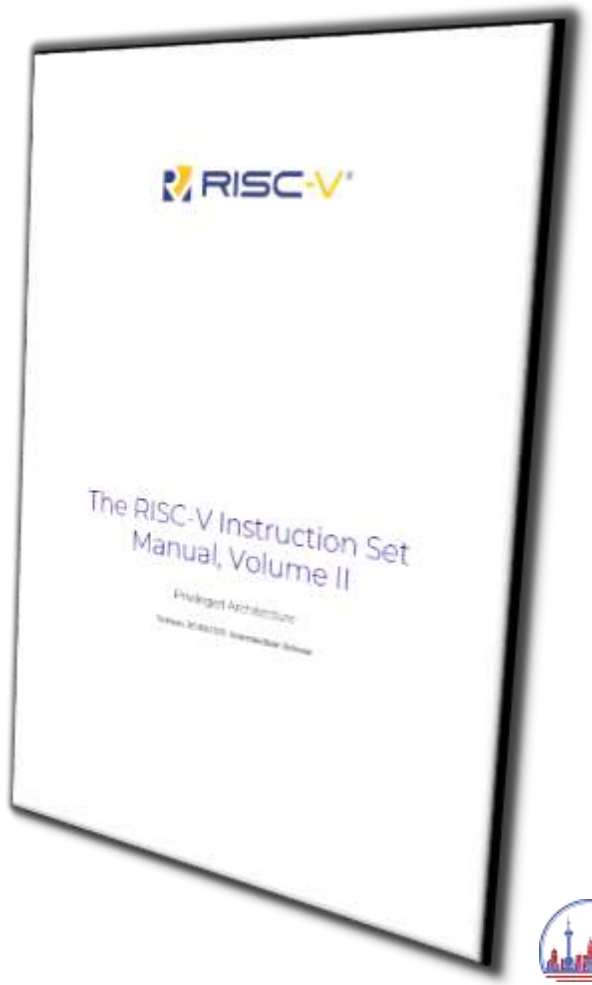
What's missing
- Microarchitectural impact has never been evaluated
- No existing implementation of the CFI spec for RISC-V



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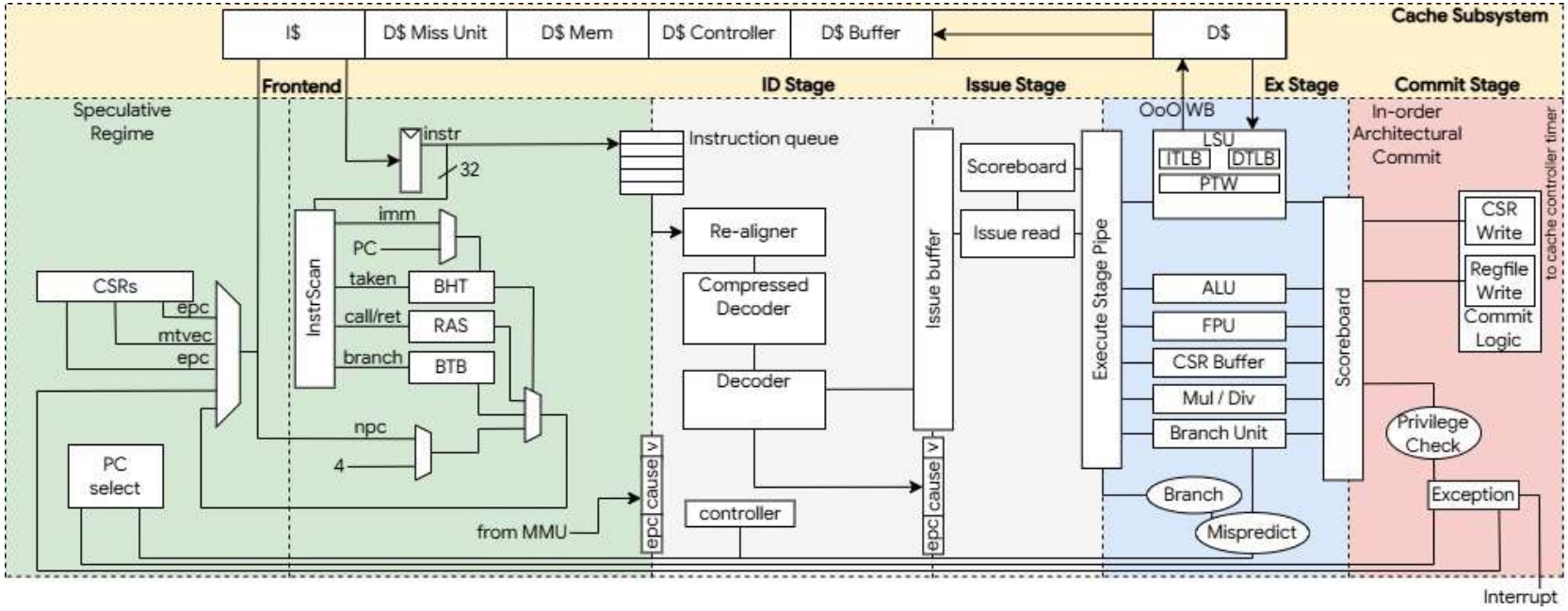
Our contribution:

- The first implementation and evaluation of the RISC-V CFI ISA extension on an application-class, open-source CPU

CVA6-CFI

- Implementation & evaluation CFI ISA Extension on CVA6 [1]
  - Open-source
  - RV64, 6-stage, in-order, single-issue CPU



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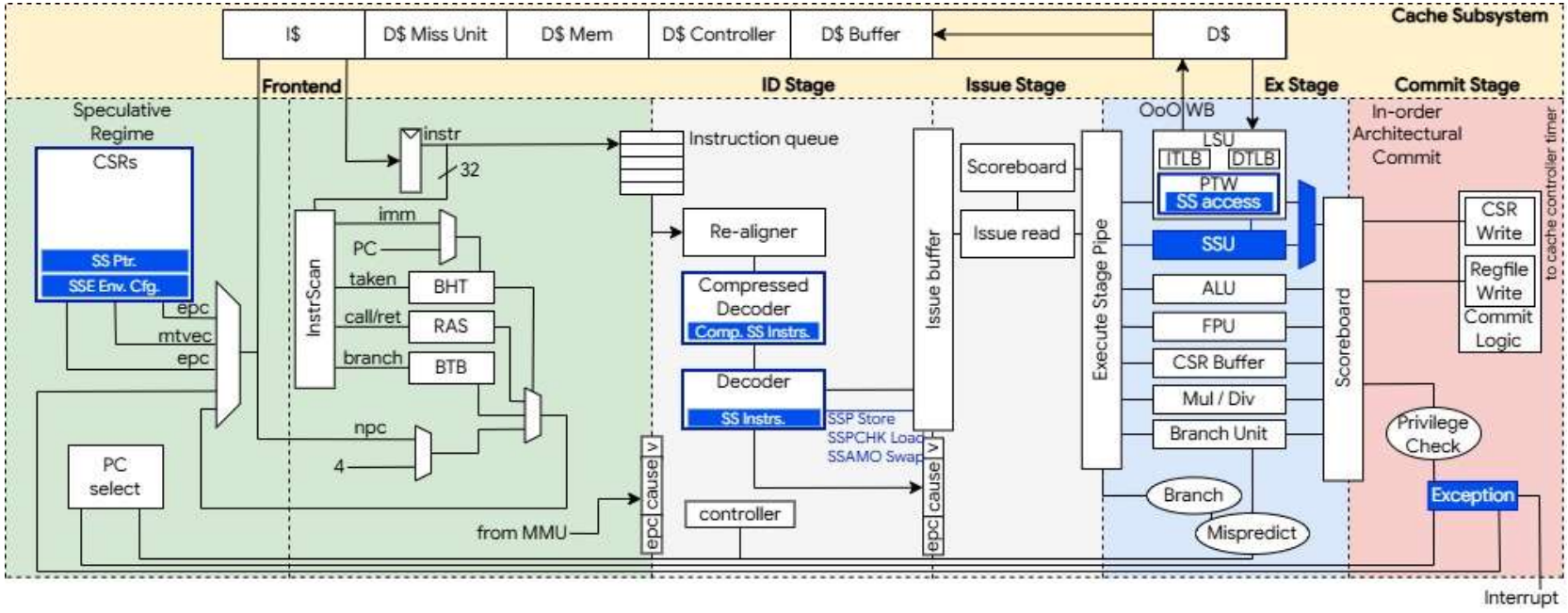

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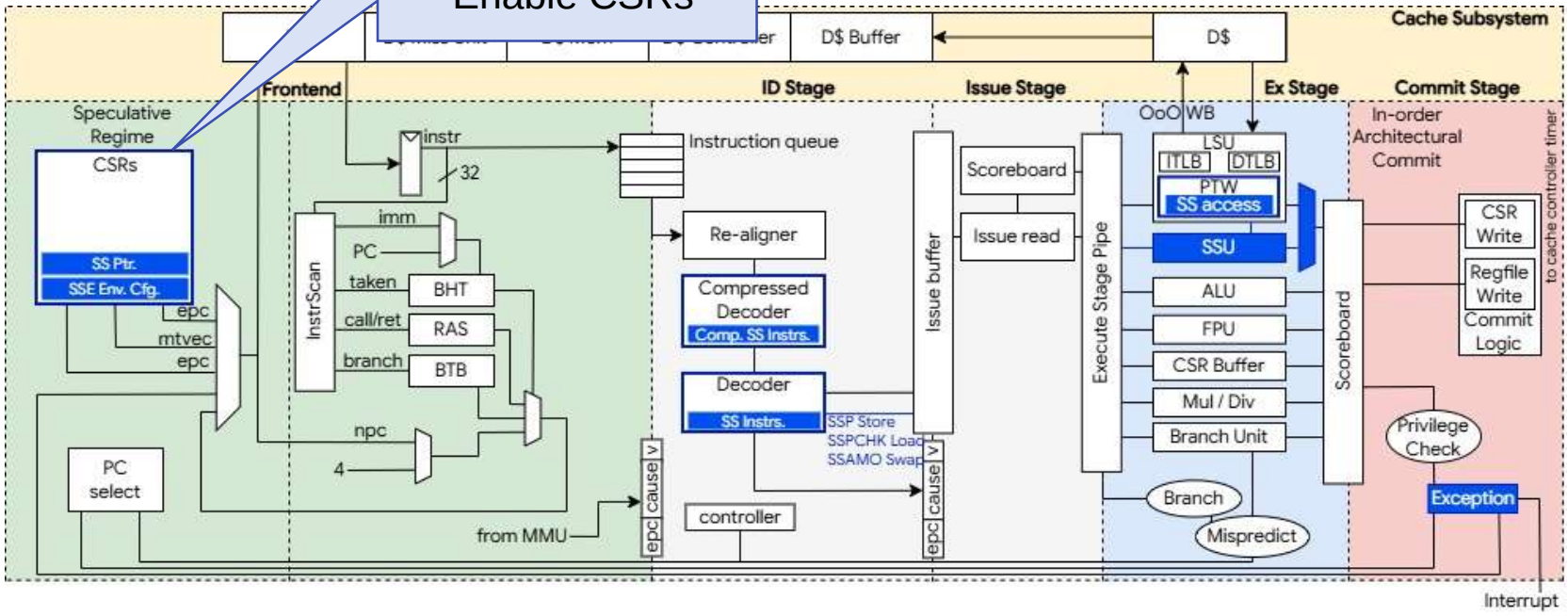
- **Shadow Stack Pointer** CSR
- Shadow Stack Enable CSRs



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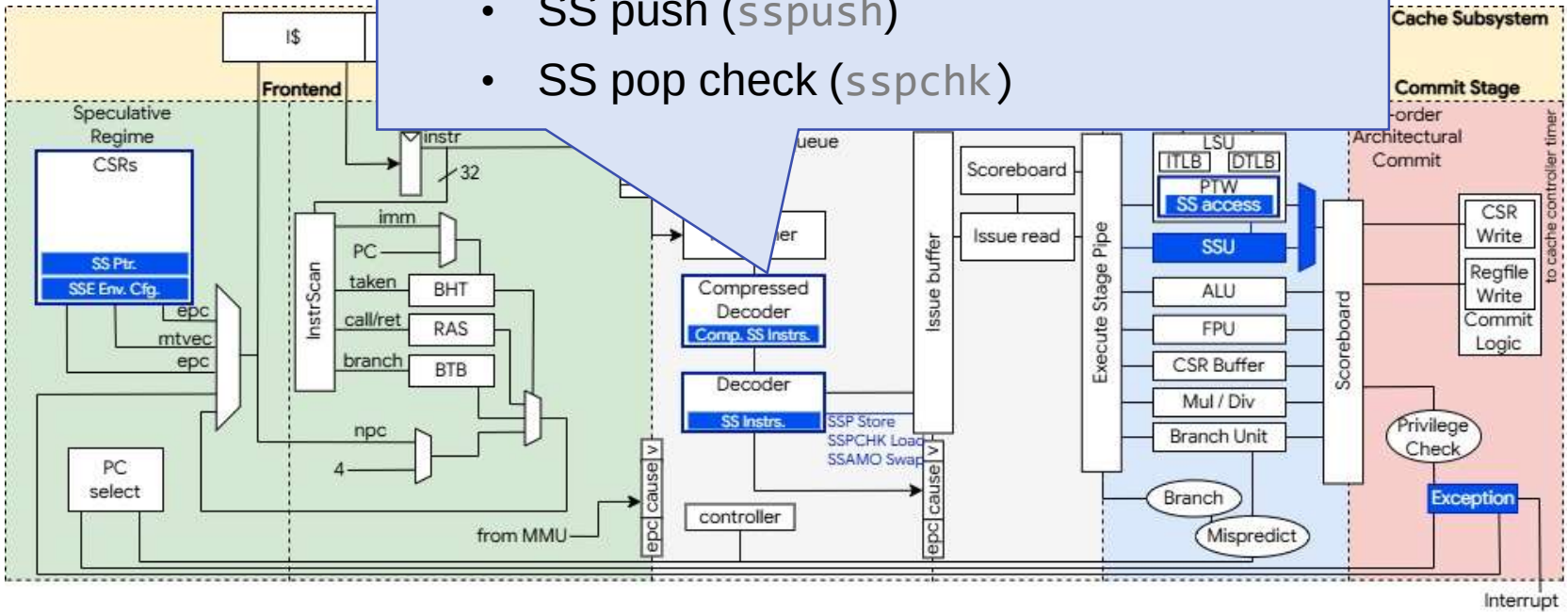

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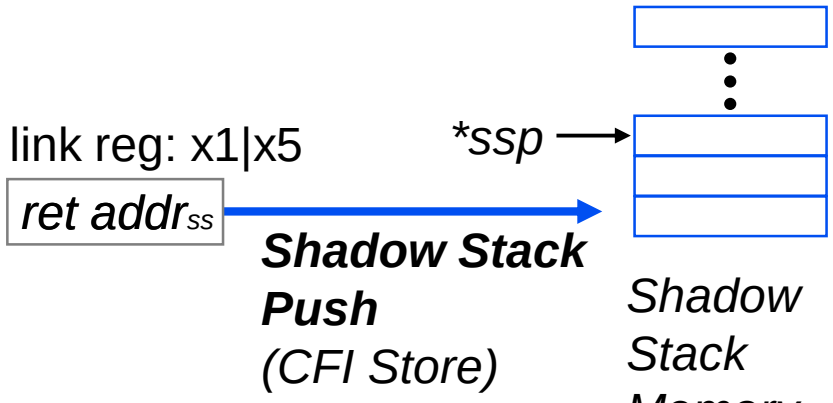

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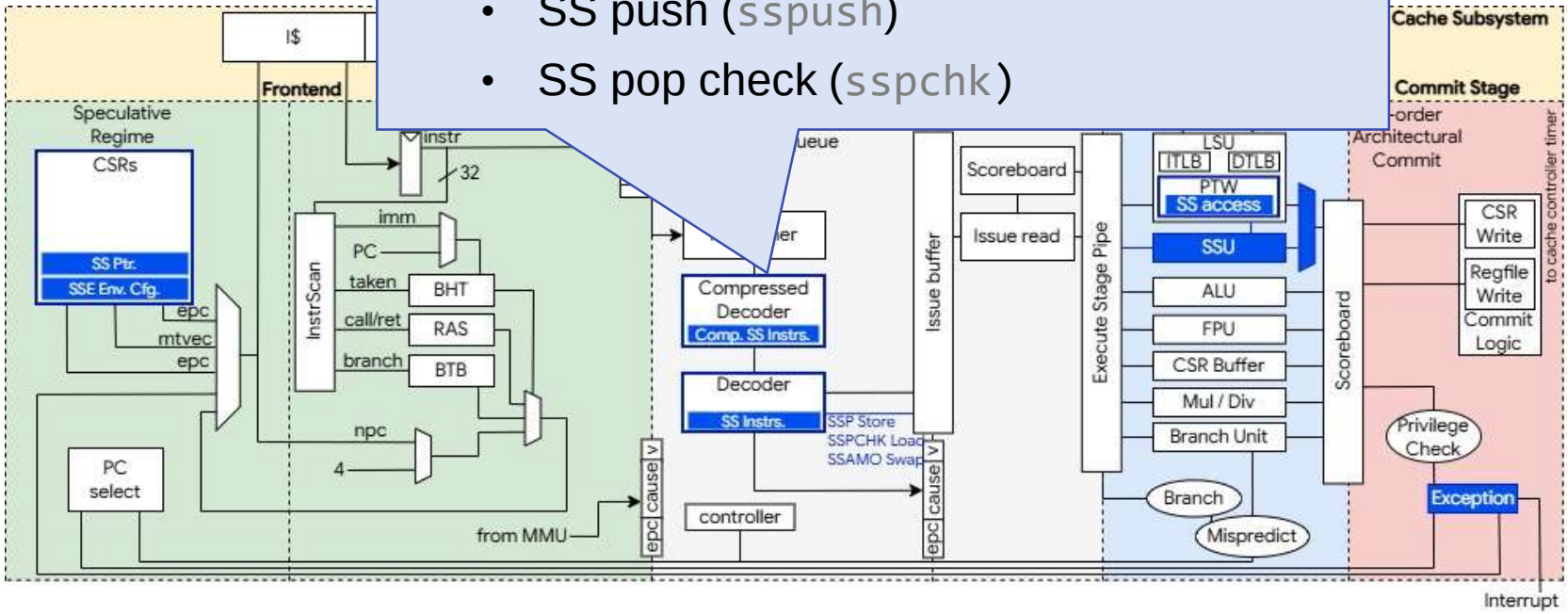

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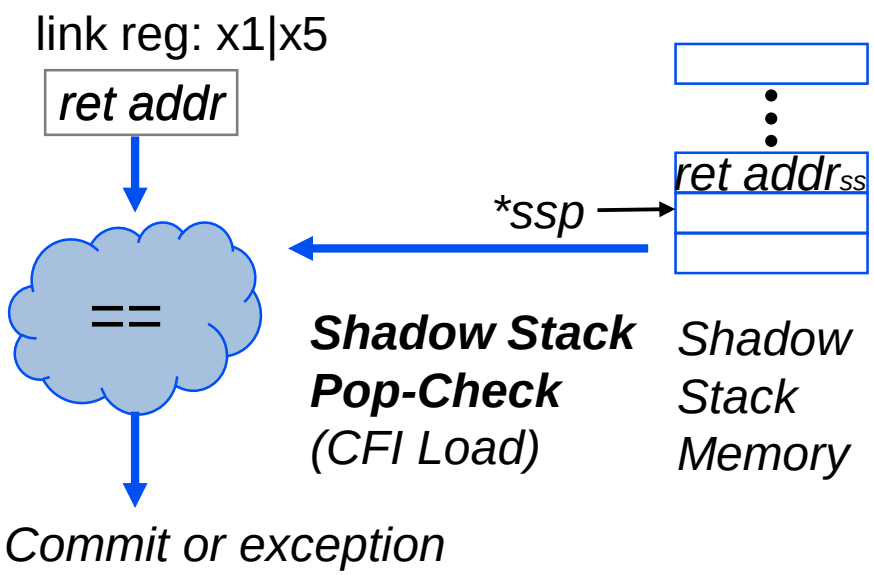

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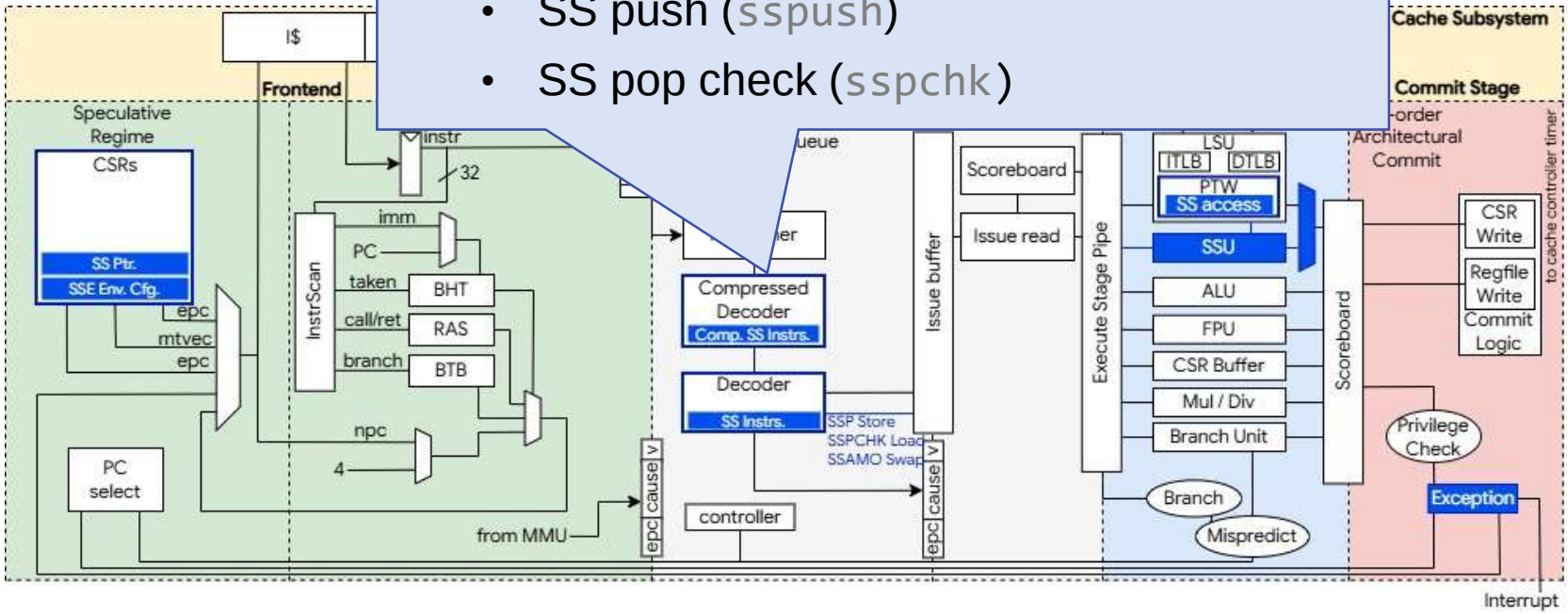

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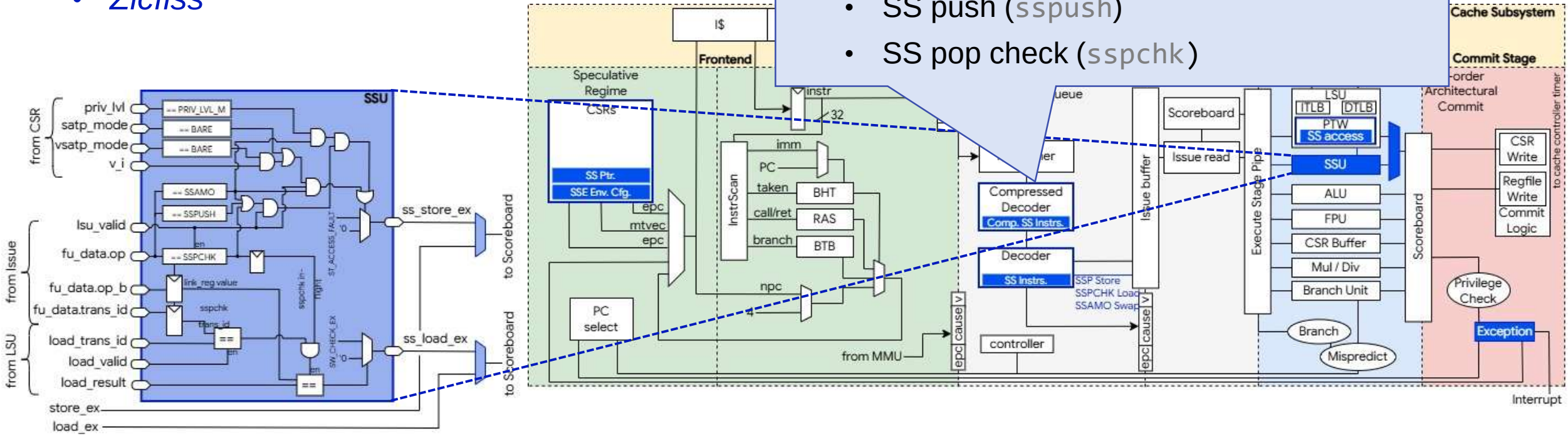

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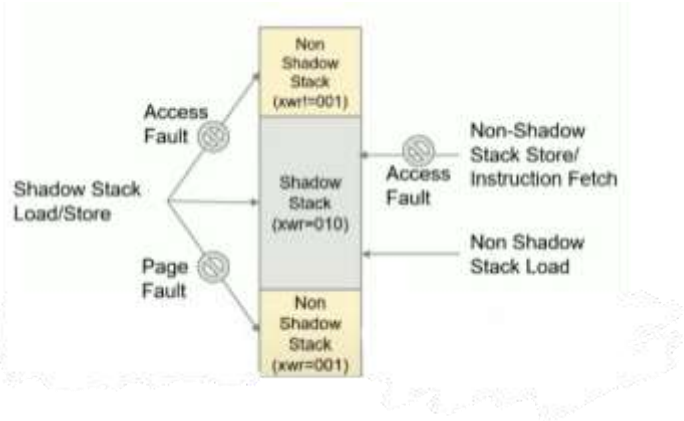
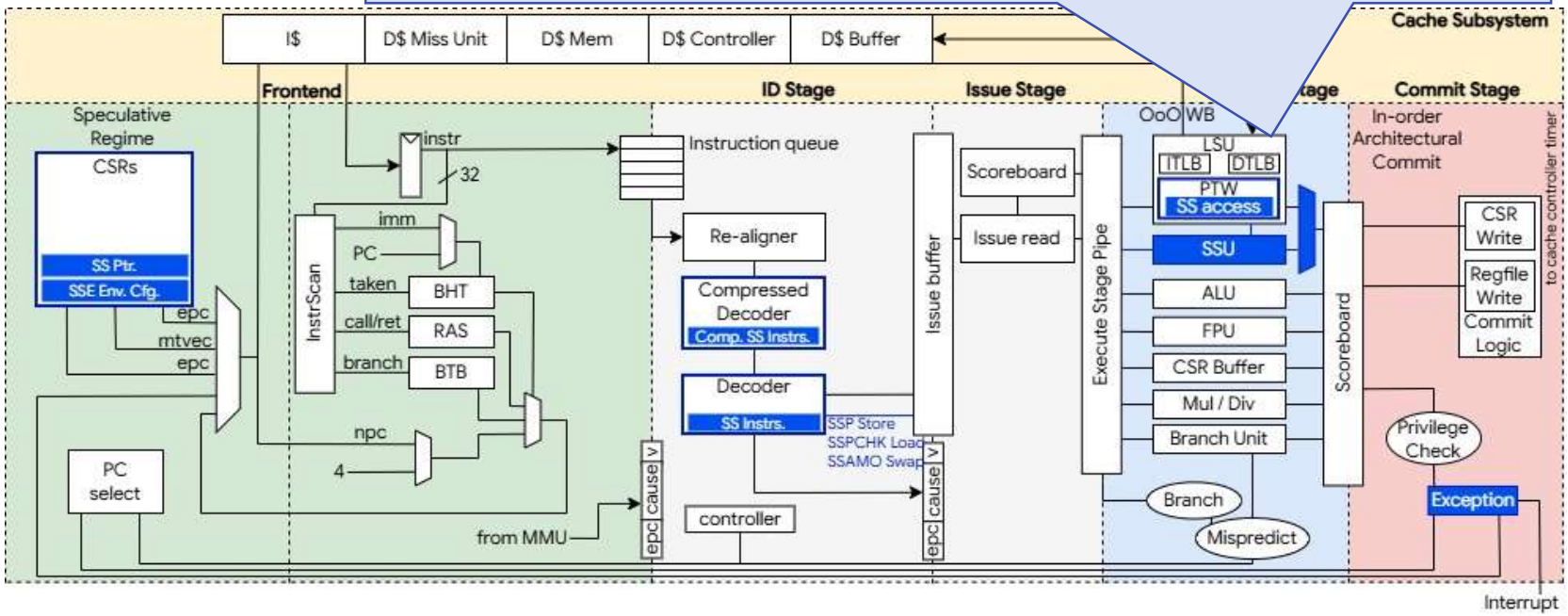


- Enforce checks on the type of accessed page
- Non-Shadow Stack instr. Only non Shadow-Stack pages and viceversa



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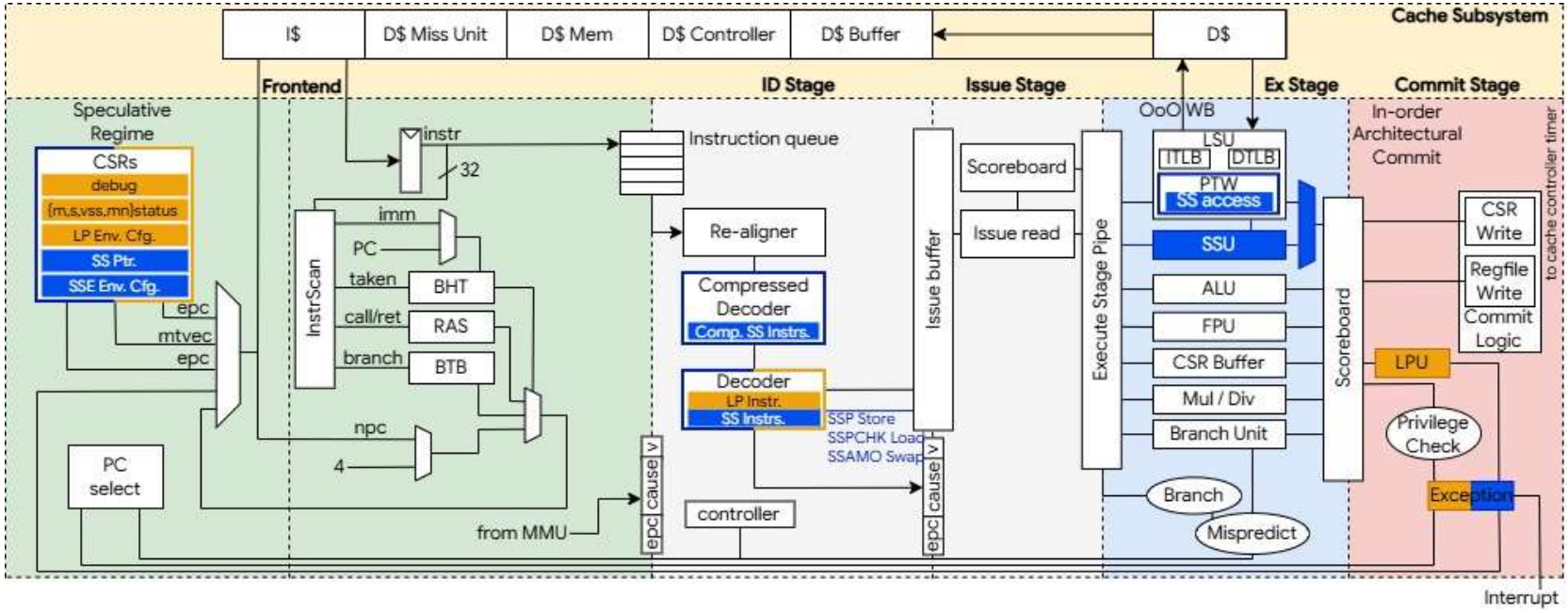

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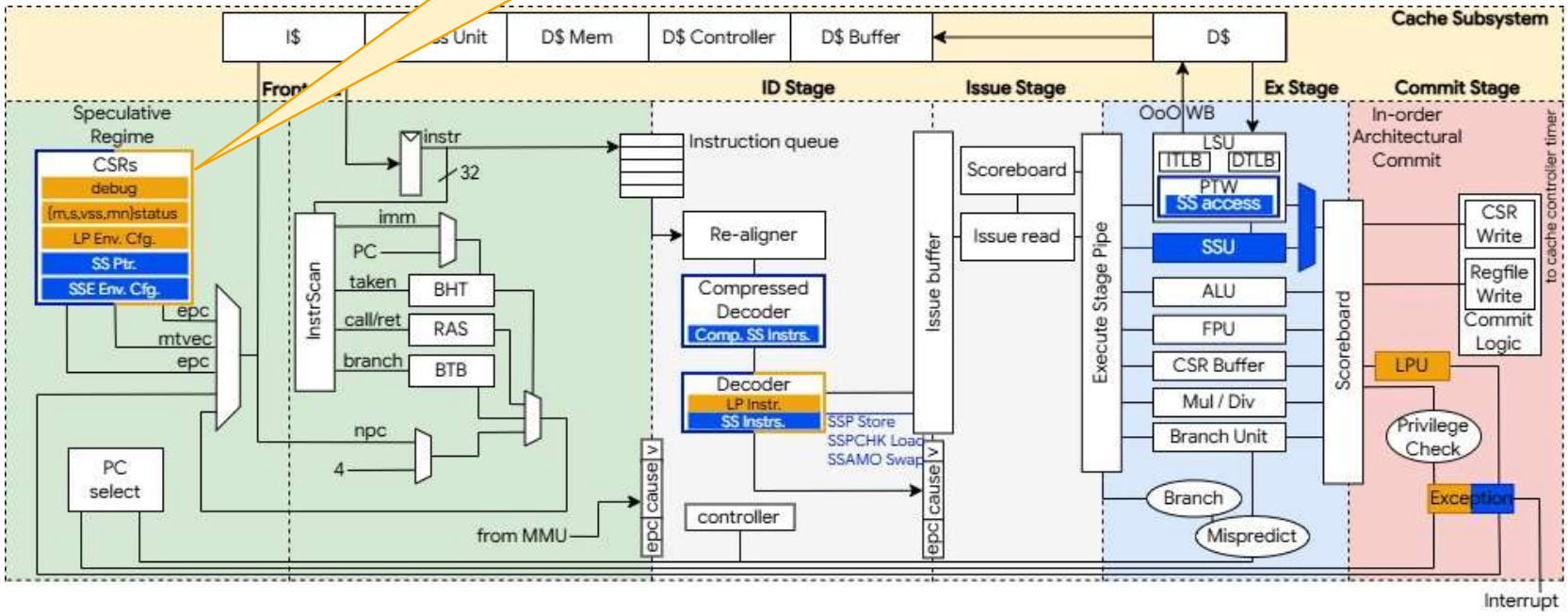

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- Landing pad instruction: `lp label`

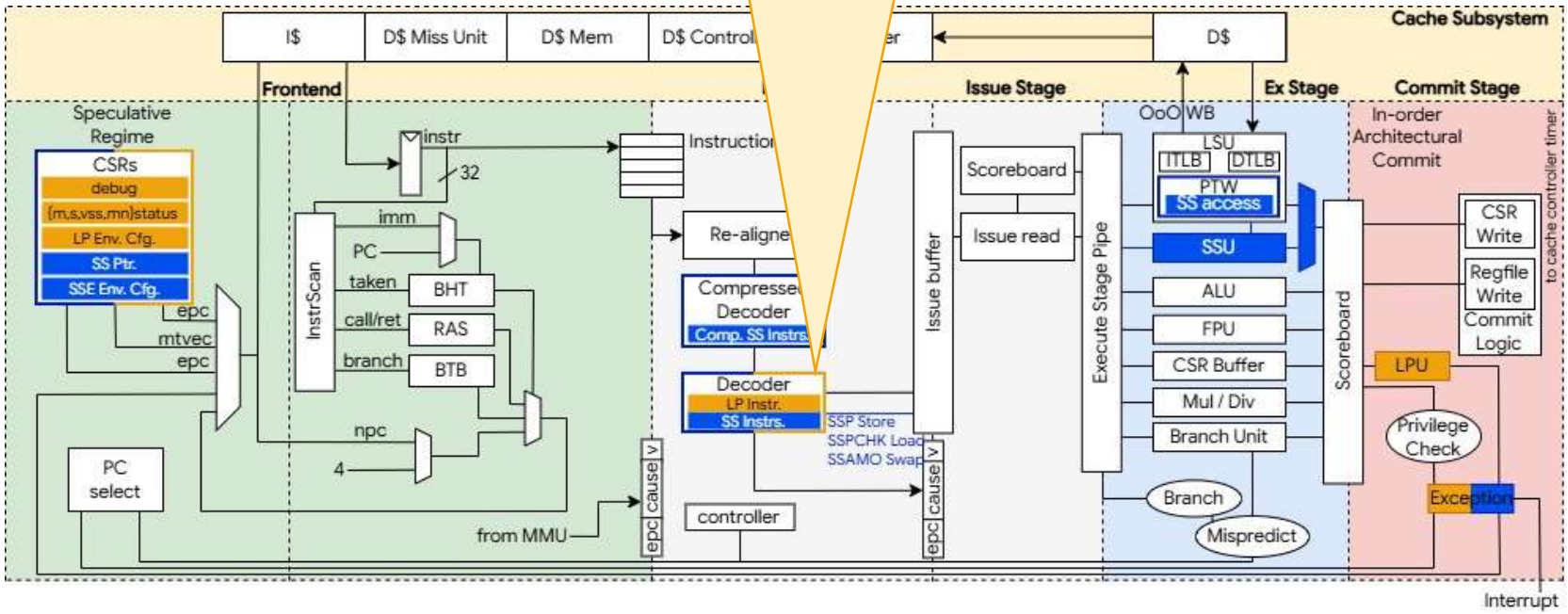
x7

label

==

auipc x7, %pcrel_hi(label)
addi x7, x7, %pcrel_lo(label)
jalr x1, xN, 0
addi sp, sp, -16

Exception



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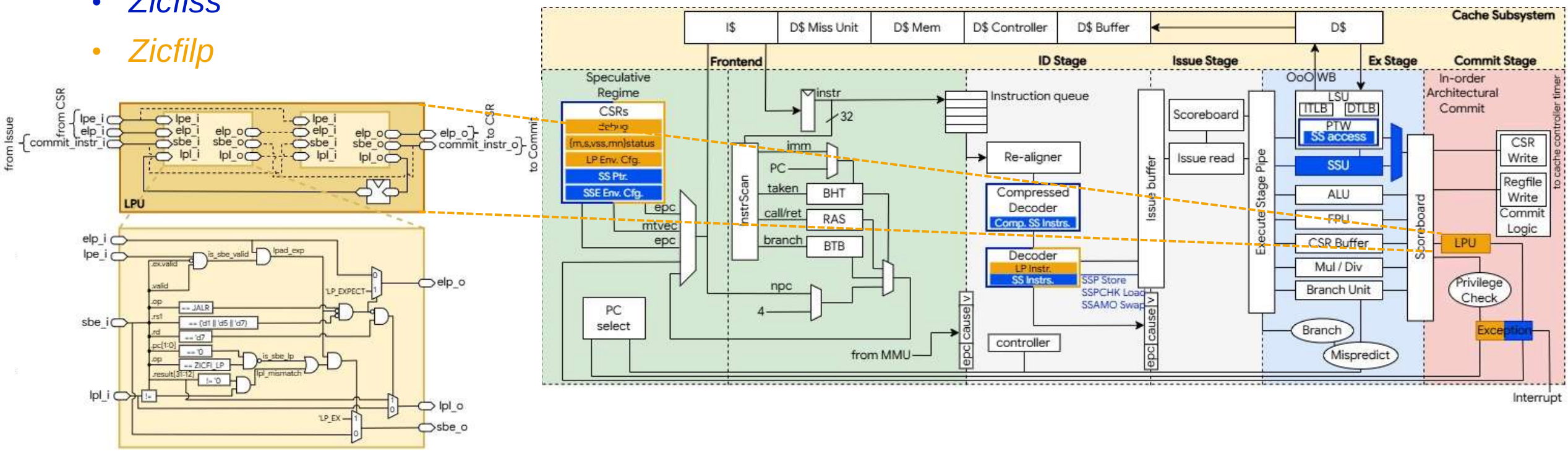

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Results

- Area overhead
  - Synthesis in GF22FDX, @800 MHz
  - *Zicfiss* and *Zcfilp* introduce no degradation in operating frequency

CVA6 Pipeline	Area [μm^2]		Overhead [%]
	Baseline	w/ CFI ext.	
CSR Reg. File	7831	8220	5.0
Fetch & Decode	1101	1124	2.1
Issue	25637	25788	0.6
Execute	61631	61854	0.4
Commit	182	372	103.6
Total	96382	97358	1.0

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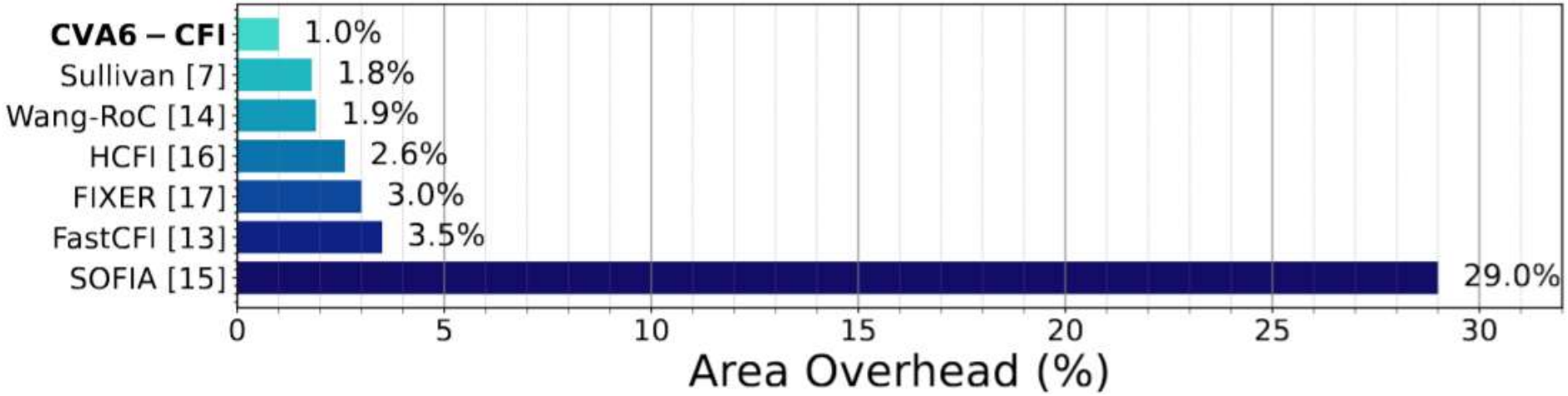
  - We compare the area overhead of our proposed CFI extension with prior hardware-centric CFI approaches [7, 13–17]
  - Overhead values are normalized to their respective baseline architectures



[7] D. Sullivan, e al,, “Efficiently Enforcing Control-Flow Integrity with a Security Coprocessor,” in IEEE SecDev, 2016

[13] W. Wang, et al., “Hardware-assisted control-flow integrity enhancement for iot devices,” IEEE DATE 2024

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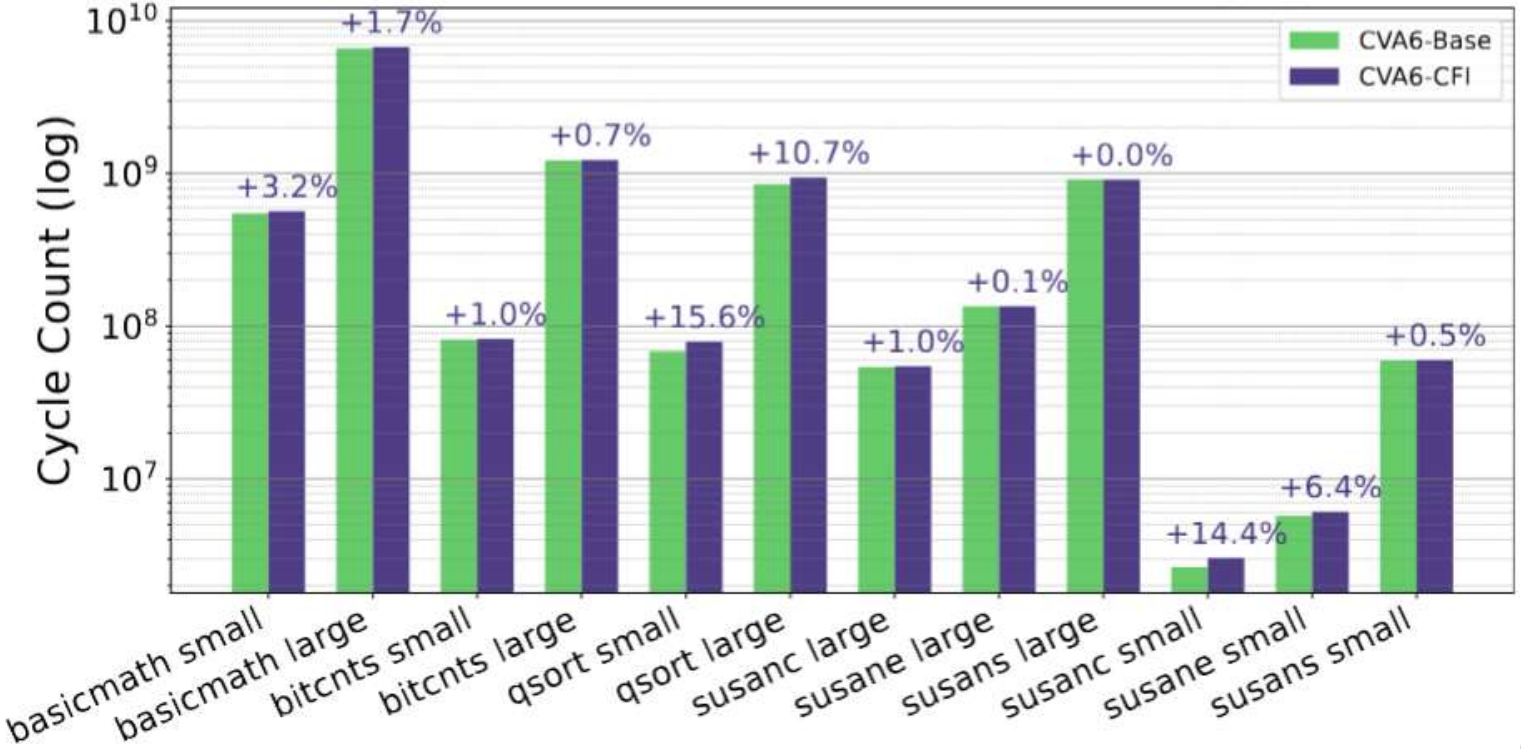
[16] N. Christoulakis, et al., “Hcfi: Hardware-enforced control-flow integrity,” ACM CODASPY 2016

[17] A. De, et al., “Fixer: Flow integrity extensions for embedded risc-v,” IEEE DATE 2019

Results

- Performance overhead
  - We evaluated the runtime overhead using *MiBench Automotive benchmark* subset
  - Compiled w/ CFI-aware SiFive GCC 13.3 [1]
  - The CFI extension introduces a modest slowdown (up to 15.6%)
  - Overhead is mainly due to shadow stack operations (`sspush`, `sspchk`)



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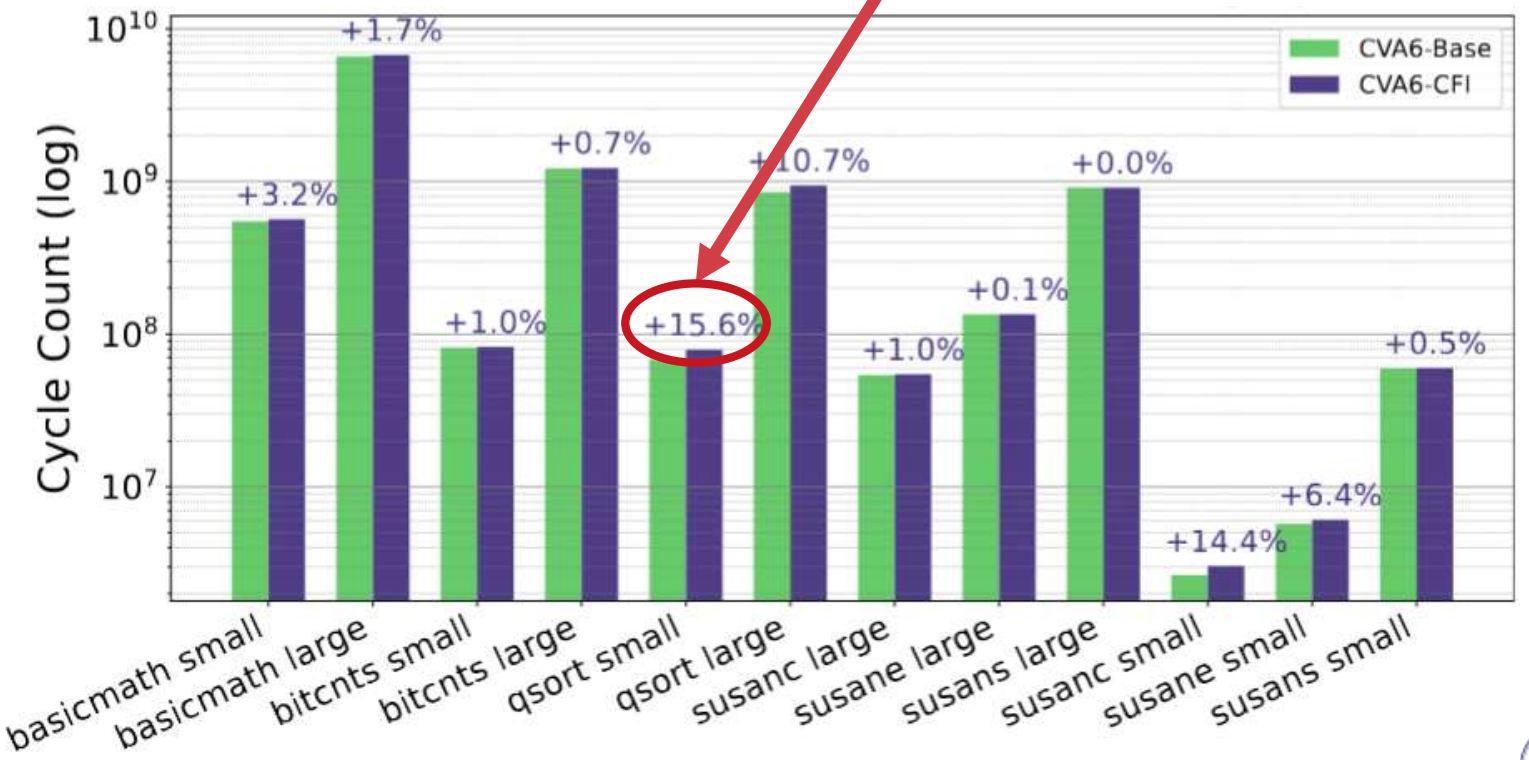
  - Open-Source! [2]



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Thank you!

Questions?