



Real-Time Histogram-Based Automated Signal Exposure Correction on FPGA for Optoacoustic Imaging

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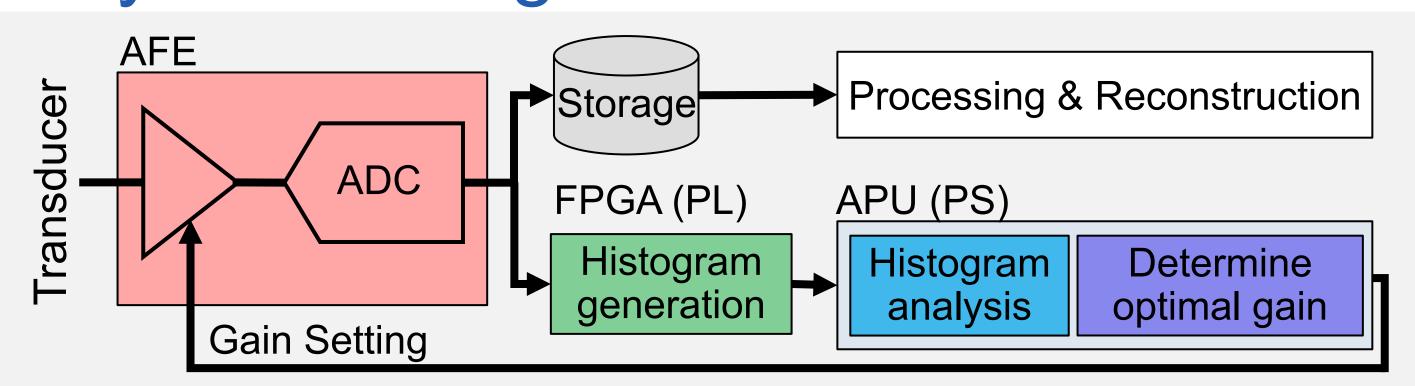
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1 Introduction

The adoption of optoacoustic imaging relies on compact, userfriendly systems that don't require expert tuning. Manual optimization of **Analog Frontend (AFE) gain** is timeconsuming, non-scalable, and prone to errors that affect image quality, especially at high frame rates.

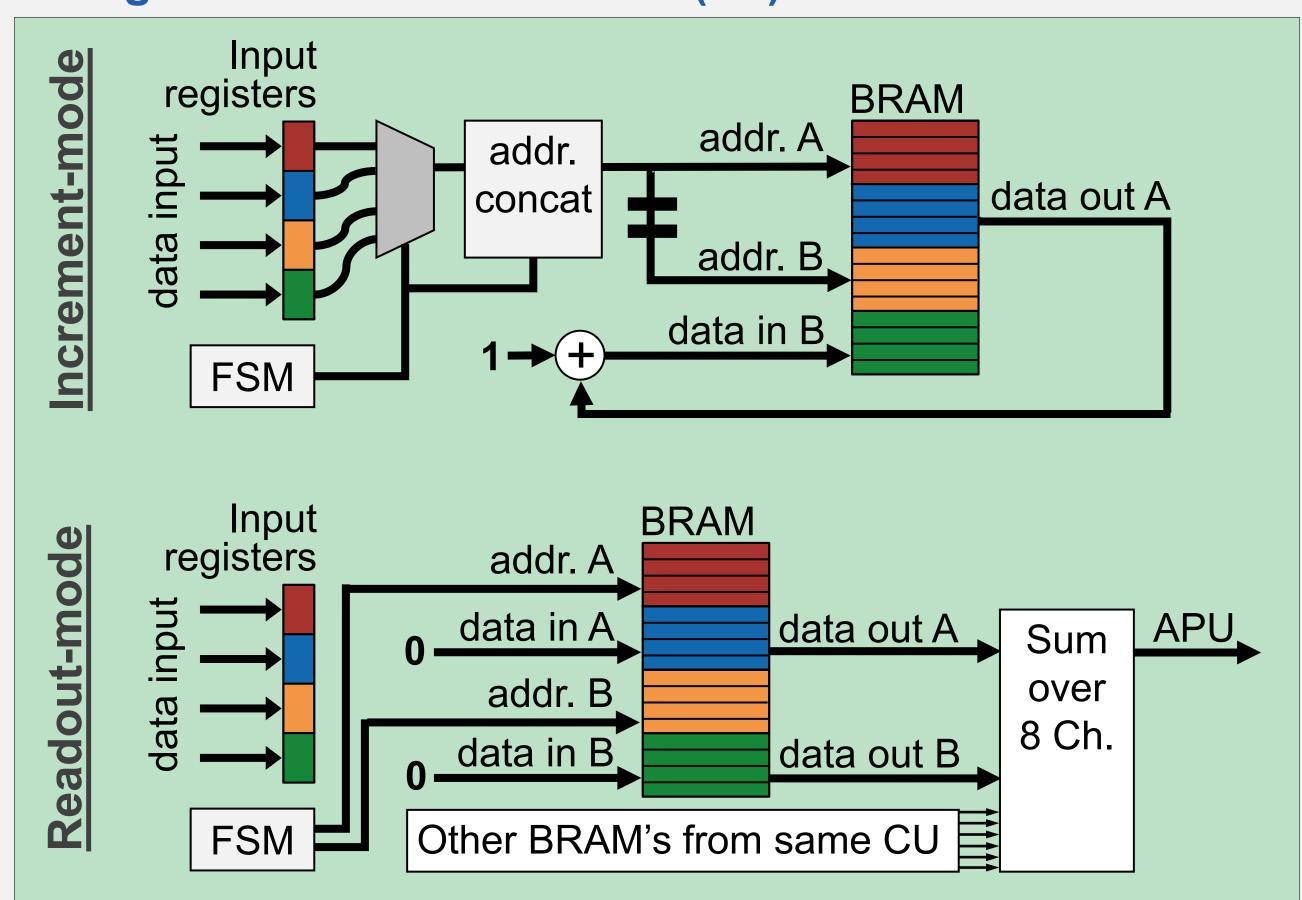
This work proposes an FPGA-based Automated Gain Control (AGC) method that uses histogram analysis of raw ultrasound data. AGC provides near instantaneous adjustments, as no image reconstruction is needed, and effectively prevents overor underexposure, consistently setting an optimal gain level.

2 System Design

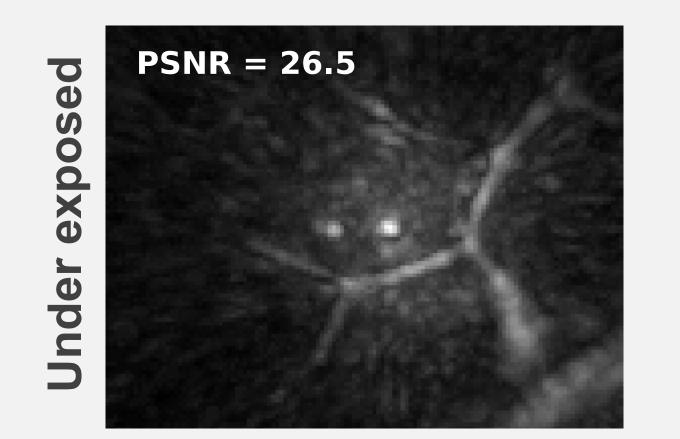


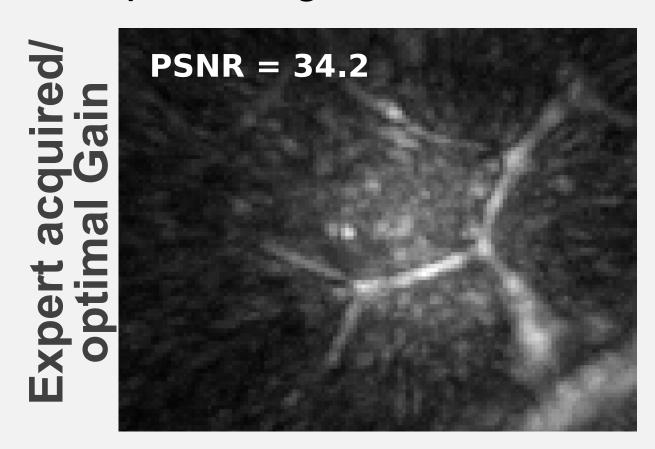
- 256 Channel Input stream at 100MHz with 16 bit resolution
- Grouped into Compute Units (CU) of 16 Channels

Histogram Generation – FPGA (PL)



- A histogram is generated for each channel
- Multiple channels are summed together during readout
- Application processor determines if the image is under- or overexposed and changes the acquisition gain





Gain Control – APU (PS) Sum of Determine Determine Average width of histograms W_{a. max} from histograms over all CU AFE settings histogram (W_a) Histogram: (log₁₀) AGC max bin count count If W_a Bin 30000 40000 50000 20000 Output amplitudes $W_{a, min} < W_{a} < W_{a, max}$ $W_a \ge W_{a, max}$ $W_{a, min} \leq W_{a}$ Underexposed **Optimal gain** Overexposed Increase gain by Reference frame Keep current gain $W_{a, opt} / W_{a}$ at minimum gain

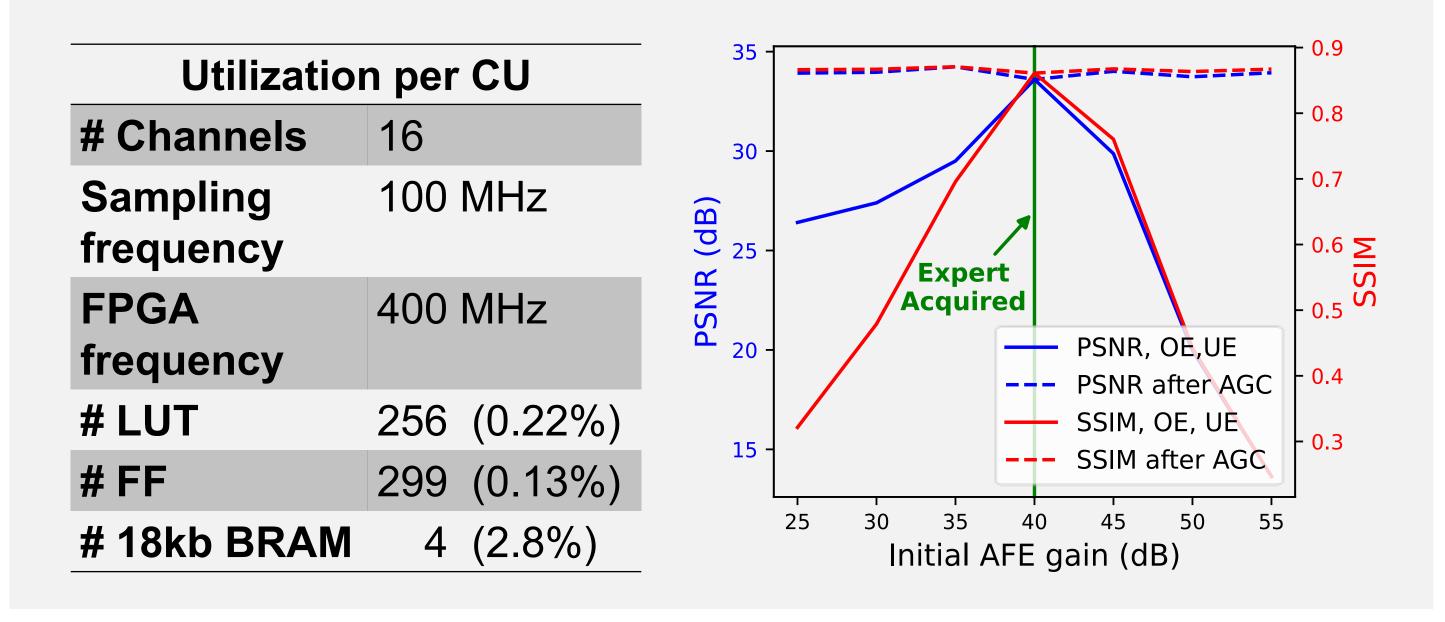
3 Results

Image Quality:

- AGC sets optimal gain over a dynamic range of 65dB
- Achieves SSIM: > 0.96 to expert acquired image (almost identical).

Hardware:

 Low resource implementation on Xilinx Kria K26 (more than 300 channels possible on small FPGAs)



4 Conclusion

- Histogram-based over- or underexposure detection directly from the AFE data stream
- Fully autonomous, real-time AFE gain correction
- Optimal image quality achieved with minimal FPGA resource usage



