

From an Open-Source ISA to Open-Source HW to Open-Source Silicon

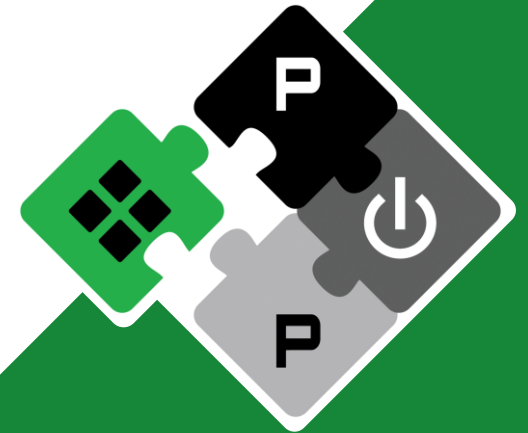
Integrated Systems Laboratory (ETH Zürich)

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PULP Platform

Open Source Hardware, the way it should be!



@pulp_platform 

pulp-platform.org 

youtube.com/pulp_platform 

Team of 100 people in ETH Zürich – University of Bologna



- **Research on energy-efficient computing architectures**
 - Started in 2013, celebrated 10 years of PULP last year
- **Led by Luca Benini**
 - Involves ETH Zürich (Switzerland) and University of Bologna (Italy)
 - Large group of almost 100 people

ETH zürich



ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

Team of 100 people in ETH Zürich – University of Bologna



- Research on energy-efficient computing architectures



We have designed and tested more than 60 PULP ICs



Check <http://asic.ethz.ch> for all our chips

We believe in open source



- **Collaboration with many different domain experts**
 - We cannot afford to do everything in-house
- **No long discussions on IP ownership and background IPs**
 - Everything in the open
- **We can start right away**
 - Time is spent on design not necessary paperwork
 - The licensing settles most of the needed discussions (who owns it, who can do what)
- **Friendly licensing for commercial purposes**
 - Permissive licensing allows commercial exploitation, foreground of partners can be closed
- **You can see what we have and evaluate us in advance**

Many benefits are enabled by open source



Managing Complex Designs

Faster Collaborations

Facilitates Industry/Academia Relationships

Auditable Designs, Reproducible Results

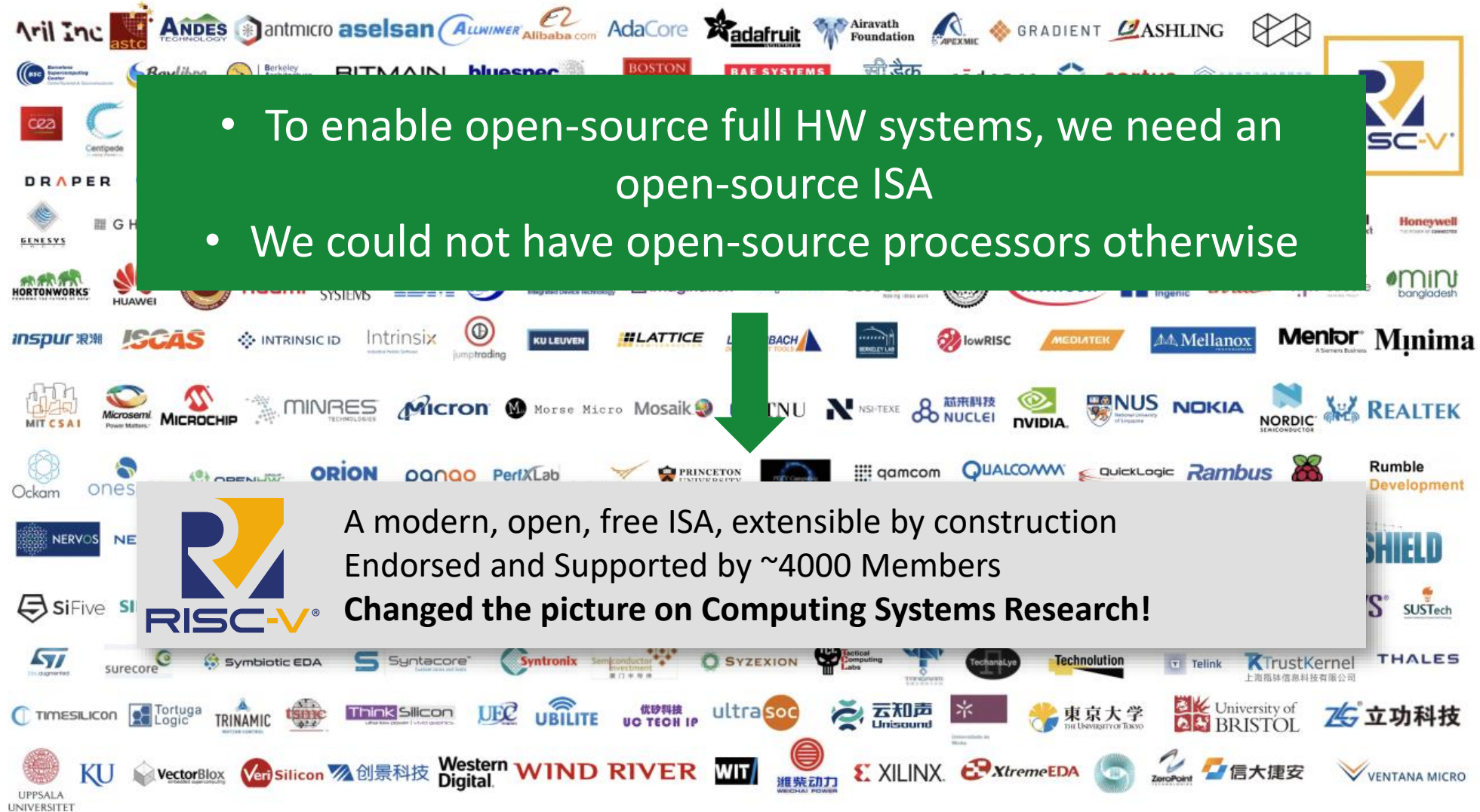
Starting from an open-source ISA: RISC-V



- To enable open-source full HW systems, we need an open-source ISA
- We could not have open-source processors otherwise



A modern, open, free ISA, extensible by construction
Endorsed and Supported by ~4000 Members
Changed the picture on Computing Systems Research!



....

and many many more

RISC-V Open-Source Software



Huge momentum, extensible,
open-source, patent troll safe

- Toolchains



GCC, LLVM

Emulators: QEMU, TinyEMU, Spike, Renode

- System tools

A wide SW ecosystem already available to evaluate, ... and more
and use RISC-V hardware systems

- Language Runners

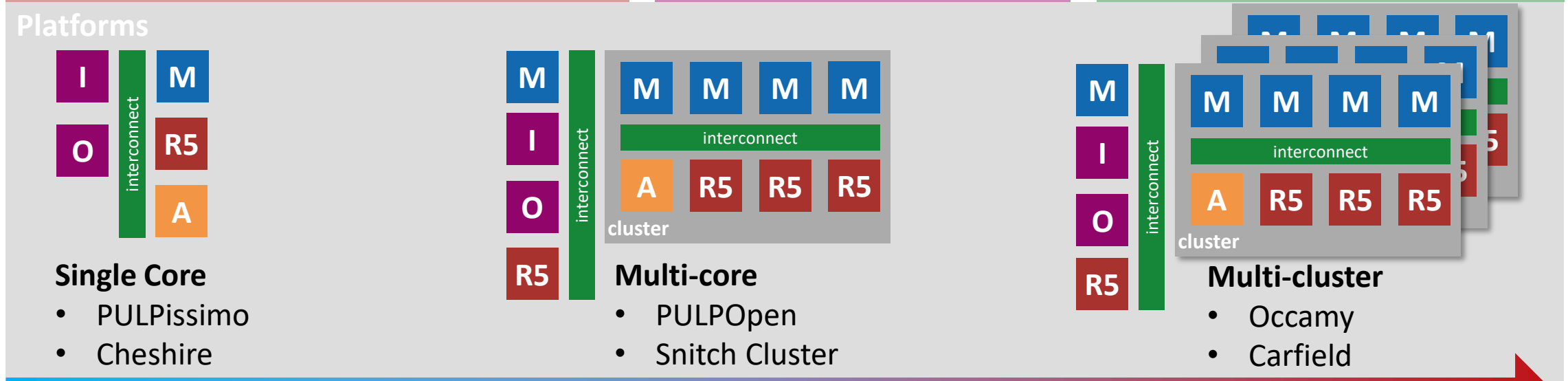
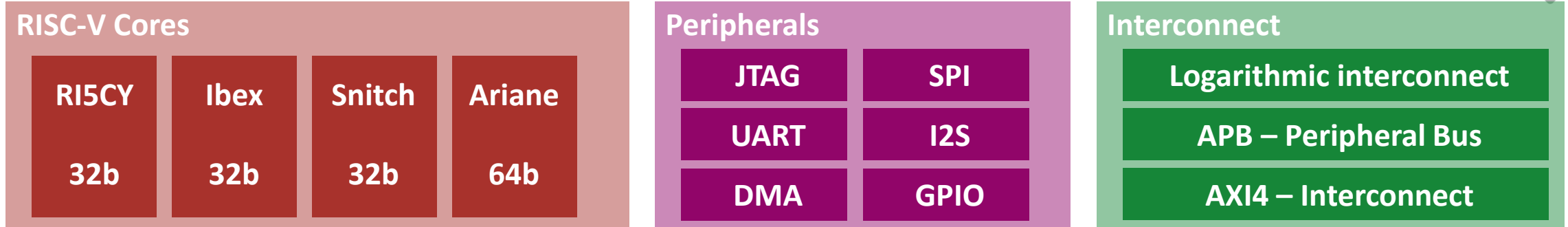
- Operating Systems



Linux: Fedora, OpenSUSE, Gentoo,
OpenEmbedded/Yocto, Buildroot, OpenWRT, FreeBSD
FreeRTOS, Zephyr, RTEMS, Xv6, HelenOS, ... and more

<https://github.com/riscv/riscv-software-list>

What PULP provides is a box of building blocks



All of our designs are open-source hardware



- All our development is on GitHub using a permissive license
 - HDL source code, testbenches, software development kit, virtual platform

<https://github.com/pulp-platform>



- Allows anyone to use, change, and make products without restrictions.

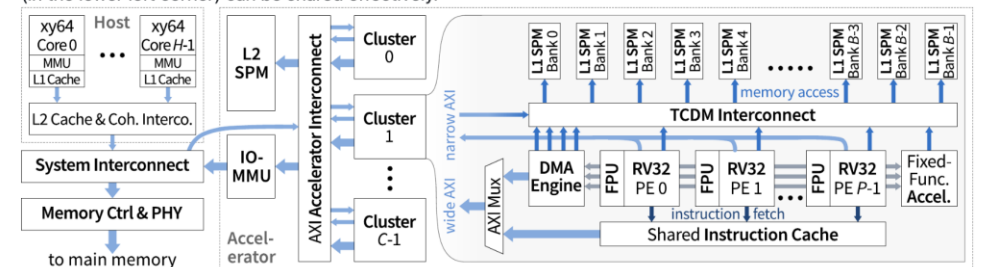
The screenshot shows the GitHub repository page for 'pulp-platform'. At the top, there is a navigation bar with 'Overview', 'Repositories 239', 'Projects 1', 'Packages', and 'People 14'. Below this, there are four pinned repository cards:

- pulp** (Public): This is the top-level project for the PULP Platform. It instantiates a PULP open-source system with a PULP SoC (microcontroller) domain accelerated by a PULP cluster with 8 cores. It has 312 stars and 93 forks.
- pulpissimo** (Public): This is the top-level project for the PULPissimo Platform. It instantiates a PULPissimo open-source system with a PULP SoC domain, but no cluster. It has 288 stars and 137 forks.
- snitch** (Public): Lean but mean RISC-V system!
- hero** (Public): Heterogeneous Research Platform (HERO) for exploration of

Heterogeneous Research Platform (HERO)

HERO is an FPGA-based research platform that enables accurate and fast exploration of heterogeneous computers consisting of programmable many-core accelerators and an application-class host CPU. Currently, 32-bit RISC-V cores are supported in the accelerator and 64-bit ARMv8 or RISC-V cores as host CPU. HERO allows to seamlessly share data between host and accelerator through a unified heterogeneous programming interface based on OpenMP 4.5 and a mixed-data-model, mixed-ISA heterogeneous compiler based on LLVM.

HERO's hardware architecture, shown below, combines a general-purpose host CPU (in the upper left corner) with a domain-specific programmable many-core accelerator (on the right side) so that data in the main memory (in the lower left corner) can be shared effectively.



All of our designs are open-source hardware



- All our development is on GitHub using a permissive license
 - HDL source code, testbenches, software development

Many of the GitHub Trending SystemVerilog repositories for the past months are:

- either directly from our group
- or have originated in our group

Explore Topics **Trending** Collections Events GitHub Sponsors

Search: Type to search

Trending

See what the GitHub community is most excited about this month.

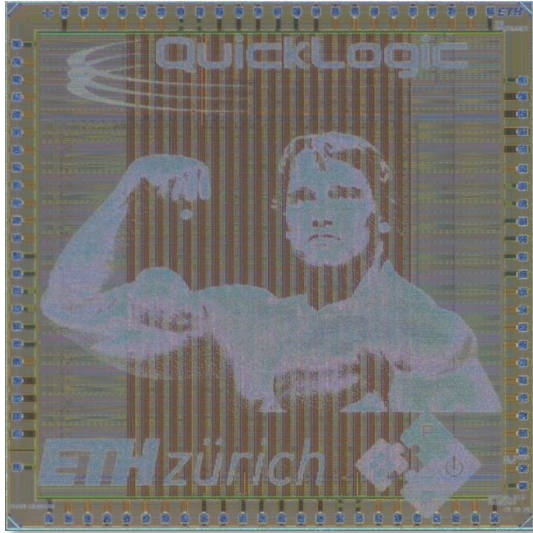
Repositories Developers Spoken Language: Any Language: SystemVerilog Date range: This month

- lowRISC / opentitan** OpenTitan: Open source silicon root of trust
SystemVerilog 2,100 647 Built by [avatars] 43 stars this month
- pulp-platform / axi_mem_if** Simple single-port AXI memory interface
SystemVerilog 29 21 Built by [avatars] 1 star this month
- pulp-platform / riscv-dbg** RISC-V Debug Support for our PULP RISC-V Cores
SystemVerilog 166 64 Built by [avatars] 7 stars this month
- pulp-platform / axi2apb**
SystemVerilog 12 19 Built by [avatars] 0 stars this month
- pulp-platform / axi_riscv_atomics** AXI Adapter(s) for RISC-V Atomic Operations
SystemVerilog 39 11 Built by [avatars] 0 stars this month
- pulp-platform / apb_node**
SystemVerilog 5 17 Built by [avatars] 0 stars this month
- openhwgroup / cv32e40p** CV32E40P is an in-order 4-stage RISC-V RV32IMFCXpulp CPU based on RISCV from PULP-Platform
SystemVerilog 832 369 Built by [avatars] 20 stars this month

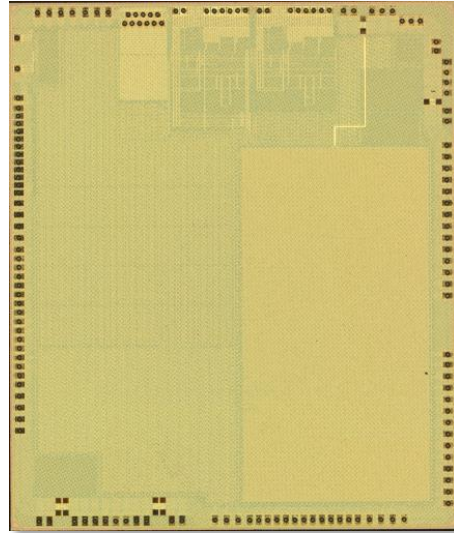
snitch Public
Lean but mean RISC-V system!

hero Public
Heterogeneous Research Platform (HERO) for exploration of

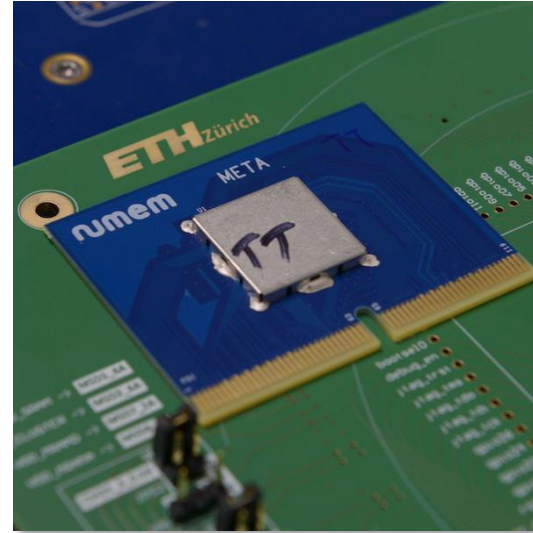
The open model led to successful industry collaborations



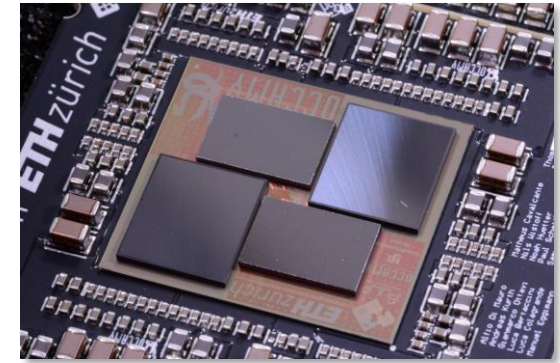
Arnold (GF22)
eFPGA with RISC-V core



Vega (GF22)
IoT Processor with
ML acceleration



Siracusa (TSMC16)
IoT Processor with
NVM technology



Occamy (GF12)
Chiplet based ML
accelerator with 432
RISC-V cores

And many have used our work for their research



Smallest RISC-V Device for Next-Generation Edge Computing

RISC-V Workshop

Our 1st gen. processor and 2.5D integrated device

Processor SoC (D02)

SoC size: 300 μ m x 250 μ m, GF14LPP
 SoC arch: Based on PULPino (RV32IMC) PULPino
 On chip memory: 2KB data SRAM
 + Authentication engine
 + Analog custom circuits(LDO, Clock/Reset, PD/LED IF)

Seiji Munetoh¹, Chitra K Subramanian², Arun Paidimarri², Yasuteru Kohda²
 IBM Research – Tokyo¹ & T.J. Watson Research Center²

RISC-V week Barcelona 2018

An 8-core RISC-V Processor with Compute near Last Level Cache in Intel 4 CMOS

Gregory K. Chen, Phil C. Knag, Carlos Tokunaga, Ram K. Krishnamurthy
 Circuit Research Lab, Intel Corporation, Hillsboro, OR, USA, gregory.k.chen@intel.com

ISA	RV64GC
Execution	Out-of-order
L1I	16kB/core, 4-way
L1D	8kB/core, 4-way
NoC	64b 2D Mesh
L2 LLC	512kB, 4-way
LLC BW 1GHz	1.0 Tb/s
CNC Area Overhead	1.4%
#CNC MACs	128
CNC RF	1kB/slice
Energy Eff. 0.6V	285 GOPS/W
LLC Energy Eff. 0.6V	1.6 TOPS/W

VLSI Symposium 2022

The Deep Learning Revolution and Its Implications for Computer Architecture and Chip Design

Presenting the work of many people at Google

Jeff Dean
 Google Research

Article
A graph placement methodology for fast chip design

<https://doi.org/10.1038/s41586-021-03544-w>
 Received: 3 November 2020
 Accepted: 13 April 2021
 Published online: 9 June 2021

Azalia Mirhoseini¹*, Anna Goldie^{1,2}*, Elrahim Songhor¹, Shen Wang¹, You Azade Naz¹, Jiawo Pak¹, Andy Tong¹, Quoc V. Le¹, James Laudon¹, Richard I

Fig. 4 | Convergence plots on Ariane RISC-V CPU. Placement cost of training a policy network from scratch versus fine-tuning a pre-trained policy network for a block of Ariane RISC-V CPU.

ISSCC Keynote 2020 – Nature 2020

AutoDMP: Automated DREAMPlace-based Macro Placement

Anthony Agnesina aagnesina@nvidia.com NVIDIA Corporation Austin, TX, USA	Puranjay Rajvanshi prajvanshi@nvidia.com NVIDIA Corporation Santa Clara, CA, USA	Tian Yang tiyang@nvidia.com NVIDIA Corporation Santa Clara, CA, USA	Geraldo Pradipta gpradipta@nvidia.com NVIDIA Corporation Santa Clara, CA, USA
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Figure 7: Pre-CTS placements of the logical groups and cell densities of the MemPool Group designs using NanGate 45nm process (freq. = 333 MHz, density = 68%). Congestion (H/V): Innovus (2.66%/1.54%), AutoDMP (3.48%/1.86%).

ISPD'23

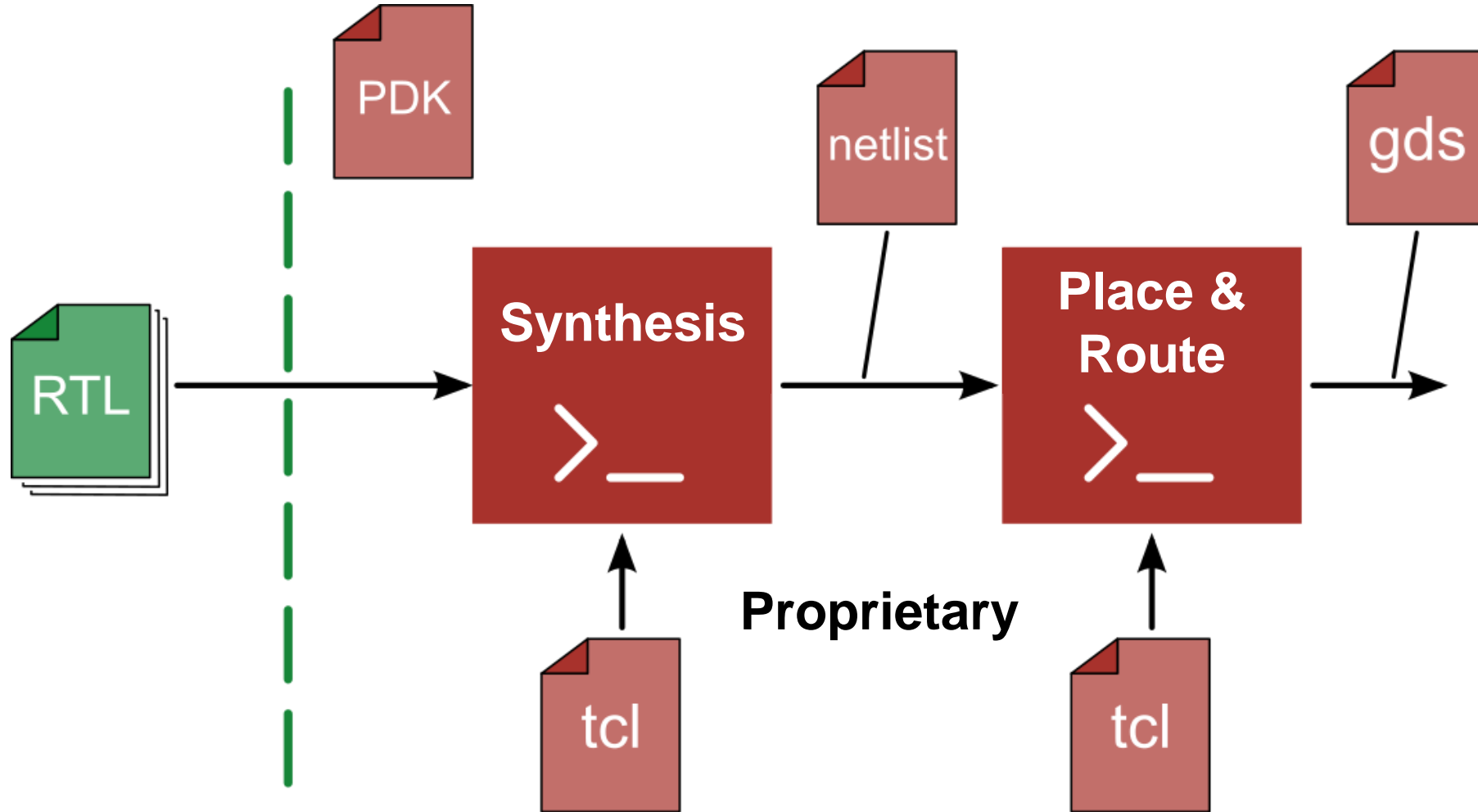
Some (surprising) side effects of open-source hardware



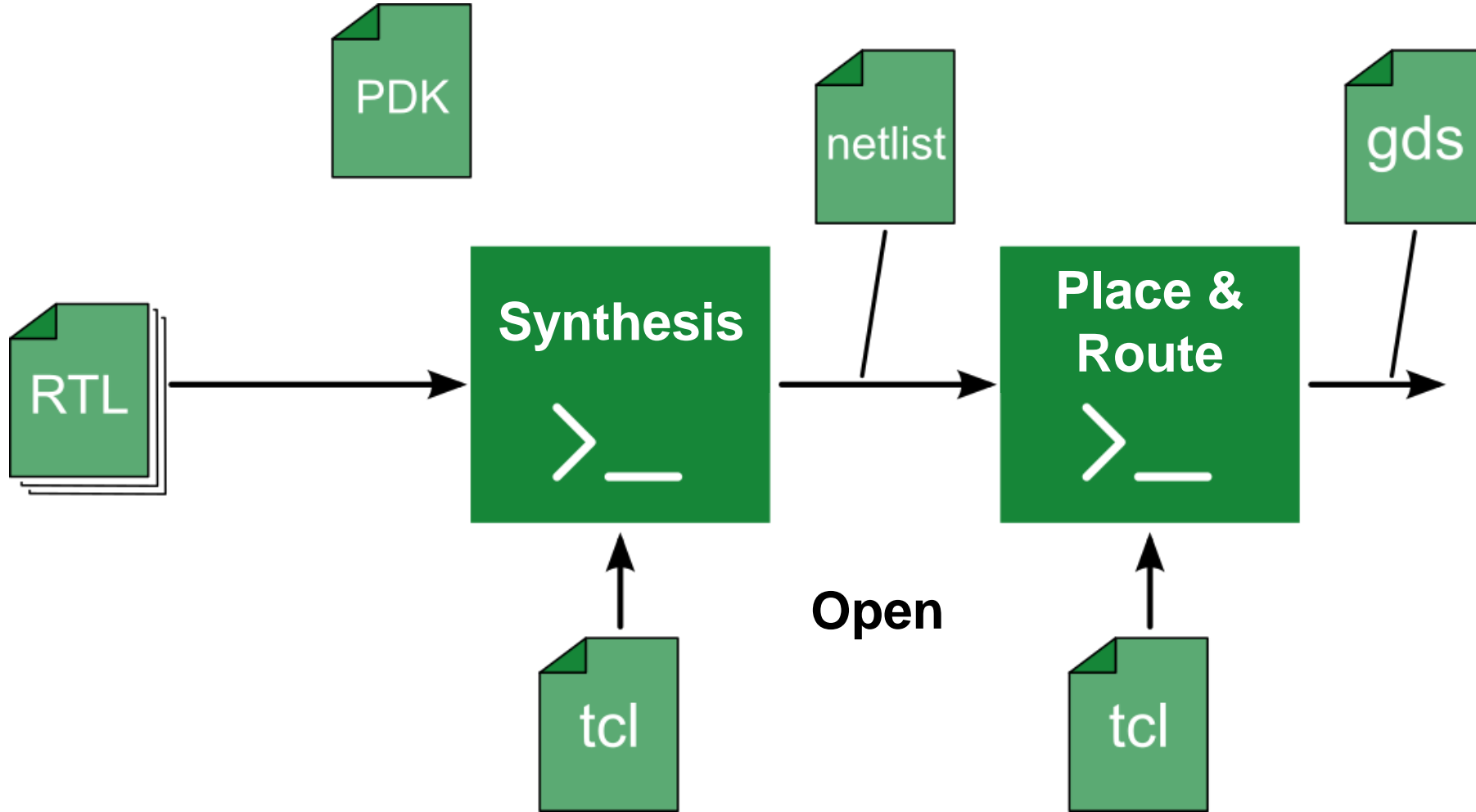
- **There is a surprising amount of bureaucracy involved**
 - Code Ph.D. students/staff develop belongs to the university (they pay us)
 - Master/semester thesis students own the work they produce
 - Need to get proper approval for everyone involved

- **Most agreements with companies are not meant for open source**
 - Instead of paying for exclusive IP, we need sponsoring agreements
 - Important to make sure we do not sign anything that binds our open-source effort

From Open Hardware...



...to fully open-source IC design



Benefits of end-to-end openness



- **Research**

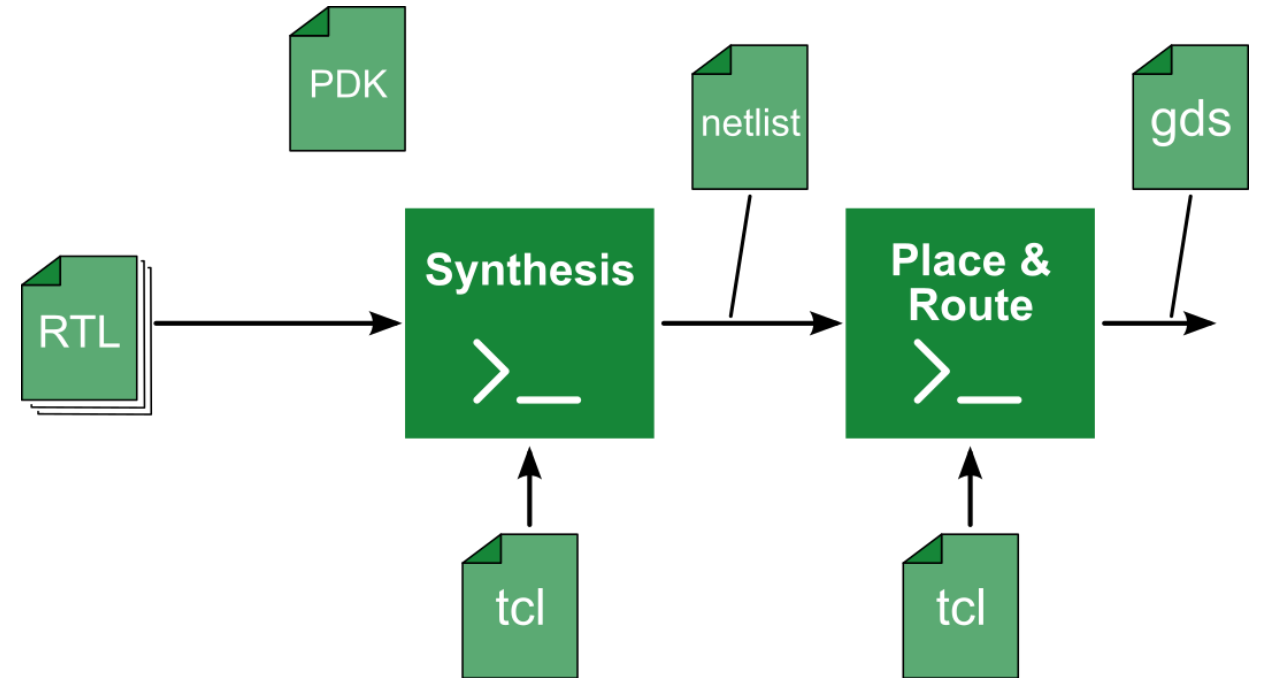
- Easier collaboration (no NDAs)
- Reproducing results
- New research (using tools or data)

- **Education**

- Increased access
- Experiment with flows and tools
- No black boxes, full transparency

- **Industry**

- Transparent chain of trust
- Lower initial cost



Open-source PDKs are the key



- **Physical designs will contain technology relevant information**
 - Nothing can be released (even if there were perfect open EDA tools) without technology info
 - So no open PDK no open source releases beyond RTL/HLS code
- **IPs containing proprietary information on technology cannot be released**
 - Open PDKs will allow us to change this
- **Some good progress, more is needed**
 - Skywater (130nm), IHP (130nm)
 - A 40nm/65nm open PDK would be a game changer, many viable products could be designed

Open-source EDA tools



- **Open EDA tools work well and are improving fast**
 - ETHZ is actively collaborating with UCSD
 - Currently working with Yosys (for synthesis) and OpenRoad (for PnR)
- **Will not replace commercial EDA**
 - A gap to PPA, service, support will remain
- **Open source EDA will allow you to make your own chips**
 - Good for many applications/needs
 - Will be great for teaching
- **Summer school at ETH Zürich**
 - June 3rd – 7th



OpenROAD

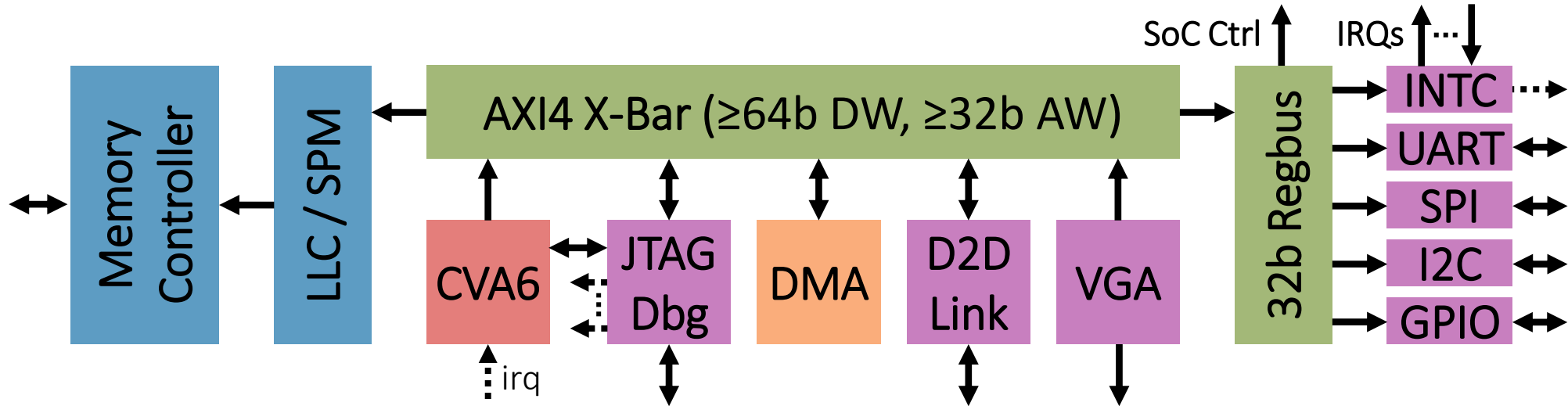
EFCL SUMMER SCHOOL
on Open Source IC Design and Computer Architectures
Zurich
June 3rd - 7th, 2024

<https://efcl.ethz.ch/efcl-summer-school.html>



Fully open IC design

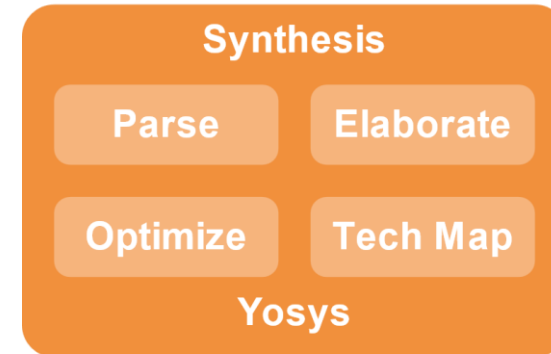
System architecture



- An open-source Linux-capable RISC-V MPU (based on <https://github.com/pulp-platform/cheshire>)
- Including a 64-bit RISC-V core (CVA6 - <https://github.com/openhwgroup/cva6>)
- About 1 MGE of logic

Open-source tool-flow

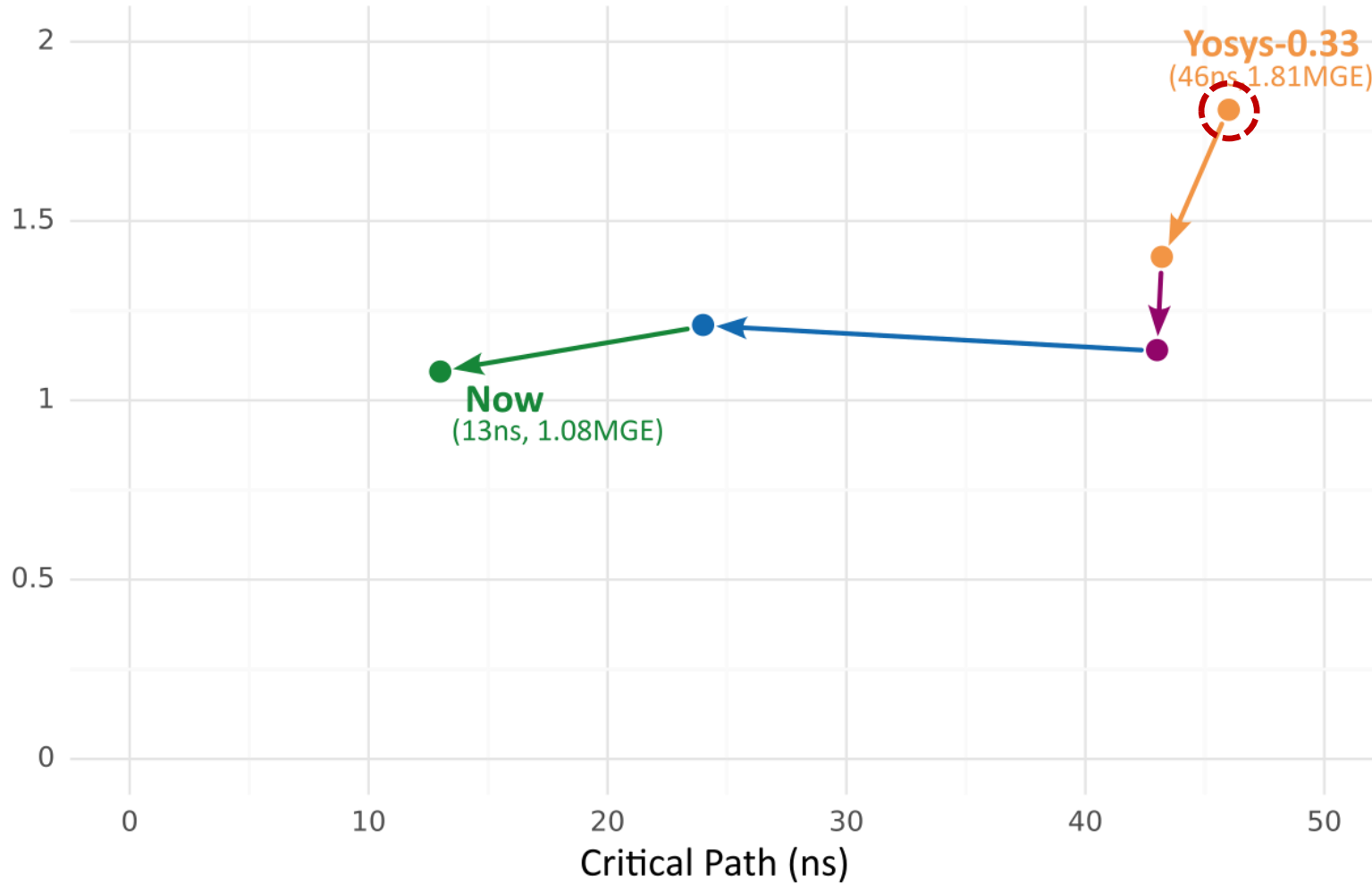
- **Open-Source PDK (IHP 130nm)**
- **Pre-Process**
 - Simplify SystemVerilog
 - Convert to Verilog
- **Synthesis**
 - Yosys from RTL to generic-cells
 - Calls ABC for logic optimization and mapping
- **Place-and-Route**
 - Collection of research tools into OpenRoad



Massive PPA improvements in 6 months



Logic Area (MGE)

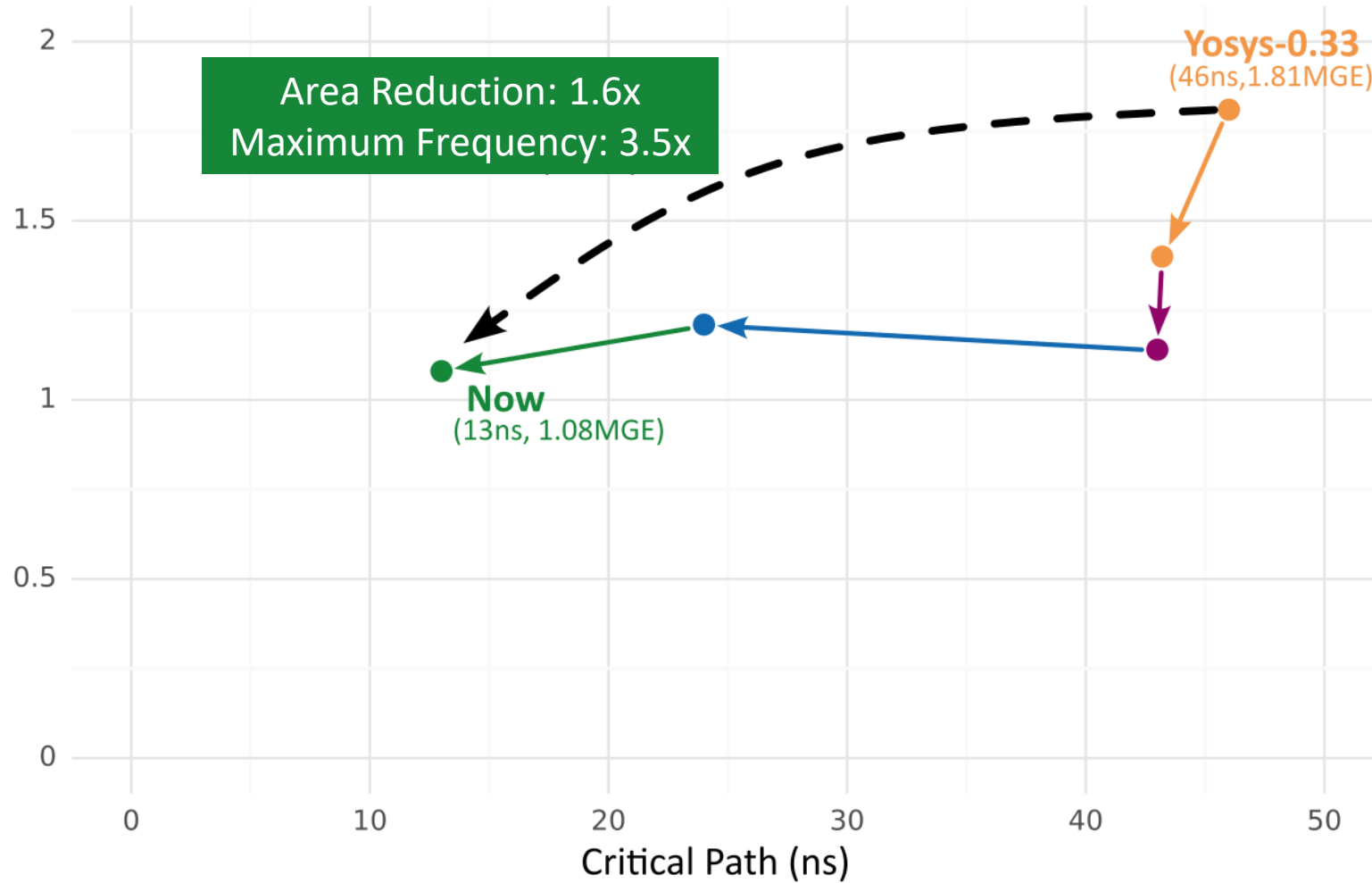


IHP130, tt-corner; Yosys-0.37 with optimized script if not mentioned otherwise

Massive PPA improvements in 6 months



Logic Area (MGE)

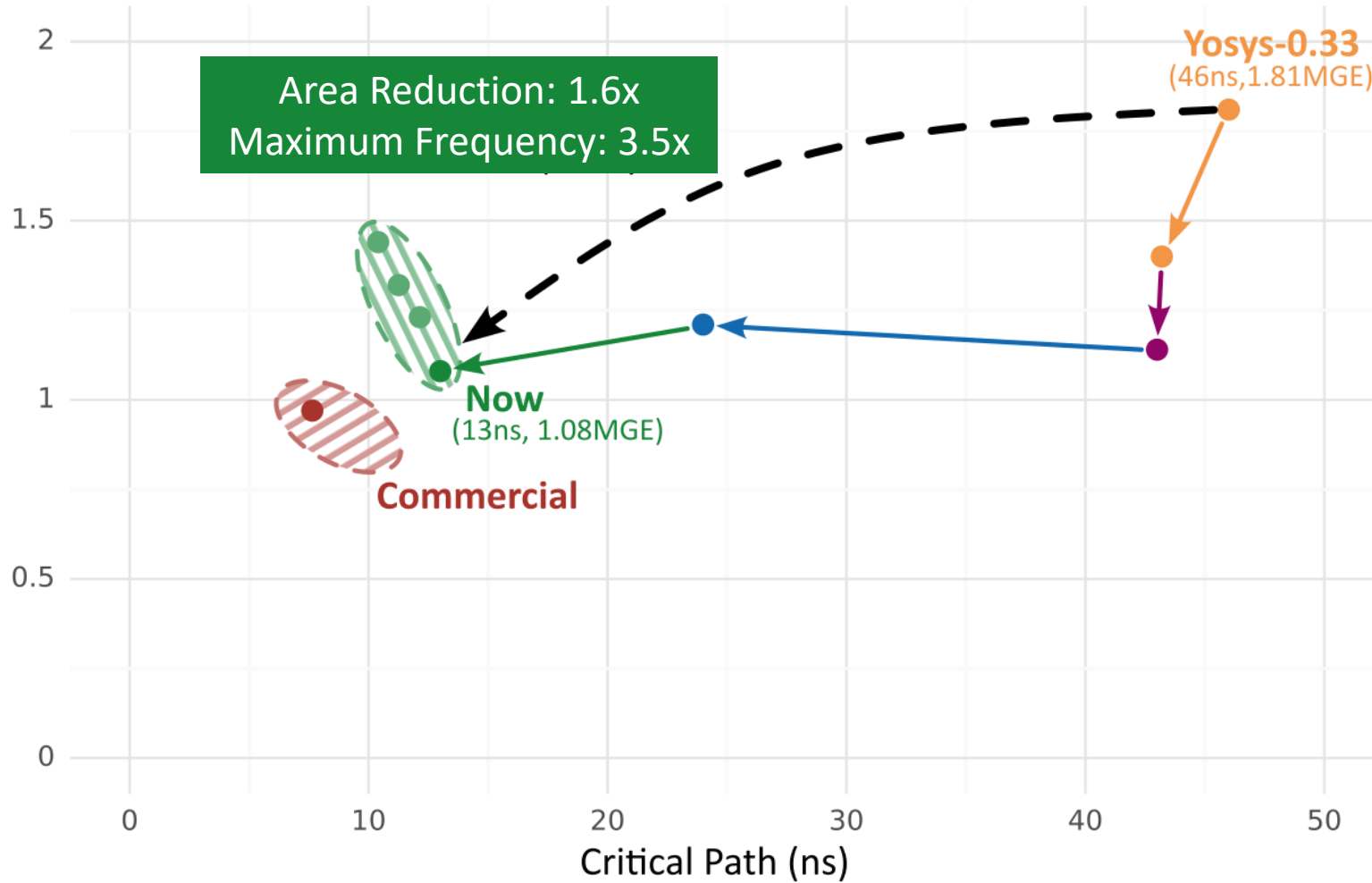


IHP130, tt-corner; Yosys-0.37 with optimized script if not mentioned otherwise

Massive PPA improvements in 6 months



Logic Area (MGE)

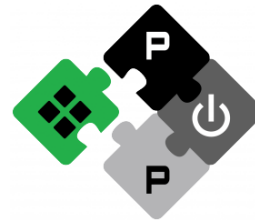
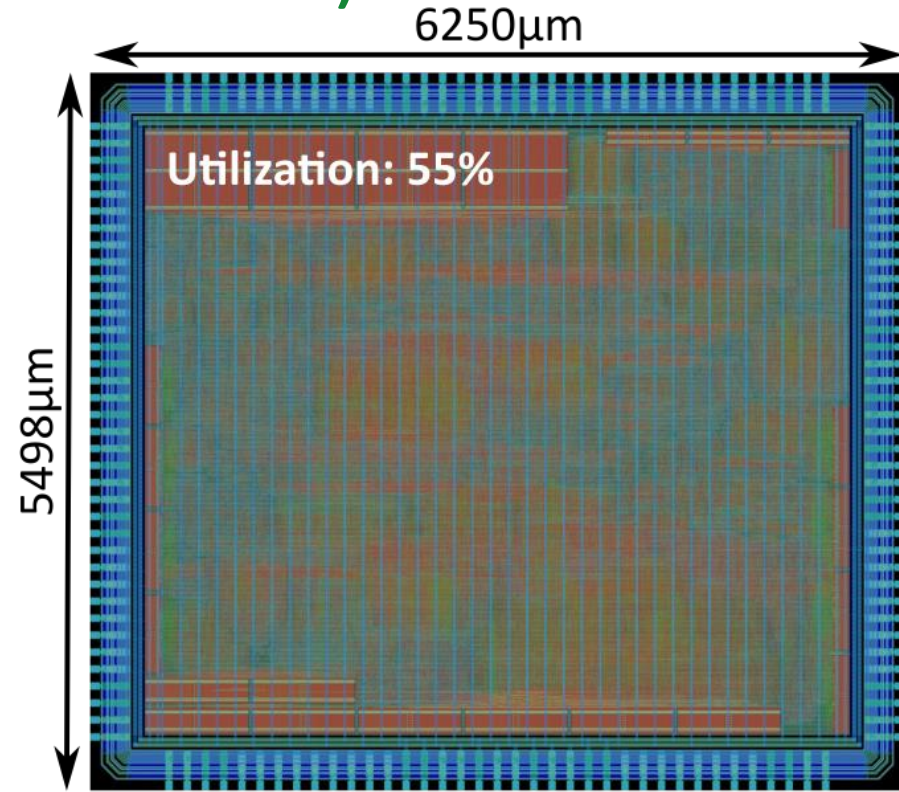


IHP130, tt-corner; Yosys-0.37 with optimized script if not mentioned otherwise

Basilisk: fully open SoC design (RTL to GDS)



- **Fully open flow**
 - GDS will be submitted in May 2024
- **Designed using IHP 130nm**
 - Open-source PDK
- **Collaboration with all main open-source EDA tool developers**
- **Key Metrics:**
 - 1.08MGE Logic
 - 13ns critical path
 - 6.25x5.5mm (34mm²)
 - 14.5h Runtime (+50% vs commercial)*



*2x 2.5GHz XeonE5-2670(10Core), max thread-count 20

In a nutshell: why open-source hardware & silicon?



- **It is a necessity**

- We can not afford to make everything ourselves, we need to collaborate
- Makes it possible to work together quickly
- Your results are more trustworthy, anybody can verify it!

- **It works**

- We have **more projects**, and **more funding** due to our open-source activities
- We were able to start many interesting and fruitful collaborations

- **It helps others as well**

- Many companies, universities, individuals are using pieces of PULP
- There is already significant commercial use, a lot we don't even know about



<http://pulp-platform.org>



@pulp_platform

The future of open-source silicon is bright!

