From an Open-Source ISA to Open-Source HW to Open-Source Silicon
Integrated Systems Laboratory (ETH Zürich)

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PULP Platform
Open Source Hardware, the way it should be!
Team of 100 people in ETH Zürich – University of Bologna

- Research on energy-efficient computing architectures
  - Started in 2013, celebrated 10 years of PULP last year

- Led by Luca Benini
  - Involves ETH Zürich (Switzerland) and University of Bologna (Italy)
  - Large group of almost 100 people
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Large group of almost 100 people
We have designed and tested more than 60 PULP ICs

<table>
<thead>
<tr>
<th>Year</th>
<th>IC Name</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>2013</td>
<td>PULPv1</td>
<td>STM 28FDXO Multicore processor</td>
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<tr>
<td>2014</td>
<td>Diana</td>
<td>UMC 65 4-core system with approximate FPUs</td>
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<tr>
<td>2015</td>
<td>Fulmine</td>
<td>UMC 65 4-core system with ML and Crypto accelerators</td>
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<tr>
<td>2016</td>
<td>VivoSoC 2.001</td>
<td>SMIC 130 Mixed signal system for biosignal acquisition</td>
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<tr>
<td>2017</td>
<td>Mr. Wolf</td>
<td>TSMC 40 8+1 core IoT processor</td>
</tr>
<tr>
<td>2018</td>
<td>Poseidon</td>
<td>GF 22FDX Dual 64bit RISC-V core, 3x 8core snitch clusters, Body biasing test vehicle</td>
</tr>
<tr>
<td>2019</td>
<td>Baikonur</td>
<td>TSMC 65 IoT processor with 16 cores and QNN enhancements</td>
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<tr>
<td>2020</td>
<td>Dustin</td>
<td>GF 22FDX IoT processor with Spiking Neural and Ternary Inference Engines</td>
</tr>
<tr>
<td>2021</td>
<td>Occamy</td>
<td>GF 12LPP ML accelerator with 216 + 1 cores and HBM interface</td>
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Check [http://asic.ethz.ch](http://asic.ethz.ch) for all our chips.
We believe in open source

- **Collaboration with many different domain experts**
  - We cannot afford to do everything in-house

- **No long discussions on IP ownership and background IPs**
  - Everything in the open

- **We can start right away**
  - Time is spent on design not necessary paperwork
  - The licensing settles most of the needed discussions (who owns it, who can do what)

- **Friendly licensing for commercial purposes**
  - Permissive licensing allows commercial exploitation, foreground of partners can be closed

- **You can see what we have and evaluate us in advance**
Many benefits are enabled by open source

Managing Complex Designs

Faster Collaborations

Facilitates Industry/Academia Relationships

Auditable Designs, Reproducible Results
Starting from an open-source ISA: RISC-V

- To enable open-source full HW systems, we need an open-source ISA
- We could not have open-source processors otherwise

A modern, open, free ISA, extensible by construction
Endorsed and Supported by ~4000 Members
Changed the picture on Computing Systems Research!

and many many more
RISC-V Open-Source Software

- Toolchains: GCC, LLVM
- System tools: BINUTILS, GDB, OpenOCD, Glibc, Musl, Newlib, ... and more
- Language Runtimes: C, C++, Fortran, GO, Rust, Java, Ocaml, ... and more
- Operating Systems: Linux: Fedora, OpenSUSE, Gentoo, OpenEmbedded/Yocto, Buildroot, OpenWRT, FreeBSD
  FreeRTOS, Zephyr, RTEMS, Xv6, HelenOS, ... and more

Huge momentum, extensible, open-source, patent troll safe

A wide SW ecosystem already available to evaluate and use RISC-V hardware systems

https://github.com/riscv/riscv-software-list
What PULP provides is a box of building blocks

**Platforms**
- **Single Core**
  - PULPissimo
  - Cheshire
- **Multi-core**
  - PULPOpen
  - Snitch Cluster
- **Multi-cluster**
  - Occamy
  - Carfield

**RISC-V Cores**
- RI5CY 32b
- Ibex 32b
- Snitch 32b
- Ariane 64b

**Peripherals**
- JTAG
- UART
- I2S
- DMA
- GPIO

**Interconnect**
- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

**IOT**
- Neureka (Convolution)
- RedMuLE (TinyML Training)
- CUTIE (Ternary DNN Inference)
- SNE (Spiking NN)

**HPC**
- Latch-Up 2024, Boston
All of our designs are open-source hardware

- All our development is on GitHub using a permissive license
  - HDL source code, testbenches, software development kit, virtual platform

https://github.com/pulp-platform

- Allows anyone to use, change, and make products without restrictions.

Heterogeneous Research Platform (HERO)

HERO is an FPGA-based research platform that enables accurate and fast exploration of heterogeneous computers consisting of programmable many-core accelerators and an application-class host CPU. Currently, 32-bit RISC-V cores are supported in the accelerator and 64-bit ARMv8 or RISC-V cores as host CPU. HERO allows to seamlessly share data between host and accelerator through a unified heterogeneous programming interface based on OpenMP 4.5 and a mixed-data-model, mixed-ISA heterogeneous compiler based on LLVM.

HERO’s hardware architecture, shown below, combines a general-purpose host CPU (in the upper left corner) with a domain-specific programmable many-core accelerator (on the right side) so that data in the main memory (in the lower left corner) can be shared effectively.

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PULP is released under the permissive Solderpad license, allowing anyone to use, change, and make products without restrictions.

Many of the GitHub Trending SystemVerilog repositories for the past months are:

- either directly from our group
- or have originated in our group
The open model led to successful industry collaborations

**Arnold (GF22)**
eFPGA with RISC-V core

**Vega (GF22)**
IoT Processor with ML acceleration

**Siracusa (TSMC16)**
IoT Processor with NVM technology

**Occamy (GF12)**
Chiplet based ML accelerator with 432 RISC-V cores
And many have used our work for their research.
Some (surprising) side effects of open-source hardware

• There is a surprising amount of bureaucracy involved
  • Code Ph.D. students/staff develop belongs to the university (they pay us)
  • Master/semester thesis students own the work they produce
  • Need to get proper approval for everyone involved

• Most agreements with companies are not meant for open source
  • Instead of paying for exclusive IP, we need sponsoring agreements
  • Important to make sure we do not sign anything that binds our open-source effort
From Open Hardware...
...to fully open-source IC design
Benefits of end-to-end openness

- **Research**
  - Easier collaboration (no NDAs)
  - Reproducing results
  - New research (using tools or data)

- **Education**
  - Increased access
  - Experiment with flows and tools
  - No black boxes, full transparency

- **Industry**
  - Transparent chain of trust
  - Lower initial cost
Open-source PDKs are the key

• Physical designs will contain technology relevant information
  • Nothing can be released (even if there were perfect open EDA tools) without technology info
  • So no open PDK no open source releases beyond RTL/HLS code

• IPs containing proprietary information on technology cannot be released
  • Open PDKs will allow us to change this

• Some good progress, more is needed
  • Skywater (130nm), IHP (130nm)
  • A 40nm/65nm open PDK would be a game changer, many viable products could be designed
Open-source EDA tools

- Open EDA tools work well and are improving fast
  - ETHZ is actively collaborating with UCSD
  - Currently working with Yosys (for synthesis) and OpenRoad (for PnR)
- Will not replace commercial EDA
  - A gap to PPA, service, support will remain
- Open source EDA will allow you to make your own chips
  - Good for many applications/needs
  - Will be great for teaching
- Summer school at ETH Zürich
  - June 3rd – 7th

https://efcl.ethz.ch/efcl-summer-school.html
Fully open IC design
• An open-source Linux-capable RISC-V MPU (based on https://github.com/pulp-platform/cheshire)
• Including a 64-bit RISC-V core (CVA6 - https://github.com/openhwgroup/cva6)
• About 1 MGE of logic
Open-source tool-flow

- Open-Source PDK (IHP 130nm)
- Pre-Process
  - Simplify SystemVerilog
  - Convert to Verilog
- Synthesis
  - Yosys from RTL to generic-cells
  - Calls ABC for logic optimization and mapping
- Place-and-Route
  - Collection of research tools into OpenRoad
Massive PPA improvements in 6 months

IHP130, tt-corner; Yosys-0.37 with optimized script if not mentioned otherwise

Latch-Up 2024, Boston
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Area Reduction: 1.6x
Maximum Frequency: 3.5x

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Basilisk: fully open SoC design (RTL to GDS)

- Fully open flow
  - GDS will be submitted in May 2024

- Designed using IHP 130nm
  - Open-source PDK

- Collaboration with all main open-source EDA tool developers

- Key Metrics:
  - 1.08MGE Logic
  - 13ns critical path
  - 6.25x5.5mm (34mm²)
  - 14.5h Runtime (+50% vs commercial)*

*2x 2.5GHz XeonE5-2670(10Core), max thread-count 20
In a nutshell: why open-source hardware & silicon?

- **It is a necessity**
  - We can not afford to make everything ourselves, we need to collaborate
  - Makes it possible to work together quickly
  - Your results are more trustworthy, anybody can verify it!

- **It works**
  - We have more projects, and more funding due to our open-source activities
  - We were able to start many interesting and fruitful collaborations

- **It helps others as well**
  - Many companies, universities, individuals are using pieces of PULP
  - There is already significant commercial use, a lot we don’t even know about
The future of open-source silicon is bright!