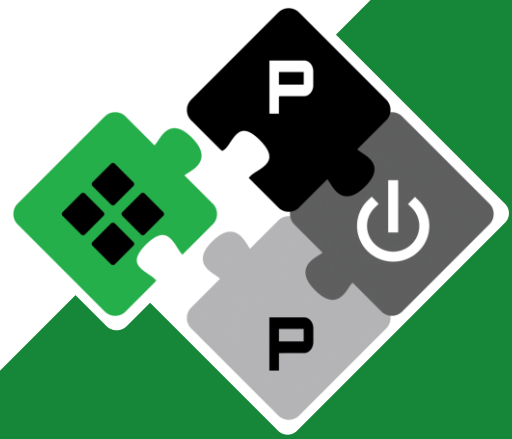
ETH zürich

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

Scaling Up Event-based Many-Core System Simulation with GVSoC

Integrated Systems Laboratory (ETH Zürich)

Rafael Medina Morillas medinar@iis.ee.ethz.ch



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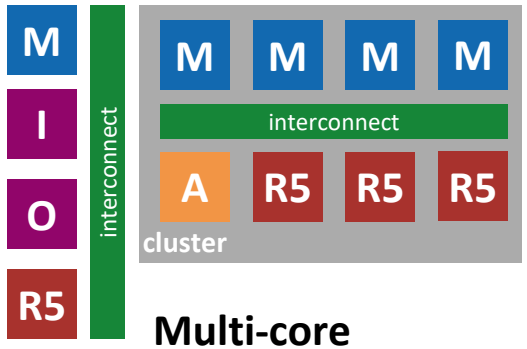
PULP Platform

Open Source Hardware, the way it should be!

Scaling Up Research on RISC-V Systems

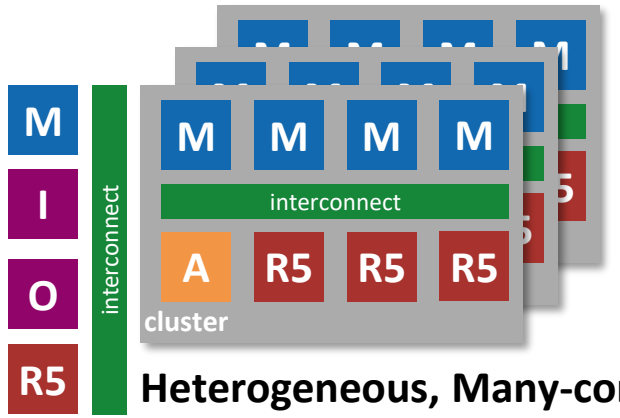
Single core

- PULPino, PULPissimo
- Cheshire



Multi-core

- OpenPULP
- ControlPULP



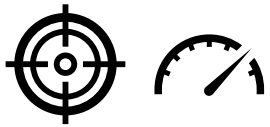
Heterogeneous, Many-core

- Hero, Carfield, Astral
- Occamy, Mempool

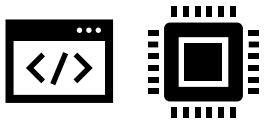
IOT → **HPC**

Simulation approaches need to scale at the same rate

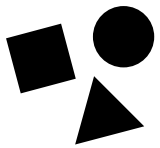
System-level Simulation



- **Assess hardware and end-to-end applications**
  - Performance and power insights
  - Fast deployment iterations



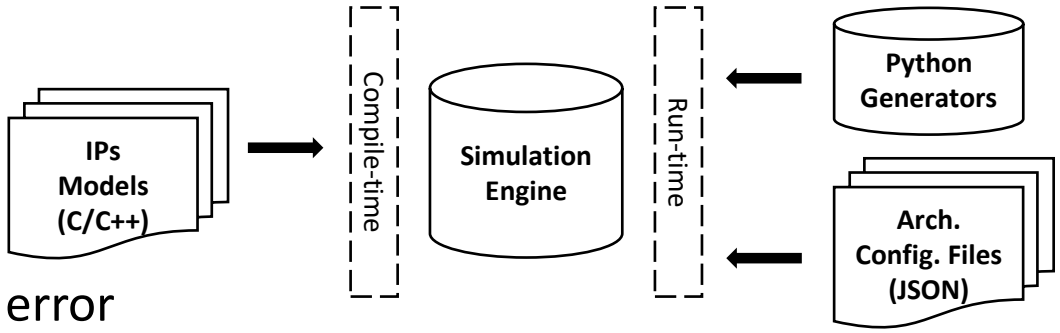
- **Target accuracy while keeping simulations fast**
  - Calibrated with RTL
  - Modeling scaled-up and scaled-out systems



- **Flexible and extensible**
  - Heterogeneous systems → wide variety of designs
  - Explore novel architectural techniques

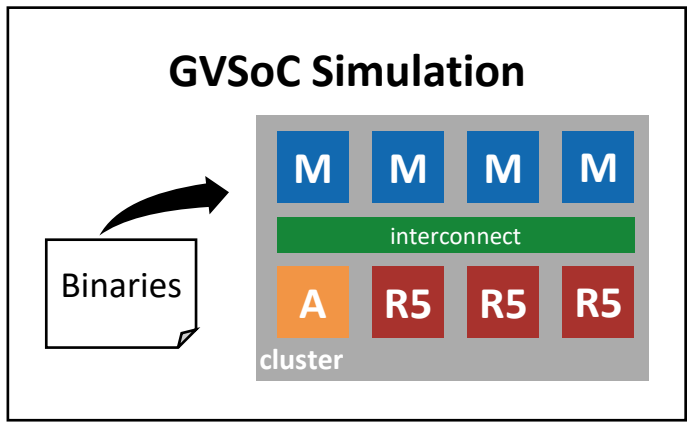
GVSoC [1]: System-level Simulation for RISC-V Platforms

- **Event-based simulation**
  - > 100x faster than RTL simulations
  - Calibrated with PULP components → < 10% timing error



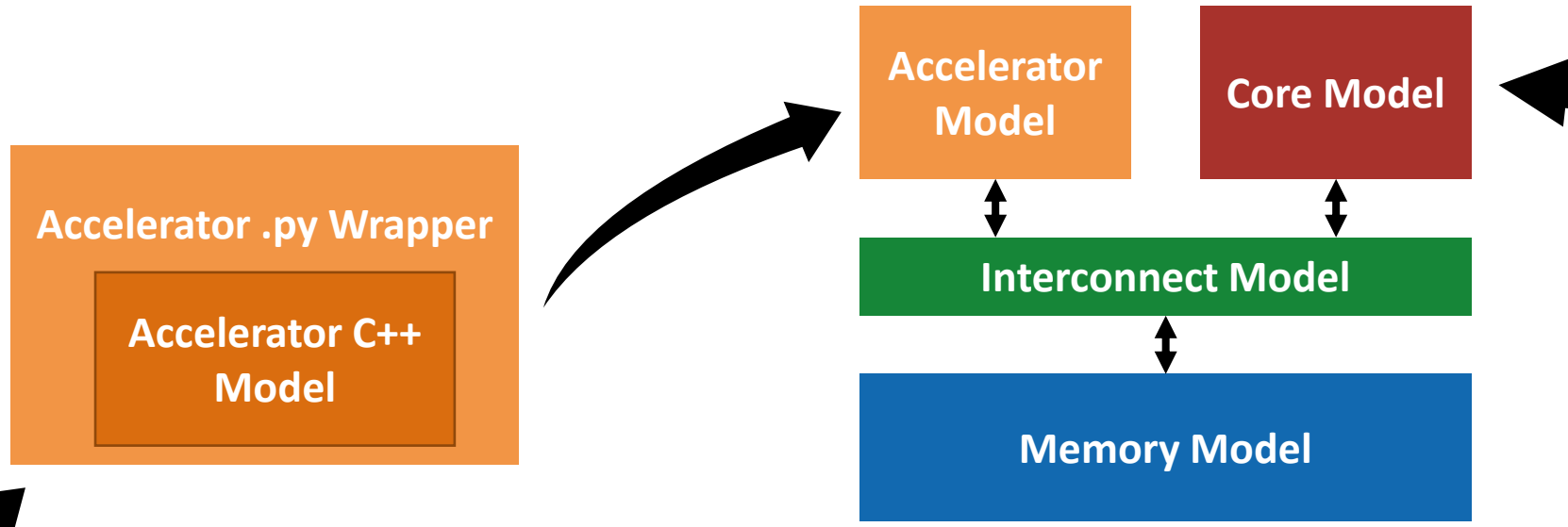
- **Modeling entire system**
  - CPUs, accelerators, caches, memories, I/O…
  - Running unmodified binaries

- **Generic interface and component encapsulation**
  - Easily extended with new architectures



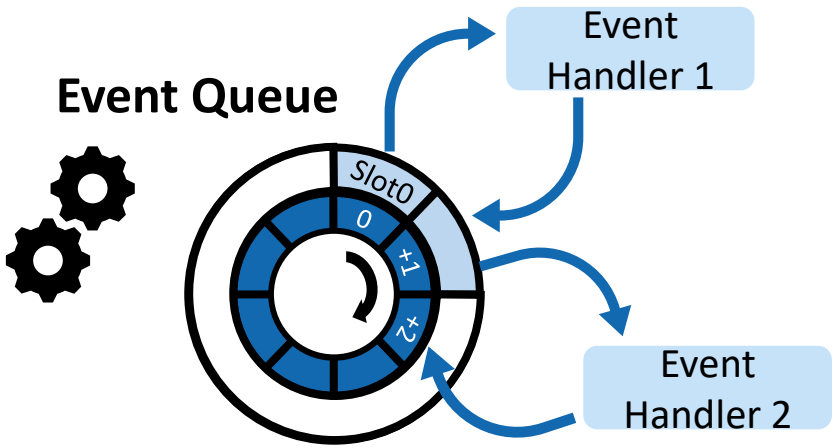
[1] N. Bruschi et al, ICCD 2021

GVSoC Structure

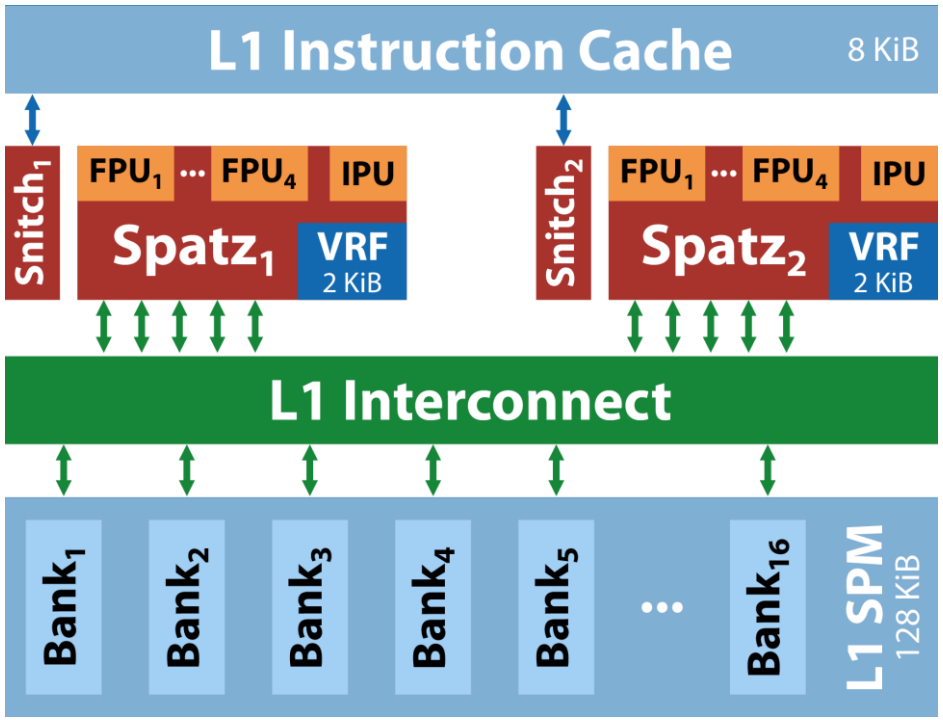


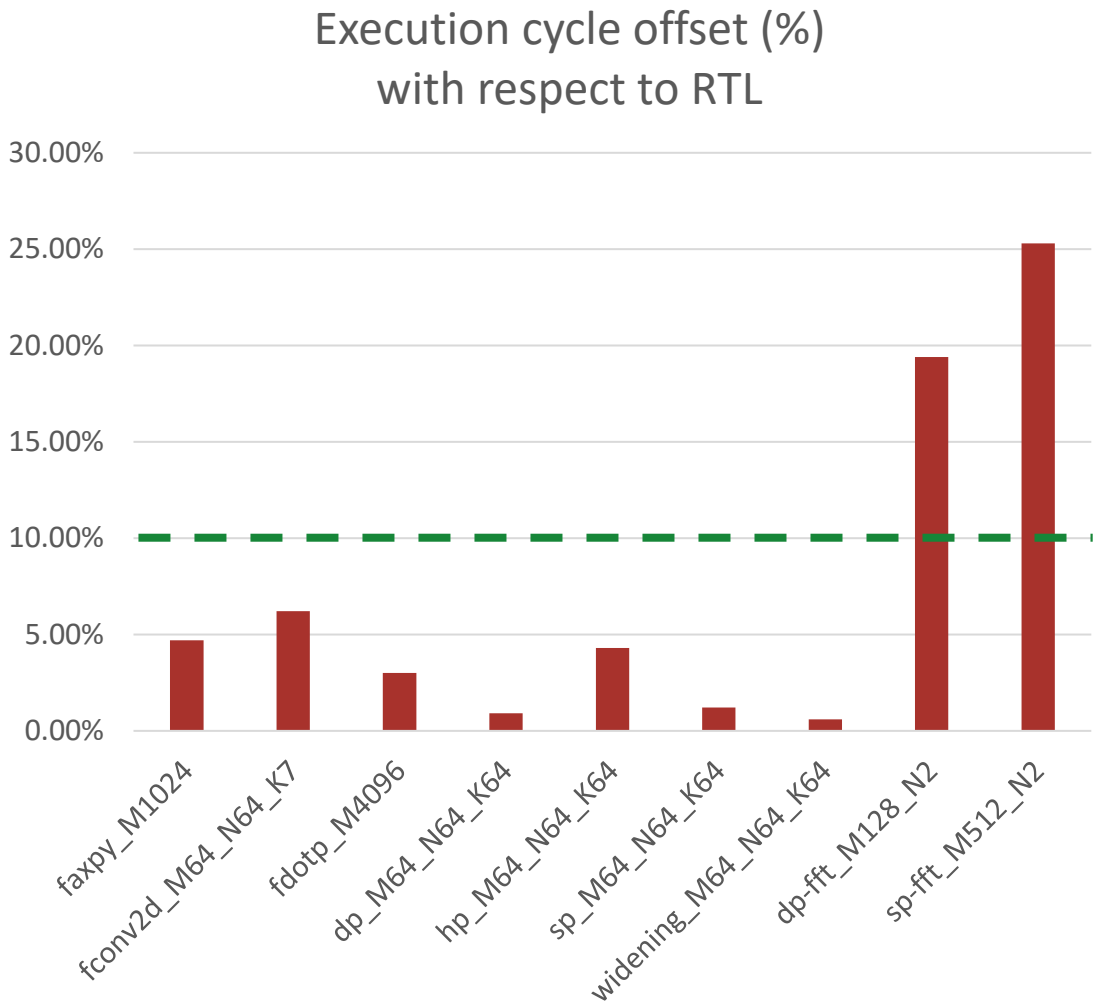
- **Instruction Set Simulator**
  - RV32
  - RV64
  - RVV
  - …

- Component behavior
- Ports
- Modifiable parameters
- Optional power model



Spatz Example

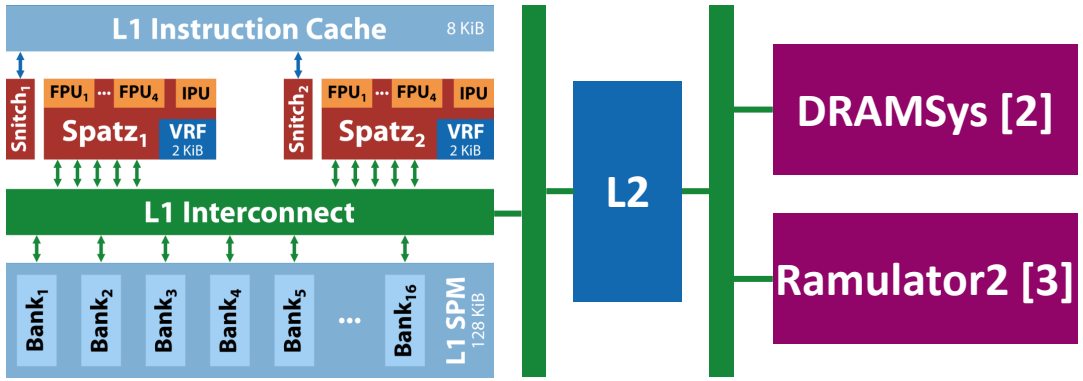




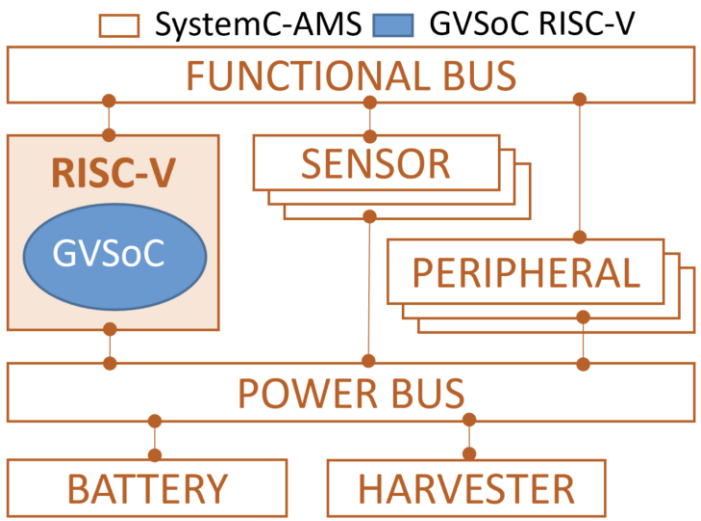
- **Up to 100× runtime speed up**
- **< 10% relative error (except FFTs)**

Two Kinds of Interface with Other Simulators

- **Instantiating a simulator as a GVSoC component**
  - Communication through the Python and C++ component wrappers
  - **Example:** modeling DRAM integration



- **Controlling GVSoC from an external simulator**
  - GVSoC provides a C++ API to control its execution
  - **Example:** modeling an Analog/Mixed-Signal system integrating RISC-V SoC [4]

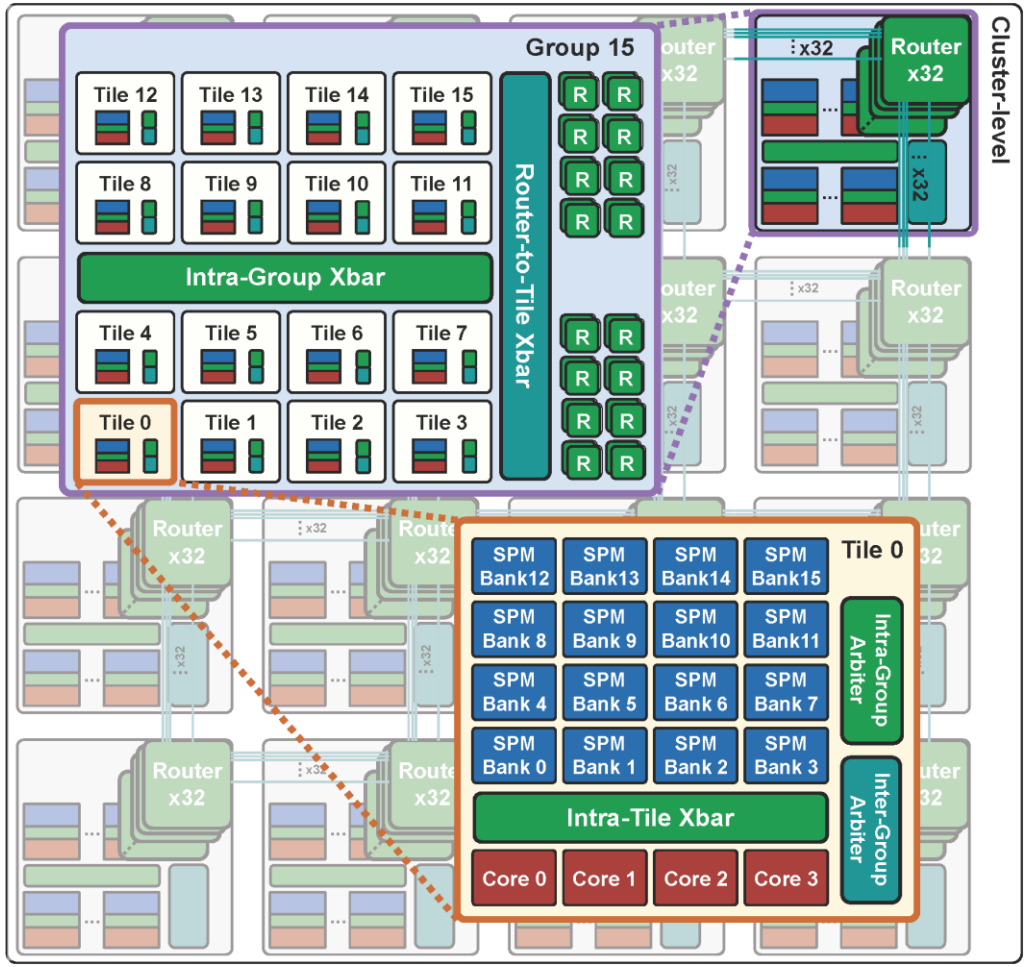


[2] L. Steiner et al., IJPP 2022 [3] H. Luo et al., ArXiv 2026 [4] M. Hamdi et al, CF Companion 2024

Scaling Up Systems: TeraNoC

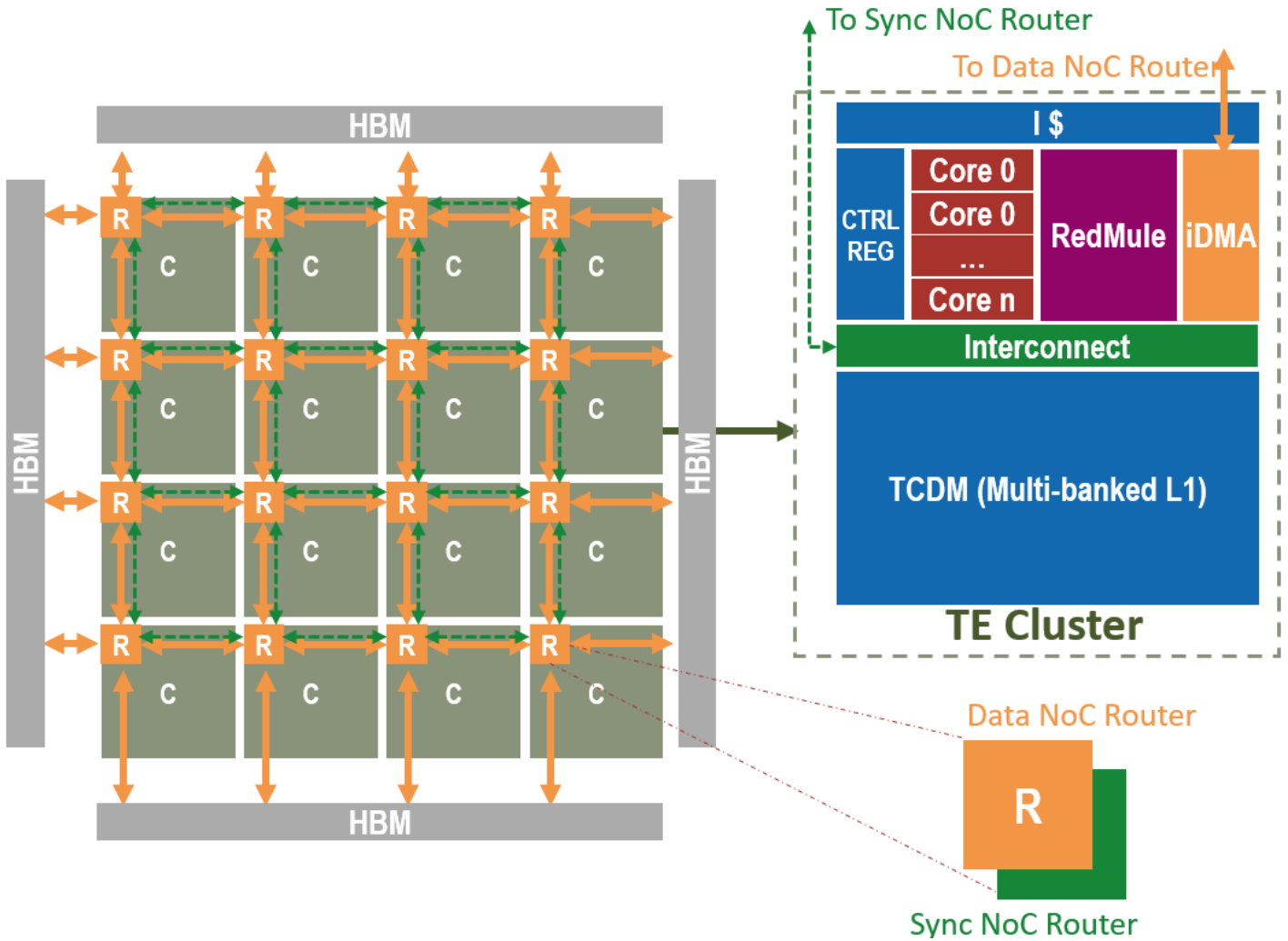
- **1024 cores sharing a L1 NUMA**
  - 4 cores in a tile connected via crossbar
  - 16 tiles in a group connected via crossbar
  - 16 groups connected via mesh NoC
- **Mixing sync-async modeling of interconnects [5]**
  - Balance speed vs. accuracy

< 7% error and 115x speedup over RTL



[5] Y. Li et al., ISVLSI 2026

Multi-cluster Systems: SoftHier



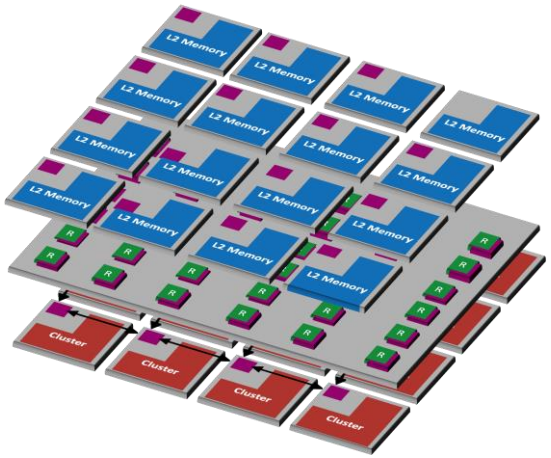
- **Exploration platform for multi-cluster NoCs [6]**
  - Heterogeneous architectures
  - Broadcast and reduction at the NoC routers
- **How to map MHA and transformers**
  - Achieving up to 4x speedup over FlashAttention-3

What next?

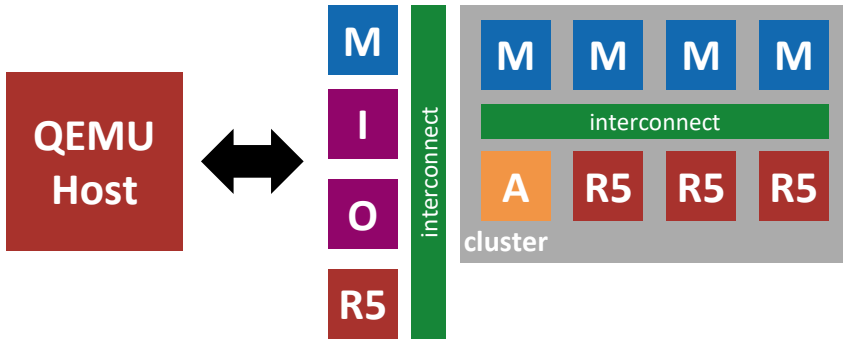
[6] C. Zhang et al., ArXiv 2026

Next Directions

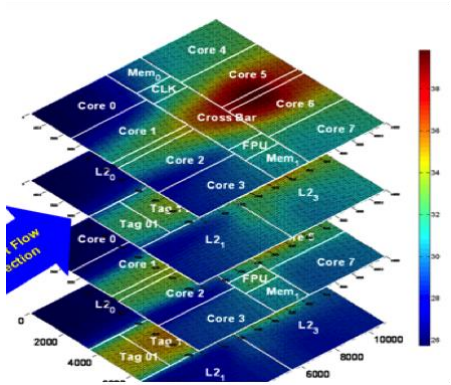
- **NoC Topology Explorations**



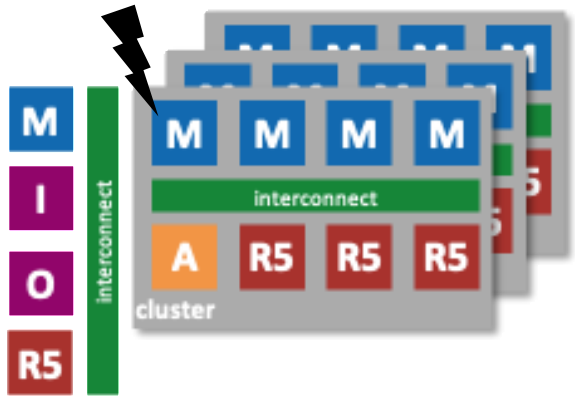
- **Interfacing with QEMU as a PCIe**



- **Thermal Co-simulation with 3D-ICE**



- **System-level Fault Injection**



Conclusions

- **GVSoC for fast and accurate simulation of RISC-V-based heterogeneous systems**
  - From single core to many-cluster
- **Easy interface with other simulators**
  - Either as main system or subsystem
- **Exploring new architectures**
  - 1024 cores and beyond
  - New accelerators
  - NoC fabrics

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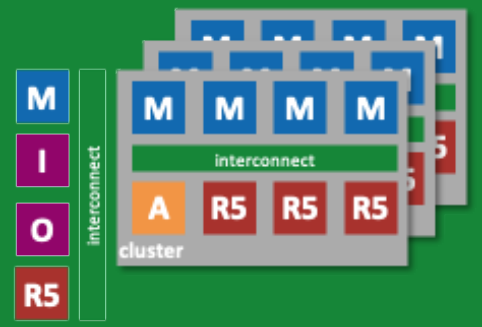

Rafael Medina Morillas (medinar@iis.ee.ethz.ch)

Q&A

pulp-platform.org
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company/pulp-platform
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Institut für Integrierte Systeme, ETH Zürich
Gloriastrasse 35
Zürich, Switzerland

DEI, Università di Bologna
Viale del Risorgimento 2
Bologna, Italy

ETH zürich
ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA