F-3: Design and Experimental Investigation of Trikarenos: A Fault-Tolerant 28nm RISC-V-based SoC

RADECS 2024 – Radiation Hardening Techniques

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RISC-V up and coming

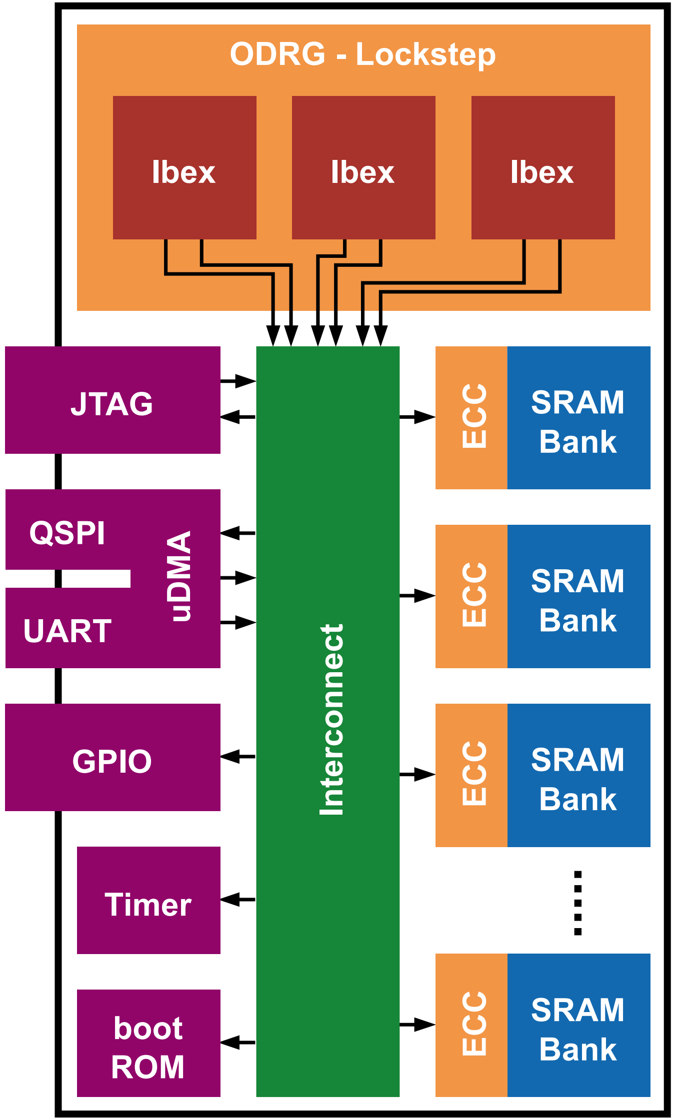
- **RISC-V is gaining traction in Space & Automotive domains**
- **Reliability is required**
  - RISC-V is ideally suited -> open ISA
- **Initial Designs are becoming available**
  - Commercial: NASA HPSC, NOEL-V
  - Academic projects: Trikarenos
- **Radiation evaluation needed**
  - Processor susceptibility
  - Strength of protection mechanisms

Contributions

- **Reliability investigation of Trikarenos SoC design**
  - Lockstepped RISC-V cores
  - ECC-protected memory
- **Evaluation under *Neutron* and *Proton* radiation**
  - Neutron beam experiments at *ChipIR*
  - Proton beam experiments at *HollandPTC*
- **Analysis of SRAM error rates**
  - Effectiveness of ECC mechanism & scrubbing
- **Analysis of processor core error rates**
  - Effectiveness of Lockstep mechanism

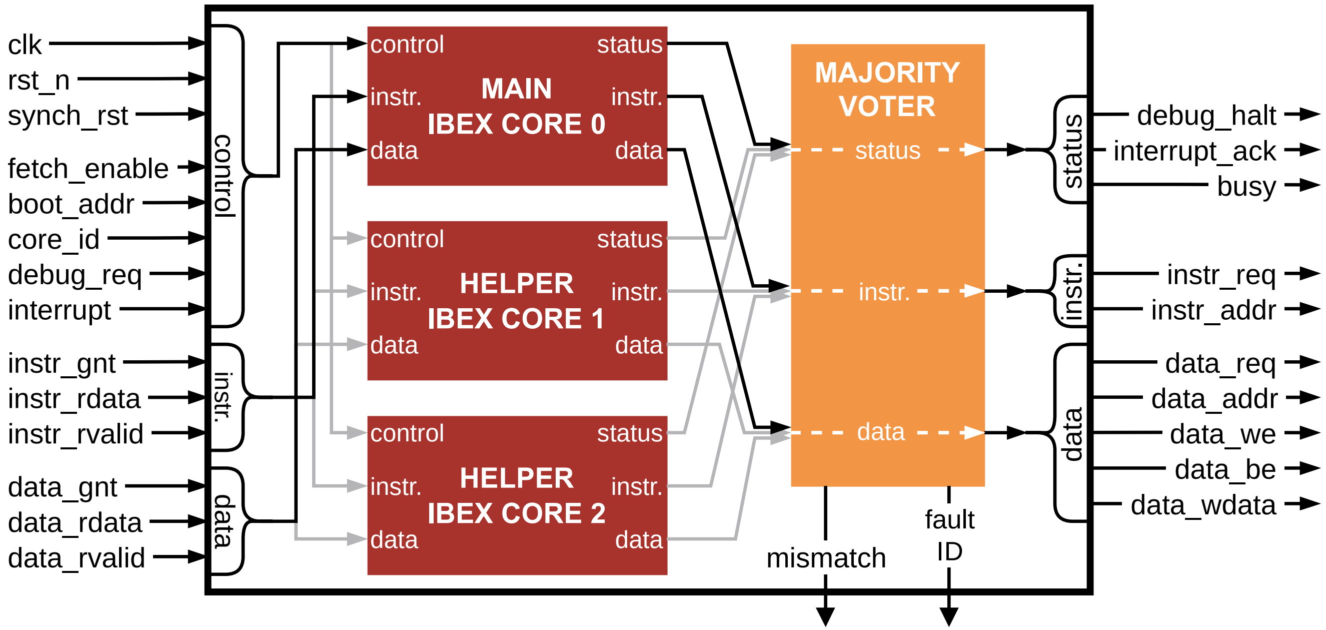
Trikarenos Design

- **PULPissimo-based SoC Design**
  - Modified for reliability
- **Three locksteped cores with voting**
- **ECC-protected memory**
- **Peripherals**
  - UART
  - QSPI
  - GPIO
- **JTAG for programming and internal access**
- **Low-latency interconnect**



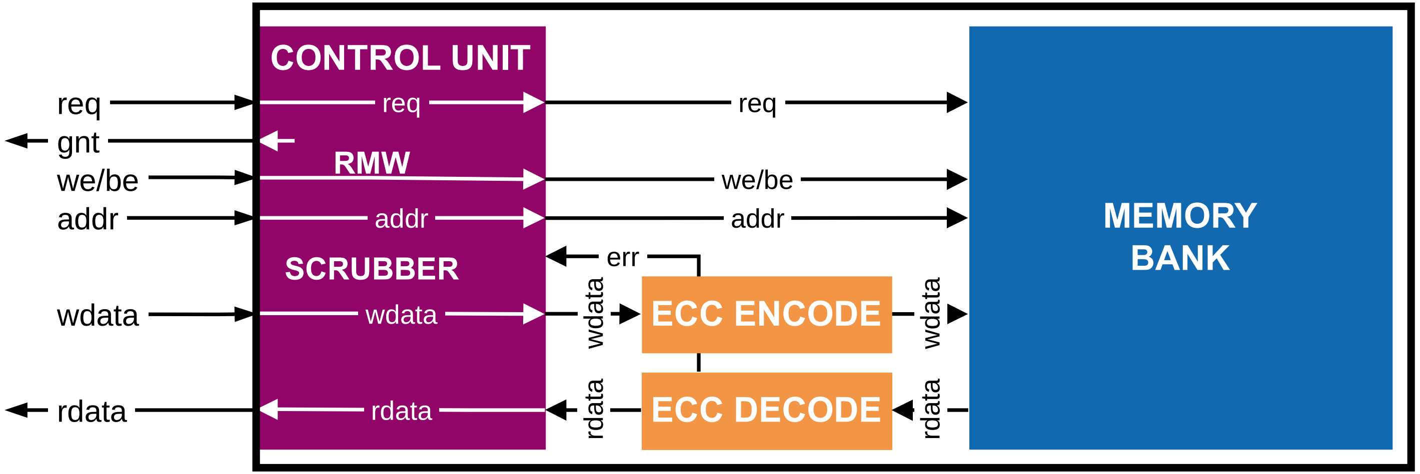
Core Lockstep Mechanism

- **Identical inputs**
  - Ensures identical operations
- **Voting on outputs**
  - Determine correct signal values
- **Internal state requires re-synchronization**
  - Saved to memory, state reset, loaded from memory
- **Switchable**
  - Can be disabled for parallel performance



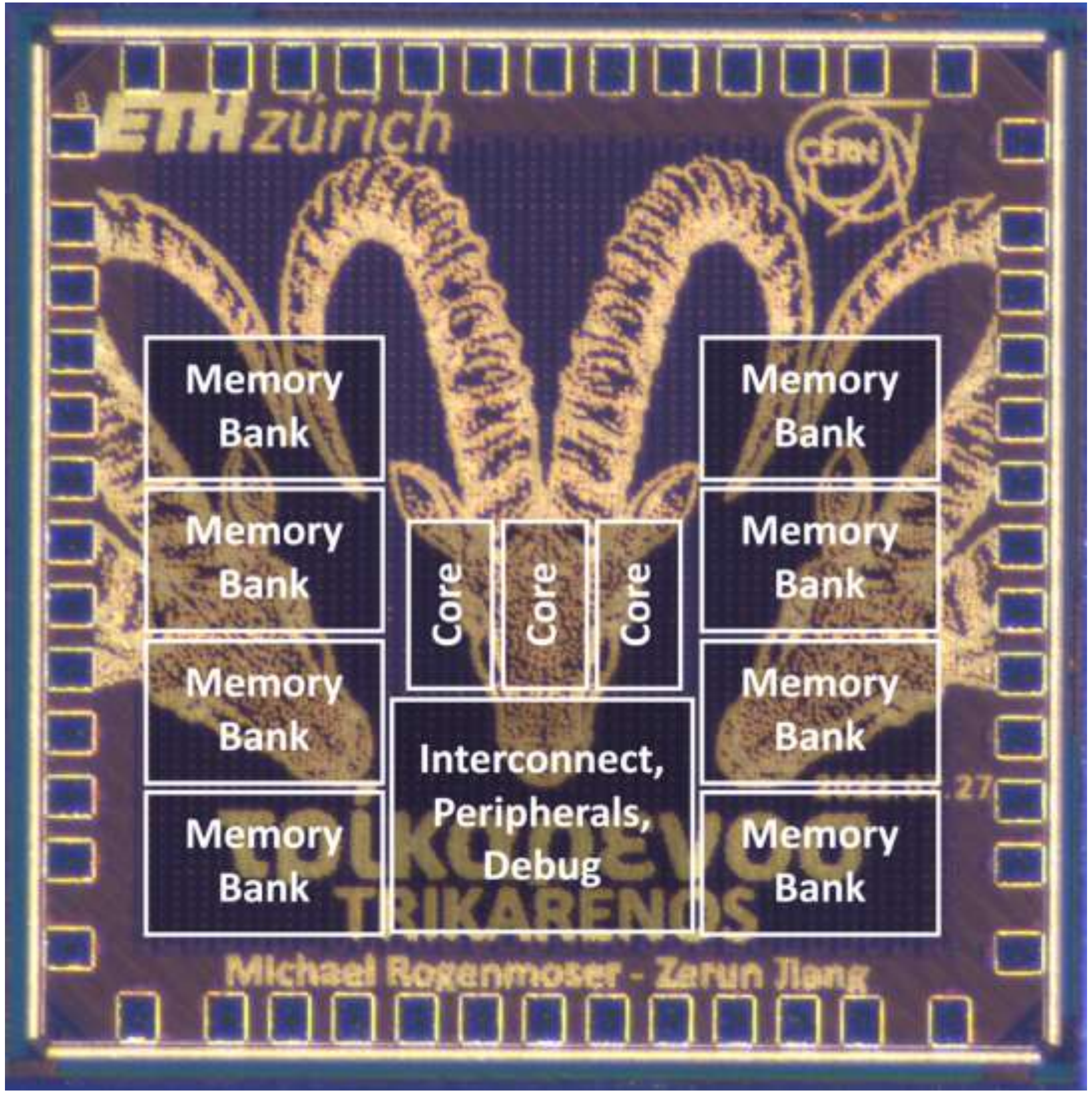
ECC memory

- **Hsiao code for efficient encoding**
  - Single Error Correction, Double Error Detection
- **32bit word stored as 39bit with parity**
- **Read-modify-write for efficient byte-wise access**
- **Scrubber for continuous correction**
  - Avoids latent errors causing uncorrectable error



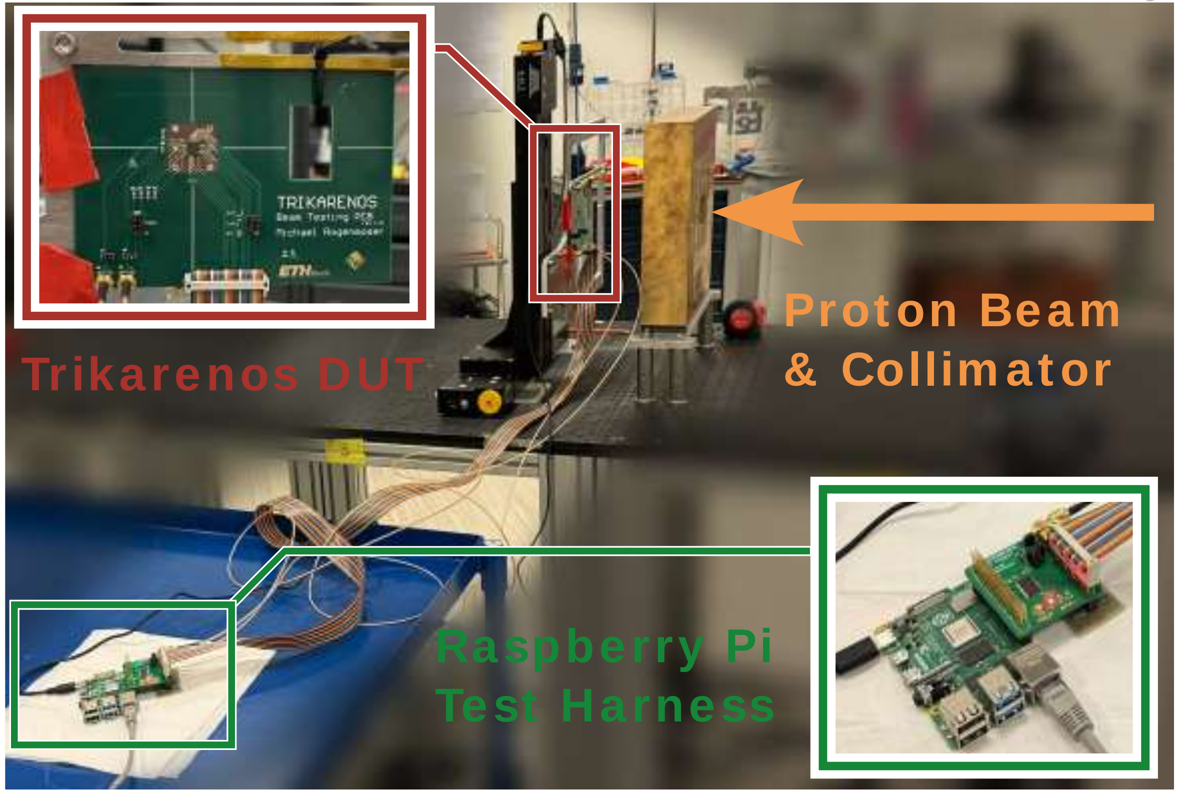
Trikarenos implementation

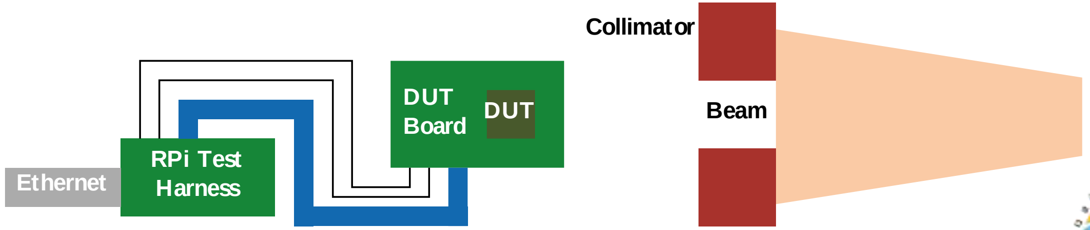
- **Implemented in TSMC 28nm**
  - TID tolerance previously investigated
- **Standard cells**
  - No hardened cells
- **Standard flows**
  - No additional protections (clock/reset tree)
- **Physical separation for cores**
  - Ensures single particle does not cause SEU in multiple cores
- **250MHz target, operating at 125MHz**
  - 0.9V core, 1.8V I/O



Experimental Setup

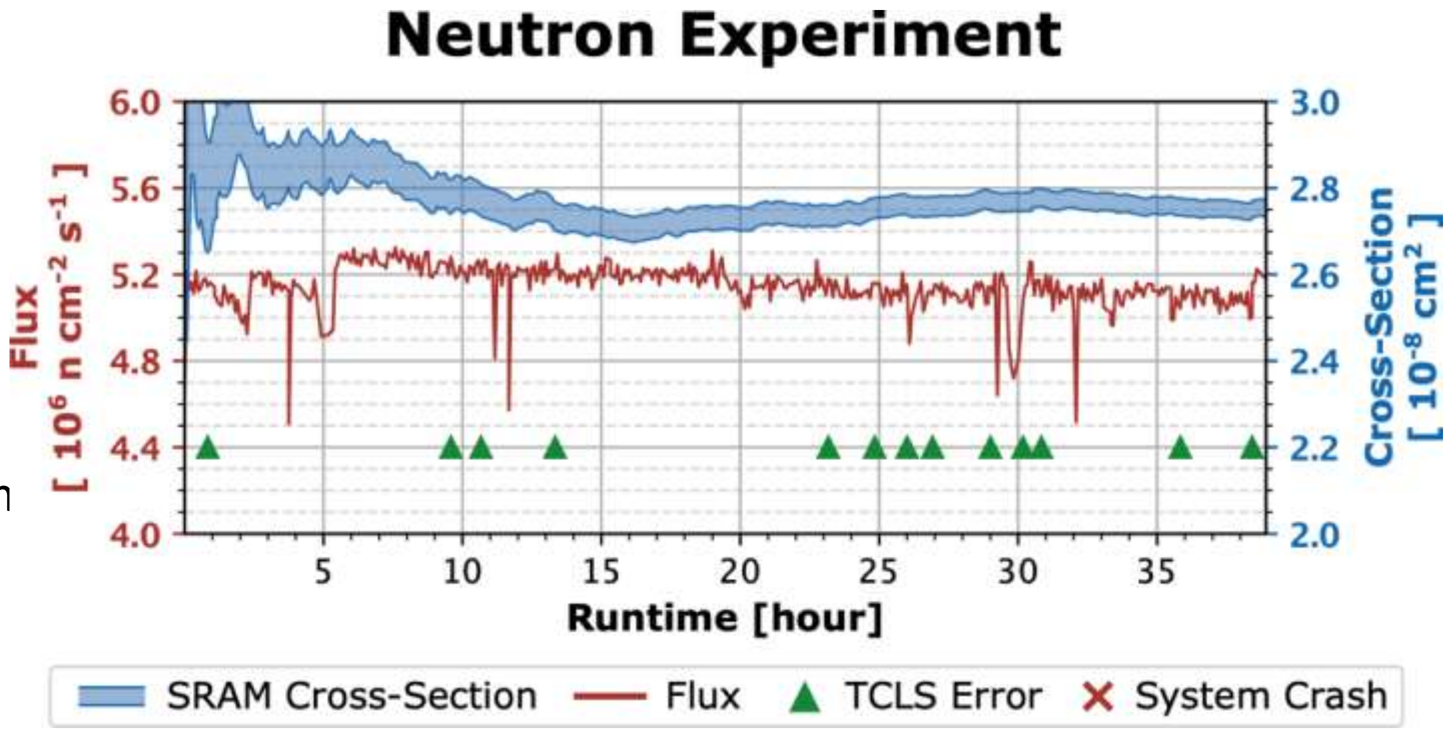
- **Trikarenos standalone on PCB**
- **Raspberry Pi**
  - For programming and monitoring
  - Stores data
  - Ethernet to transmit outside & control
- **Application on Trikarenos**
  - Coremark
  - Register operations to accumulate errors and detect TCLS correction
  - GPIOs
    - Heartbeat
    - Exception signalling





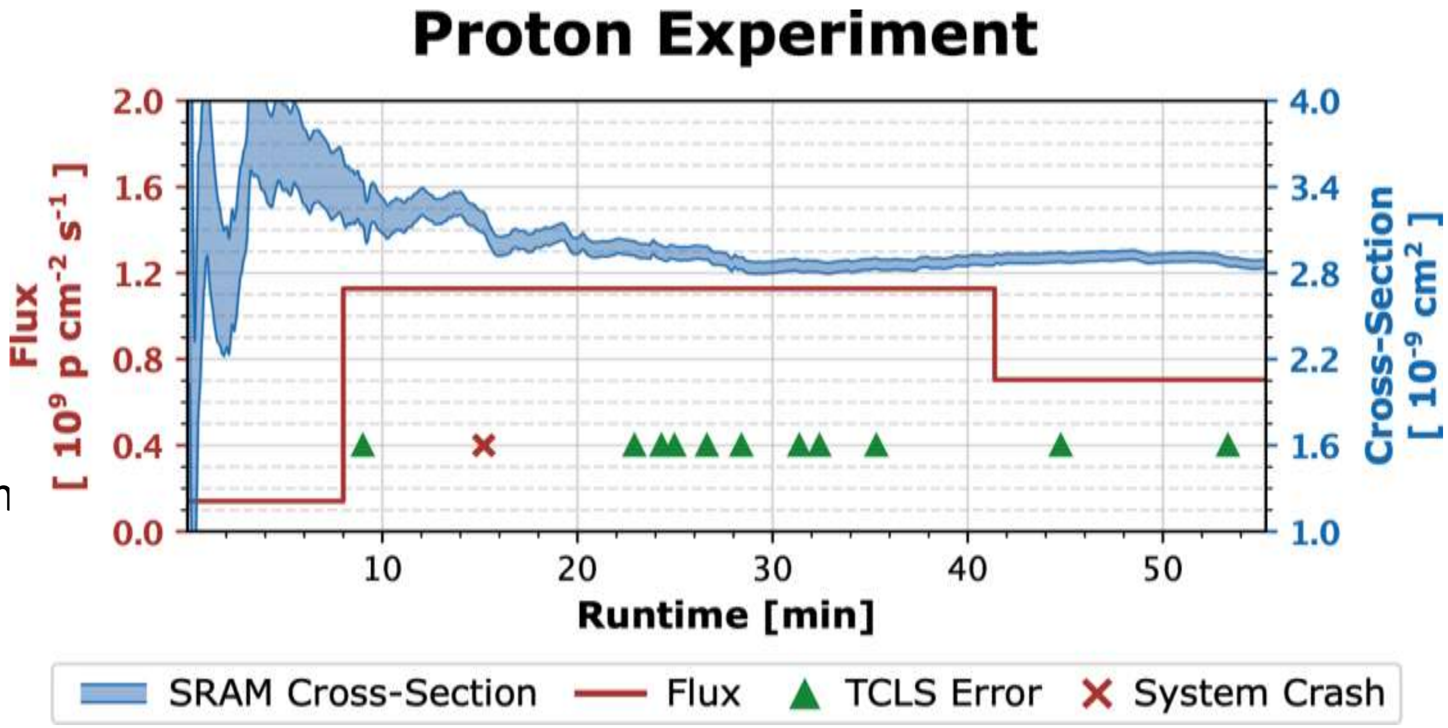
Experimental Results – Neutrons @ ChipIR

- **Neutrons**
  - Atmospheric energy distribution
  - Flux: 5×10^{6} n cm^{-2} s^{-1}
  - Total Fluence: 6.88×10^{11} n cm^{-2}
- **SRAM errors**
  - 18’786 errors
  - Cross-section: $(2.75 \pm 0.02) \times 10^{-8}$ cm
  - 256KiB usable: 2’555’904 bits: $(1.08 \pm 0.01) \times 10^{-14}$ cm^2 bit^{-1}
- **Lockstep:**
  - 13 errors: $(2.55 \pm 0.68) \times 10^{-11}$ cm^2
  - 0 system errors: $< 5.36 \times 10^{-12}$ cm^2



Experimental Results – Protons @ HollandPTC

- **Protons**
  - 200 MeV
  - Flux: Up to 1.13×10^{9} p cm^{-2} s^{-1}
  - Total Fluence: 2.91×10^{12} p cm^{-2}
- **SRAM errors**
  - 8’249 errors
  - Cross-section: $(2.86 \pm 0.03) \times 10^{-9}$ cm
  - 256KiB usable: 2’555’904 bits: $(1.12 \pm 0.01) \times 10^{-15}$ cm^2 bit^{-1}
- **Lockstep:**
  - 11 errors: $(5.25 \pm 1.51) \times 10^{-12}$ cm^2
  - 1 system errors: $< 1.91 \times 10^{-12}$ cm^2



- **1.77×10^{3} Gy during experiments**
  - No degradation observed

Memory Error Analysis

- **$(1.08 \pm 0.01) \times 10^{-14}$ cm^2 bit^{-1} for neutrons**
- **$(1.12 \pm 0.01) \times 10^{-15}$ cm^2 bit^{-1} for protons**

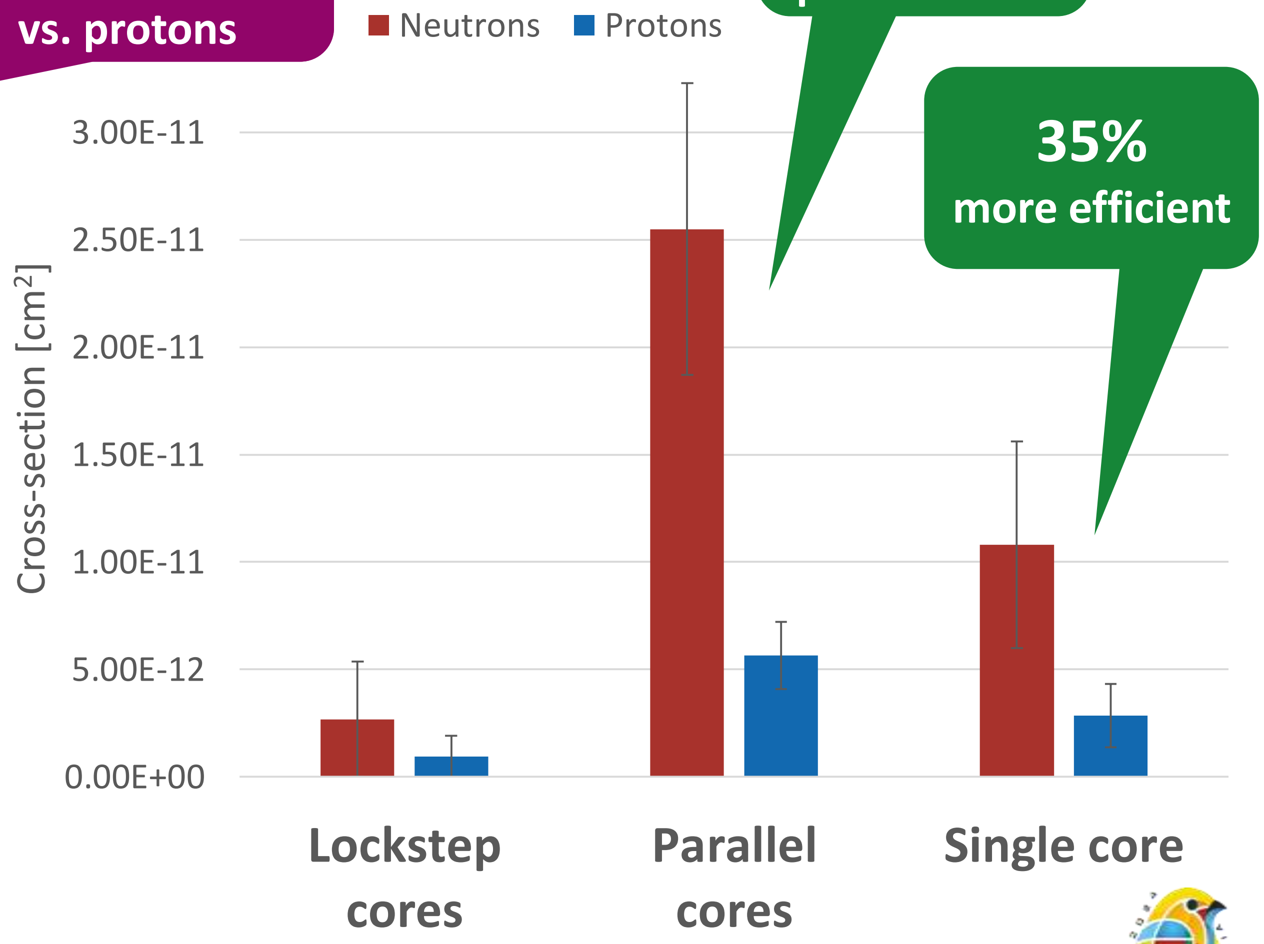
9 ×
higher for neutrons vs. protons

- ***9x* higher for neutrons vs. protons**
  - Large difference could relate to energies, particle types, …
- **Scrub rate can be tuned**
  - One scrubber per bank, 8 banks, each 8192 words
  - 1 scrub every 6225 cycles catches all errors

Lockstep and System Error Analysis

- **Lockstep cross-section**
  - $(2.55 \pm 0.68) \times 10^{-11}$ cm^2 for neutrons
  - $(5.25 \pm 1.51) \times 10^{-12}$ cm^2 for protons
- **System failure cross-section**
  - $< 5.36 \times 10^{-12}$ cm^2 for neutrons
  - $< 1.91 \times 10^{-12}$ cm^2 for protons
- **Should we disable Lockstep?**

5 × higher for neutrons vs. protons

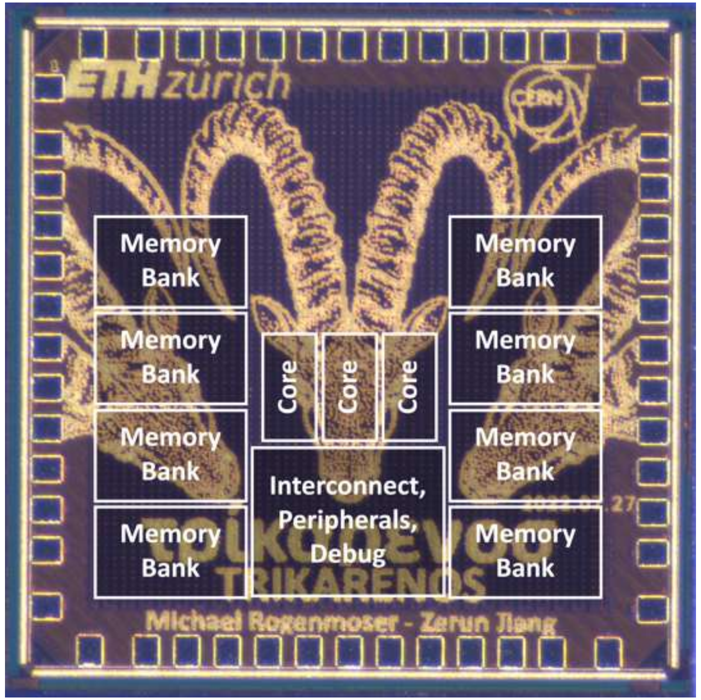


2.96 × more performance

35% more efficient

Conclusion

- **Trikarenos' protected RISC-V SoC architecture**
  - Lockstep cores for correct processing
  - ECC Memory for data consistency
- **Experimental Investigation with atmospheric neutrons and 200 MeV protons**
  - SRAM neutron vulnerability: (**1.08** ± 0.01) × $\mathbf{10^{-14}}$ cm^2 bit^{-1}
  - SRAM proton vulnerability: (**1.12** ± 0.01) × $\mathbf{10^{-15}}$ cm^2 bit^{-1}
  - Lockstep: improves reliability by **>3.5 ×**
    from (2.55 ± 0.68) × 10^{-11} cm^2 to below 5.36 × 10^{-12} cm^2
- **Extended with simulation-based fault injection for TNS special issue**
- **Targeting space mission in early 2025**



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Q&A

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