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December 8-10 | Virtual Event

CORE-V MCU SoC
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RISC-V® Summit

riscvsummit.com #RISCVSUMMIT
CORE-V MCU SoC, Open Source, 22nm MCU with Embedded FPGA

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History

• Both platforms originate from the PULP Project: Tuned for energy-efficiency

• CORE-V MCU is derived from PULPissimo
  • Efficient micro-controller
  • Improved CV32E40P
  • Standardized OBI protocol
  • APB for µDMA subsystem

• CORE-V APU is derived from Ariane’s SoC
  • UNIX-capable system
  • Minimal infrastructure to demonstrate the core
  • AXI-based
  • Xilinx Peripherals (SPI, DW converter)
CORE-V MCU

• Shared memory
  • Unified Data/Instruction Memory

• Support for Accelerators
  • i.e., HW Processing Engine (HWPE)
  • Direct shared memory access
  • Programmed through APB bus

• μDMA for I/O subsystem
  • Can copy data directly from I/O to memory without involving the core

• Used as controller in larger systems

https://github.com/openhwgroup/core-v-mcu
CORE-V MCU

• Rich set of peripherals for edge AI sensors (vision and time series):
  • QSPI (up to 280 Mbps)
  • Camera Interface
  • I2C/I2S
  • JTAG, GPIOs
  • Interrupt controller
  • boot ROM

• Custom accelerators for ML use cases

https://github.com/openhwgroup/core-v-mcu
PULP Interrupt Controller

• Generates up to 32 requests
  • Events vs. interrupts
• Mapped on the APB bus
• Receives events in a FIFO from the SoC event generator
  • Unique interrupt ID
• Mask, pending, ack, event id registers
• Special set, clear, read, write operation registers

• Sources:
  • Timers
  • GPIO
  • Custom accelerator
  • Events from the uDMA

• CV32E40P
  • Support for standardized and “fast” RISC-V interrupt mechanisms
Example for a Custom Accelerator

CTRL FSM
UCODE PROC
REG FILE SLAVE

INPUT BUFFER
TP-bit

XNOR & POPCOUNT
TP xnor + reduction tree to 16-bit

POPCOUNT ACCUMULATORS
TP x 16-bit

THRESHOLD
TP-bit

INPUT SOURCE
WEIGHT SOURCE
OUTPUT SINK

TP/32 x 32-bit memory master
STATIC MUXING

TP-bit stream

32-bit APB

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CORE-V MCU Physical Design

• Two realizations:
  • FPGA - Digilent Nexys A7 or Genesys 2
  • ASIC - GLOBALFOUNDRIES 22FDX

• ASIC coming early next year
  • Including Quicklogic eFPGA

• Prototype your custom accelerator for AI/ML applications
  1. FPGA
  2. eFPGA
OpenHW Group
BHAG
BIG HAIRY AUDACIOUS GOAL
APU & MCU SoCs

- Production Ready
- Using CORE-V CVA6 & CVE4 Cores
- Deep Sub-Micron SoCs
- On evaluation boards
- Running Linux / FreeRTOS
- Tapeout CORE-V MCU ~Q1’2021
Case Study: ETH Zurich “Arnold” Test Chip Platform

- ~600MHz, 3mm x 3mm die size on GF22FDX
- RISC-V with QuickLogic ArcticPro 2 eFPGA
Arnold – Heterogenous, Energy-Efficient Architecture

• Features
  • RISC-V General Purpose Processor
  • 512 KiB on-chip Memory
  • Broad set of peripheral I/O with memory access via µDMA
  • Tightly coupled eFPGA that supports
    • Direct connection to I/O
    • Shared memory accelerator interface
    • I/O filtering functions
    • Config and control interface to/from system

• Benefits
  • Energy efficient architecture enables flexibility to implement hardware partitioning of software requirements
  • Lower unit cost than vs discrete MCU / discrete FPGA implementations
  • OTA hardware upgrades
  • Lower NRE cost vs ‘spinning an ASIC’ for each derivative

• Project announced at OSDForum Sept 2020
• Real Time Operating System (e.g. FreeRTOS) capable ~600+MHz CV32 MCU host CPU
• Embedded FPGA fabric with hardware accelerators from QuickLogic
• Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc.) for interfacing with sensors, displays, and connectivity modules
• Built in 22FDX with GF
Software

• The SDK contains all the tools and runtime support for CORE-V based microcontrollers

• Provides:
  • HAL
  • crt0 and linker scripts
  • higher level functions (API)

• CORE-V toolchain and SW ecosystem under development

Get involved: https://github.com/openhwgroup/core-v-sw
Current Status

• CORE-V MCU CV32E40P running on Genesys 2 with simple runtime
  • Code built with Embecosm’s CORE-V GCC development tools
  • GDB/OpenOCD debug
  • Come join us and contribute at: https://github.com/openhwgroup/core-v-mcu

• CORE-V MCU with Ashling RiscFree/Opella-XD JTAG probe running on Genesys 2
Next Steps

• Further testing and debugging of the implementation
• Integration of more system peripherals
• More complex SDK
• Architectural enhancements, such as implementing Open Bus Interface with CV32 now supports
• Integration/validation of proprietary and open-source tools (hardware, software)
• Training materials, demos

Looking for collaborators to help!
CORE-V APU

- Minimum set of peripherals to boot Linux
- Code is on SD Card
- Zero-stage bootloader is in boot ROM
- UART as main UI
- Ethernet for network connectivity

https://github.com/openhwgroup/cva6
CORE-V MCU & APU FPGA

- Default Board: **Genesys 2**
  - Wide-spread adoption
  - Rich set of board peripherals
  - Reasonably cheap (discounts through OHW, academics)

- Alternative: **Nexys A7**
  - Cheaper
  - Higher availability

- “User ports“:
  - VC707, KC705
  - Ultrascale Boards
RISC-V Debug

- Draft specification 0.13
- Defines debug registers for
  - run/halt/single-step
  - reading/writing GPR, FPR and CSRs
  - Querying hart status
- JTAG interface
- OpenOCD support
- Our choice: **Execution Based**

- Standard allows for different debug probes to be used
- IDE integration
Debug (Detailed)

• Special Debug Mode
  • Less intrusive, leverage existing pipeline
  • DPC, debug-interrupt, dret and ebreak

• Halt, Resume, (Single-)step
  • Only required command: Abstract read (read floating-point register, register and CSR)
  • Debug Transport Protocol (orthogonal)
    • Currently only JTAG specified

• SystemVerilog reference implementation available
  • https://github.com/pulp-platform/riscv-dbgs
Meet the Team: HW and SW Task Groups

- **Hardware TG**
  - Hugh Pollitt-Smith (CMC)
  - Tim Saxe (QuickLogic)

- **Software TG**
  - Jeremy Bennet (Embecosm)
  - Yunhai Shang (Alibaba T-Head)

OpenHW Director of Engineering: Florian Zaruba
Get on Board!

- Development is in the open!
- CORE-V MCU
  - [https://github.com/openhwgroup/core-v-mcu](https://github.com/openhwgroup/core-v-mcu)
- CORE-V APU
  - Directly in the core’s repository
  - [https://github.com/openhwgroup/cva6](https://github.com/openhwgroup/cva6)
- Thank you and be sure to visit the OpenHW booth here at the Virtual RISC-V Summit with demos from...