OpenPiton + Ariane :
The First Linux-Booting Open-Source RISC-V Manycore

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Princeton University, ETH Zurich

openpiton.org

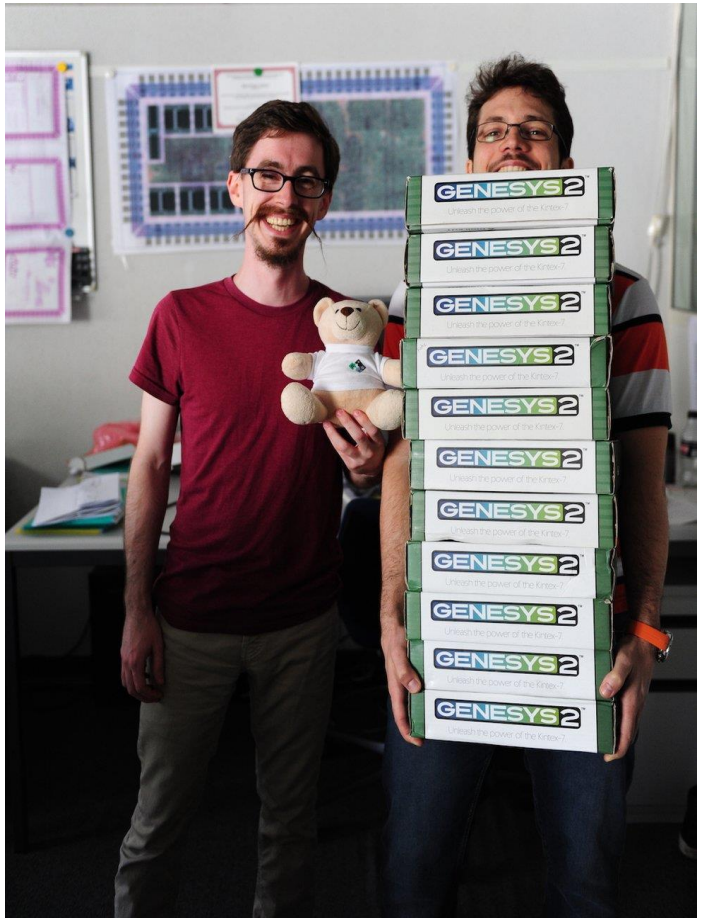
pulp-platform.org

PRINCETON UNIVERSITY

ETH zürich

Who are we?

- Jonathan Balkind
  - Lead architect of OpenPiton
- OpenPiton Team
  - Led by Prof. David Wentzlaff
  - Princeton Parallel Research Group
  - Open source HW since 2015
  - 13 PhD students
  - 1 Postdoc
  - N undergraduates



- Michael Schaffner
  - Responsible for OpenPiton+ Ariane integration
- PULP Team
  - Led by Prof. Luca Benini
  - ETHZ / Università di Bologna
  - Open source HW since 2013
  - Leaders in RISC-V development
  - Ariane dev: Florian Zaruba, Michael Schaffner and others

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Support

This material is based on research sponsored by the NSF under Grants No. CNS-1823222, CCF-1217553, CCF1453112, CCF-1823032, and CCF-1438980, AFOSR under Grant No. FA9550-14-1-0148, Air Force Research Laboratory (AFRL) and Defense Advanced Research Projects Agency (DARPA) under agreement No. FA8650-18-2-7846, FA8650-18-2-7852, and FA8650-18-2-7862 and DARPA under Grants No. N66001-14-1-4040 and HR0011-13-2-0005. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of Air Force Research Laboratory (AFRL) and Defense Advanced Research Projects Agency (DARPA), the NSF, AFOSR, or the U.S. Government.

Project Overview

- Collaboration between Princeton University and ETH Zurich
- Goal is to develop a permissively licensed, Linux capable manycore research platform based on RISC-V
  - Based on mature, extensible designs
  - Booted SMP Linux in <6 months
  - **The world's first open-source, Linux-booting, RISC-V manycore**
- Ariane
  - RV64GC Core (with extensions)
  - Linux capable
- OpenPiton
  - Manycore research platform
  - Distributed cache coherence and NoC

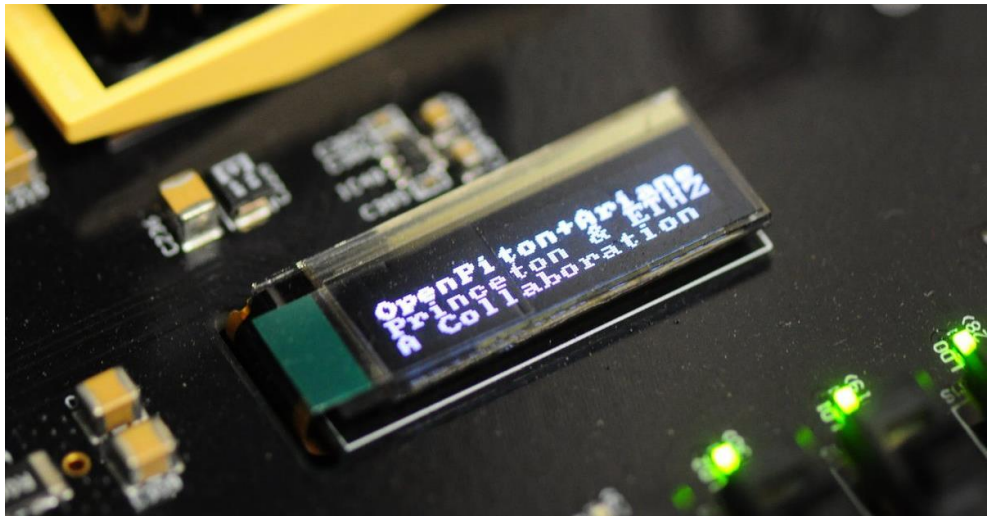
```
processor       : 0
hart            : 0
isa             : rv64imac
mmu             : sv39
uarch           : eth, ariane

processor       : 1
hart            : 1
isa             : rv64imac
mmu             : sv39
uarch           : eth, ariane

processor       : 2
hart            : 2
isa             : rv64imac
mmu             : sv39
uarch           : eth, ariane

processor       : 3
hart            : 3
isa             : rv64imac
mmu             : sv39
uarch           : eth, ariane

# cd /
```



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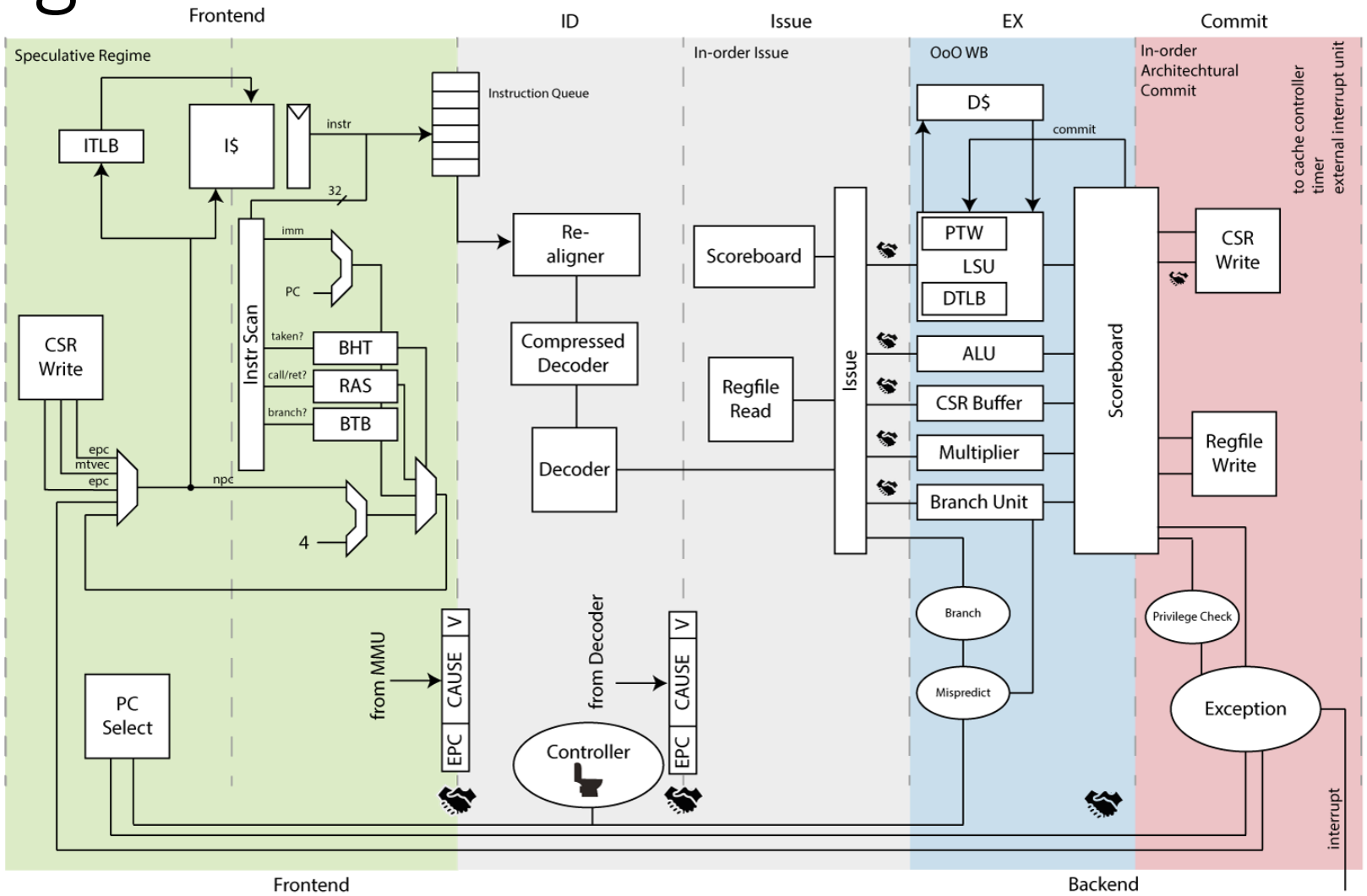
Ariane RV64GC Core

- Application class processor
  - Written in SystemVerilog
- Linux Capable
  - Tightly integrated D$ and I$
  - M, S and U privilege modes
  - TLB, SV39
  - Hardware PTW
- Optimized for performance
  - Frequency: 1.5 GHz (22 FDX)
  - Area: ~ 175 kGE
  - Critical path: ~ 25 logic levels
- 6-stage pipeline
  - In-order (single) issue
  - Out-of-order write-back
  - In-order commit
- Scoreboarding
- Designed for extensibility
- Branch-prediction
  - Return Address Stack (RAS)
  - Branch Target Buffer (BTB)
  - Branch History Table (BHT)

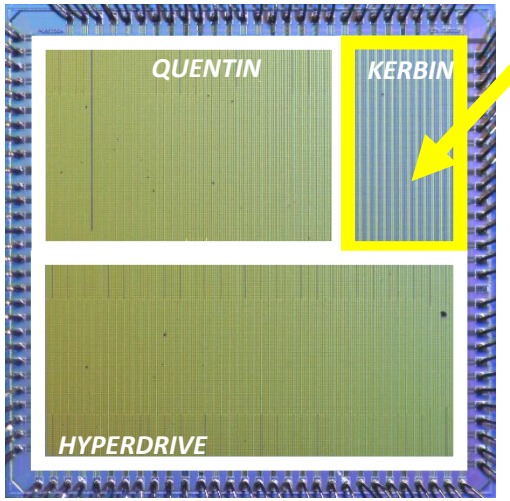
Peeking inside…



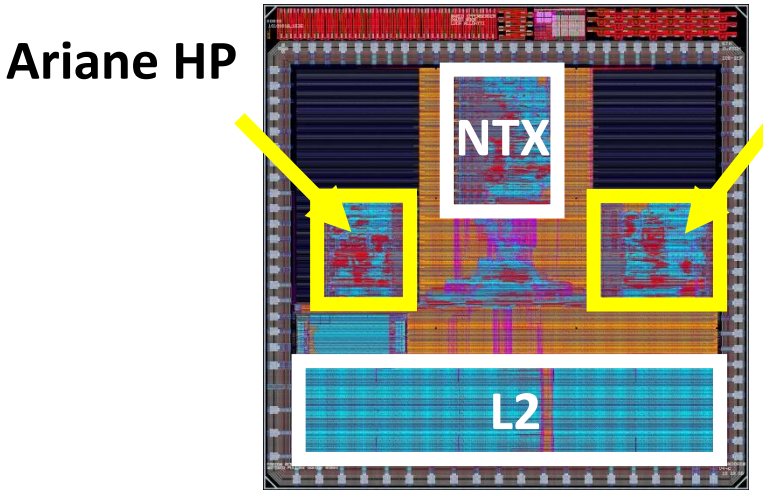
Silicon Proven Designs: Ariane

- **Ariane** taped-out in **GlobalFoundries 22nm FDX** twice
- 16kB instruction and 32kB data caches
- Poseidon:
  - Area: 0.23 mm^2 - 175 kGE
  - 0.2 - 1.7 GHz (0.5 V - 1.15 V)
- Kosmodrom:
  - RV64GCXsmallFloat, Transprecision / Vector FPU
  - **Ariane HP**
    - 8T library, 0.8V, 1.3 GHz
    - 55 mW @ 1 GHz
  - **Ariane LP**
    - 7.5T ULP library, 0.5V, 250 MHz
    - 5 mW @ 200 MHz

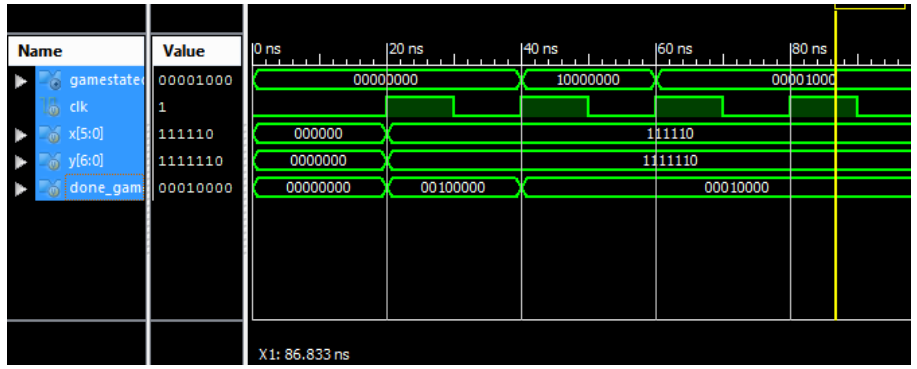
Poseidon layout



Kosmodrom layout

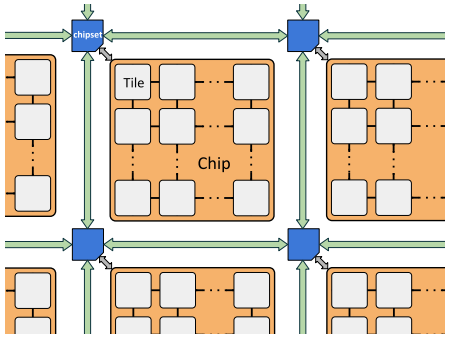


OpenPiton



- Open source manycore
- Written in Verilog RTL
- Scales to ½ billion cores
- Configurable core, uncore
- Simulation in VCS, ModelSim, Incisive, Verilator, Icarus
- Includes synthesis and back-end flow
- ASIC & FPGA verified
- ASIC power and energy fully characterized [HPCA 2018]
- Runs full stack multi-user Debian Linux
- Used for Architecture, Programming Language, Compilers, Operating Systems, Security, EDA research

debian



XILINX

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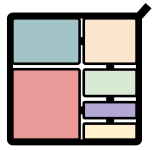
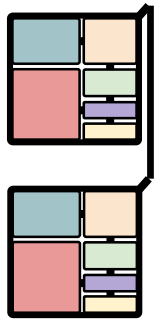
System Overview

Tile



System Overview



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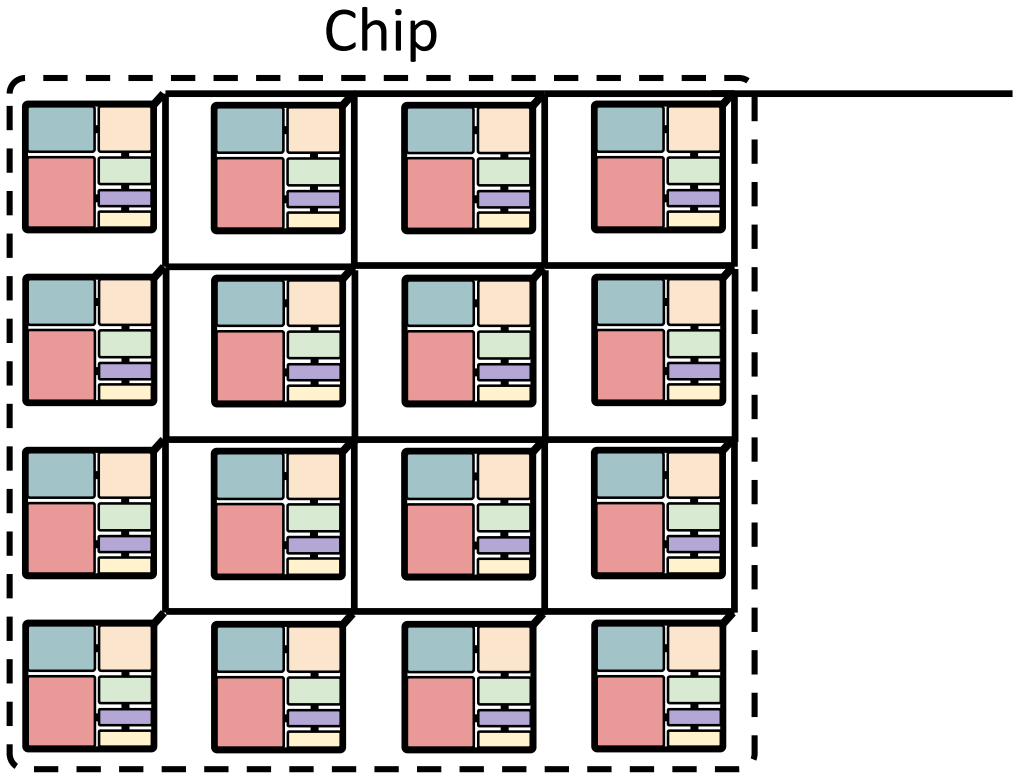

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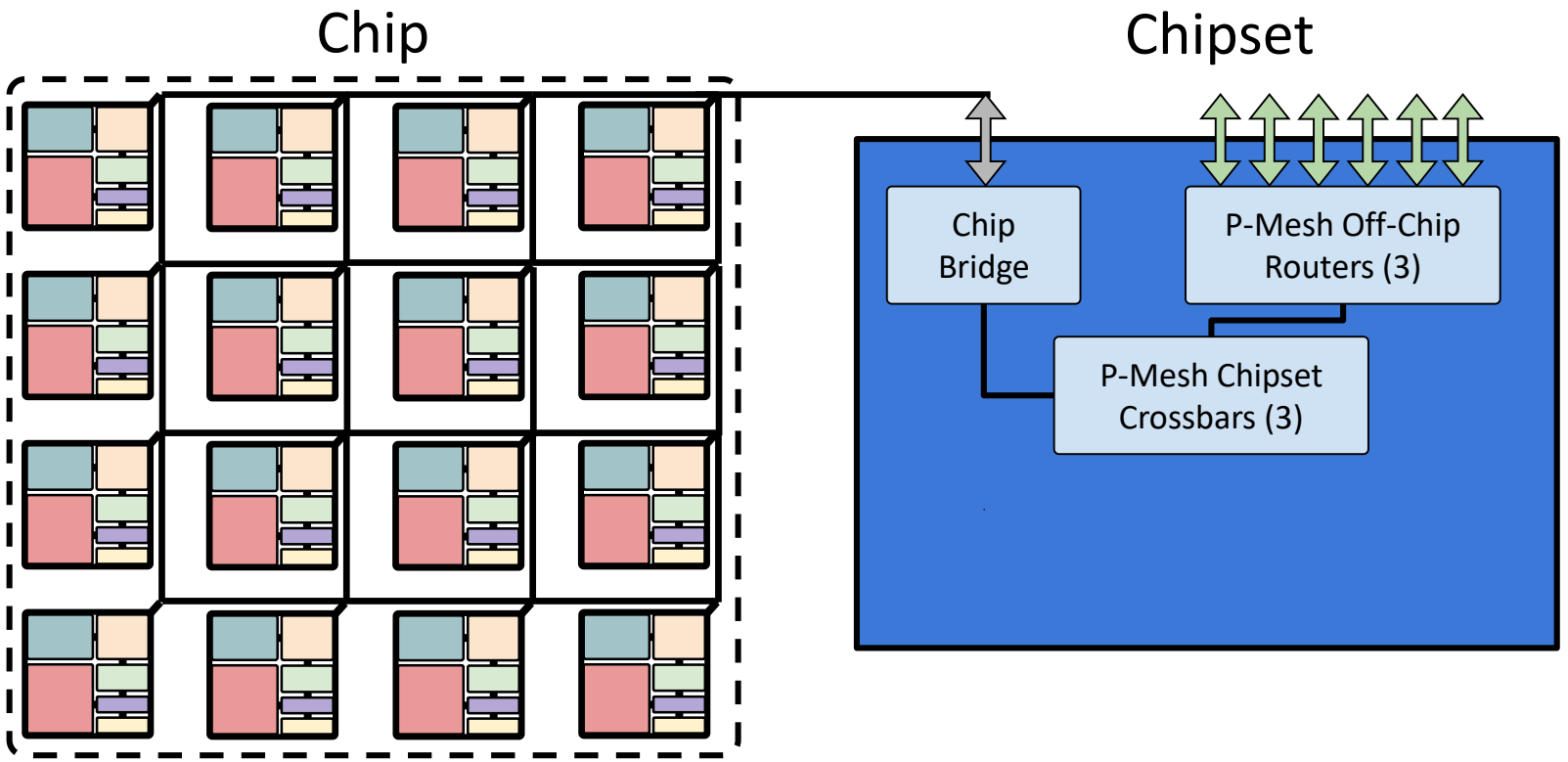
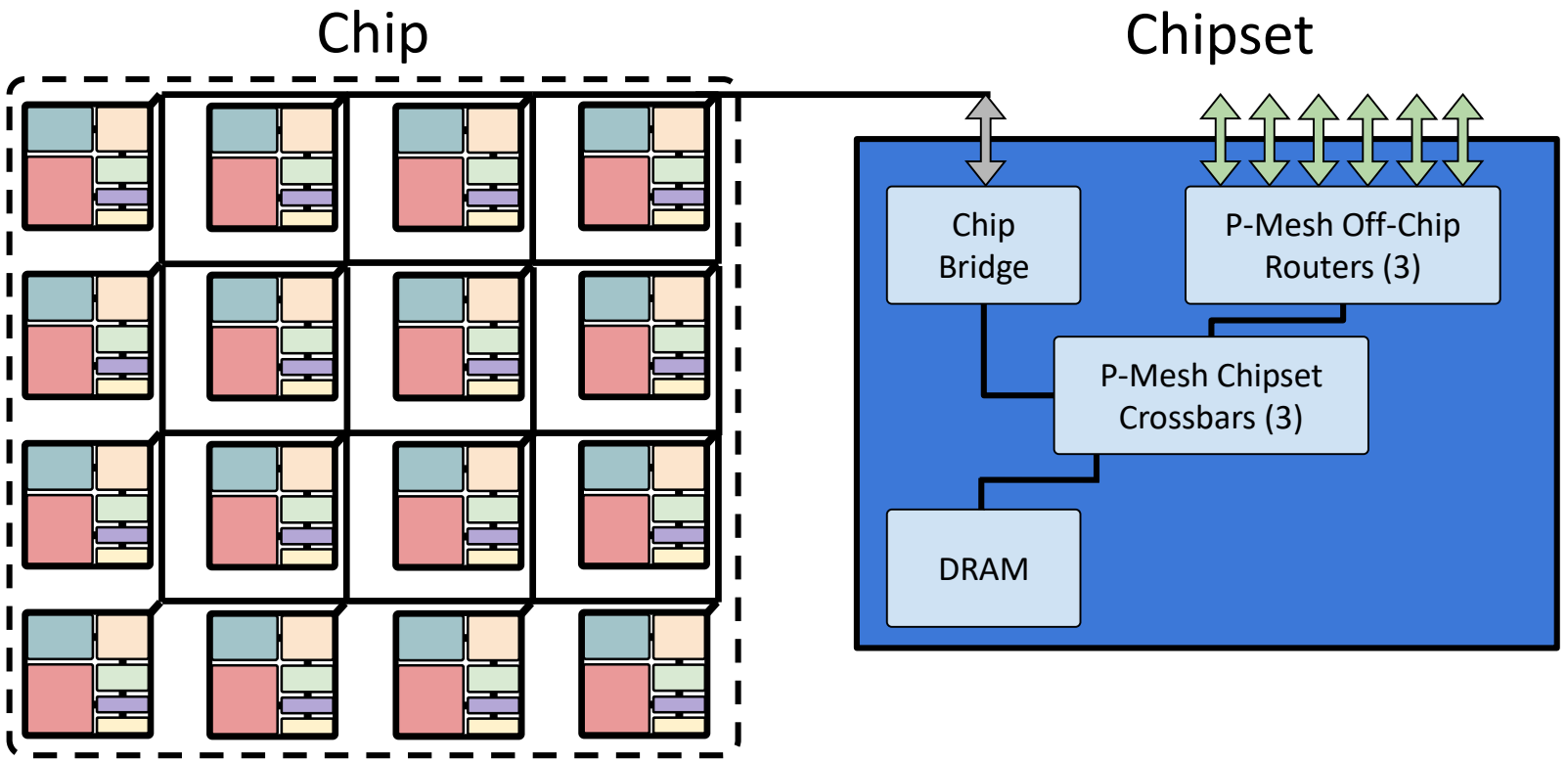


System Overview



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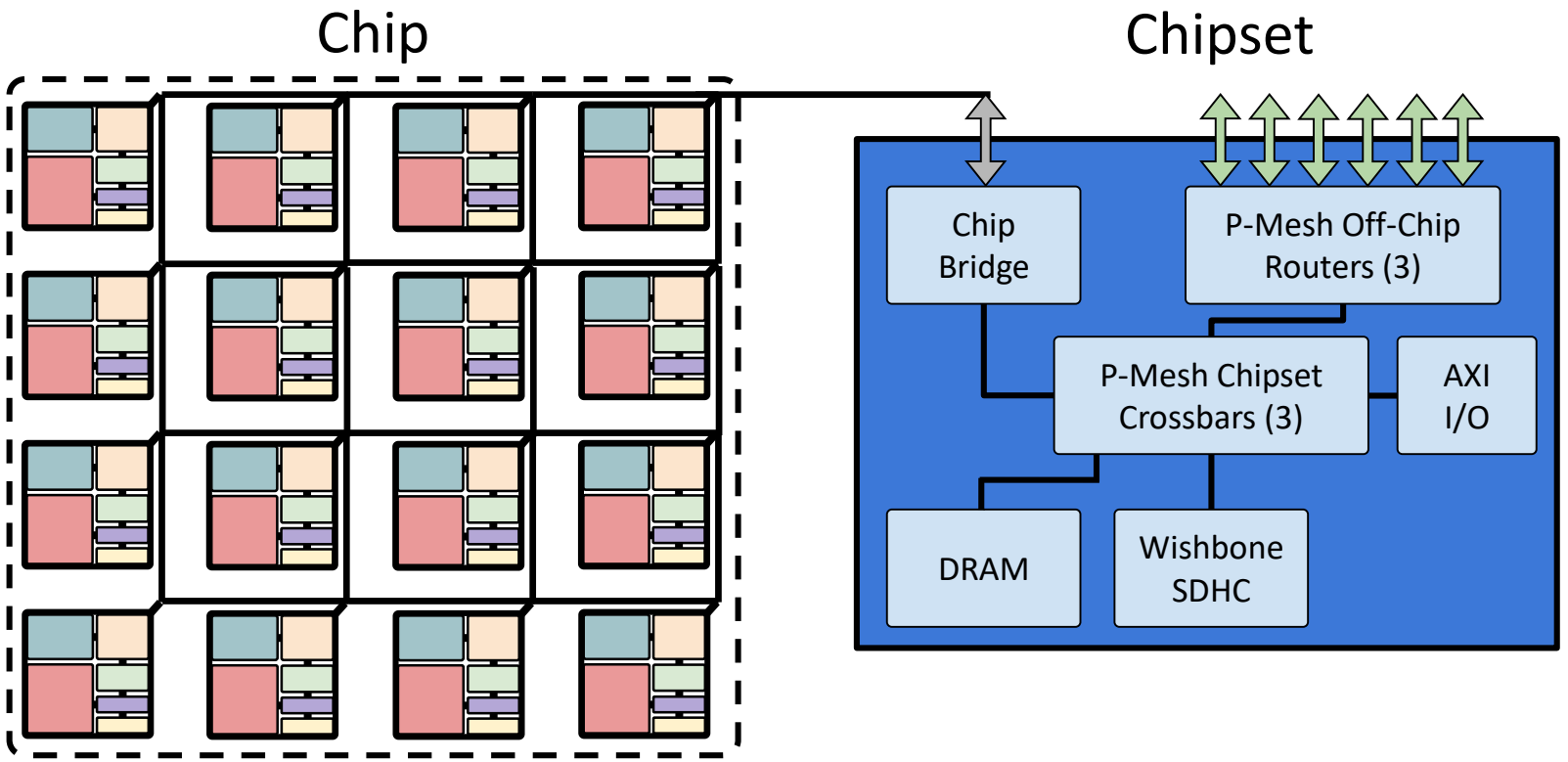
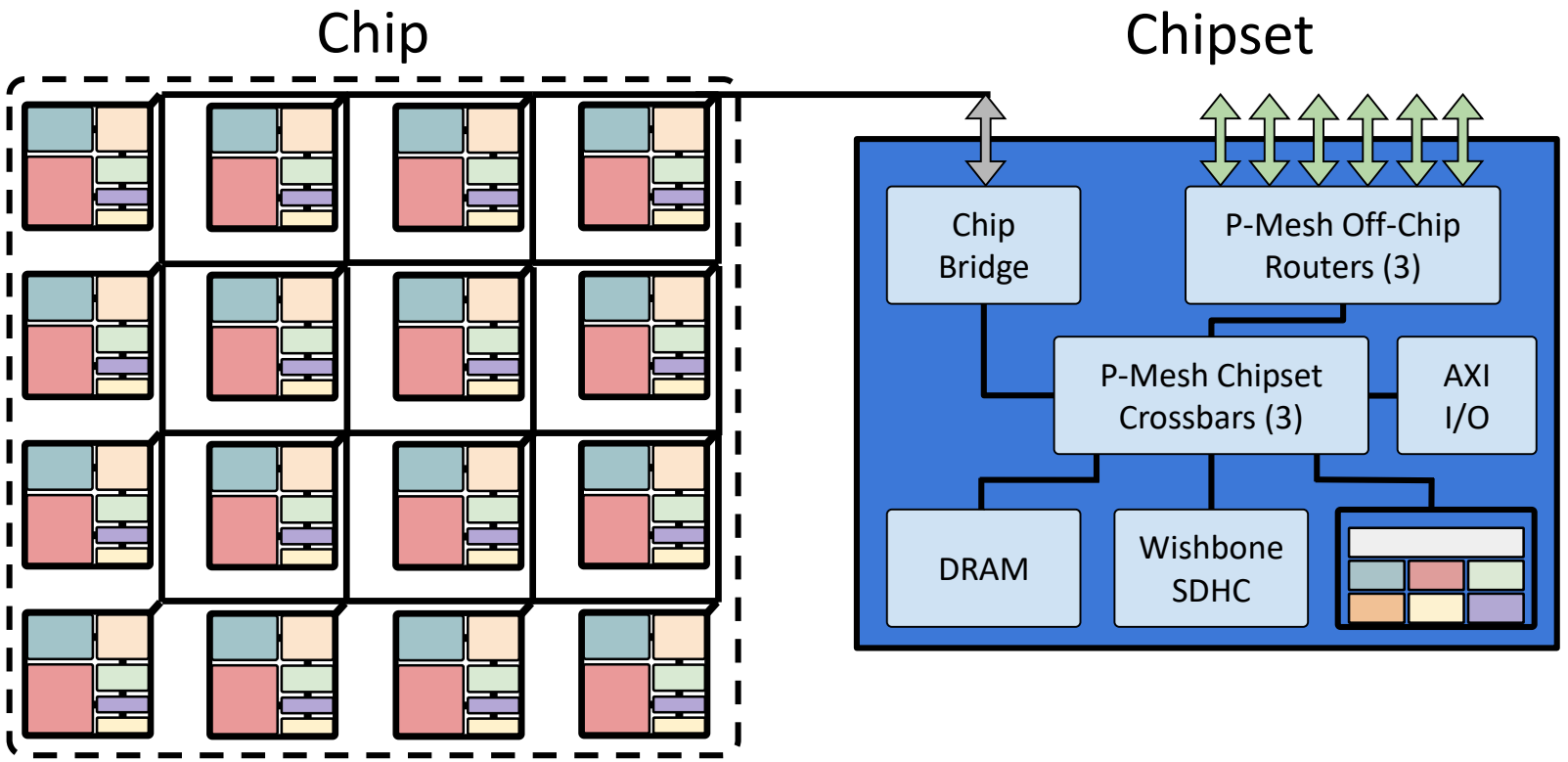
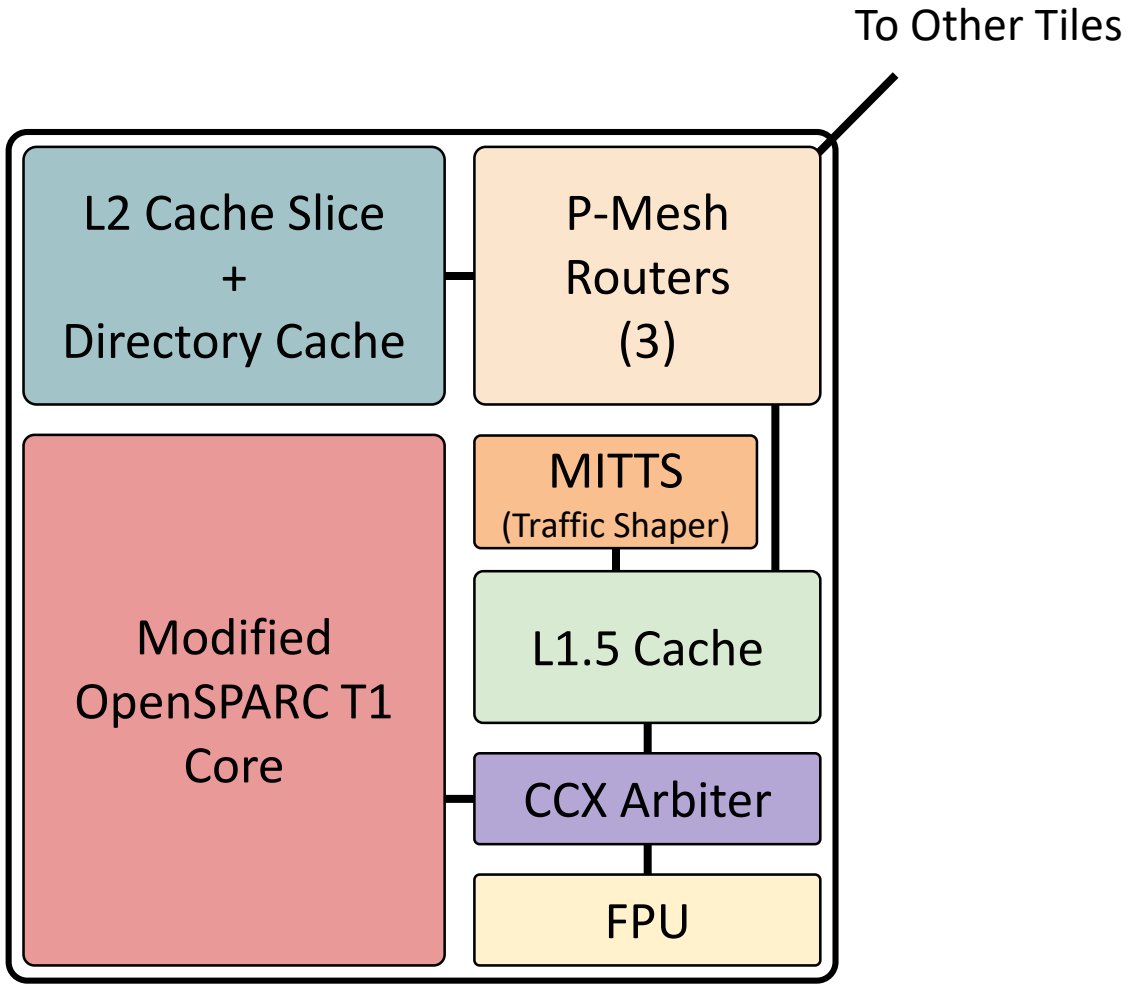


System Overview

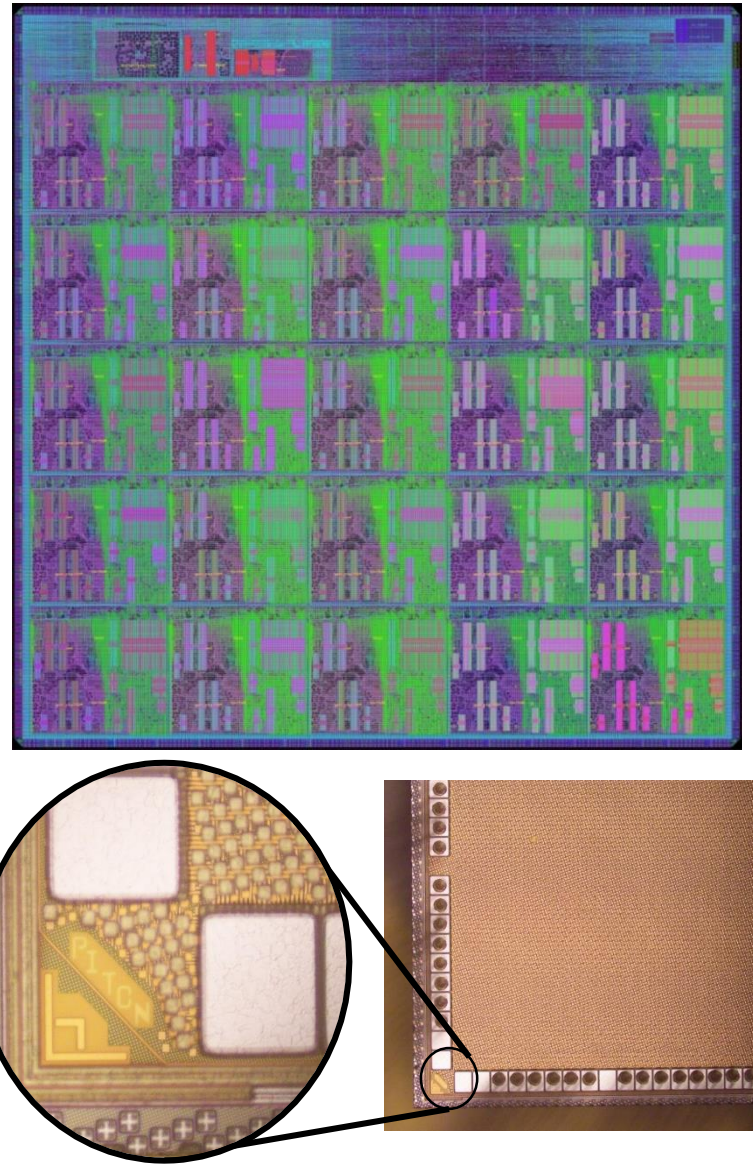


OpenPiton Tile

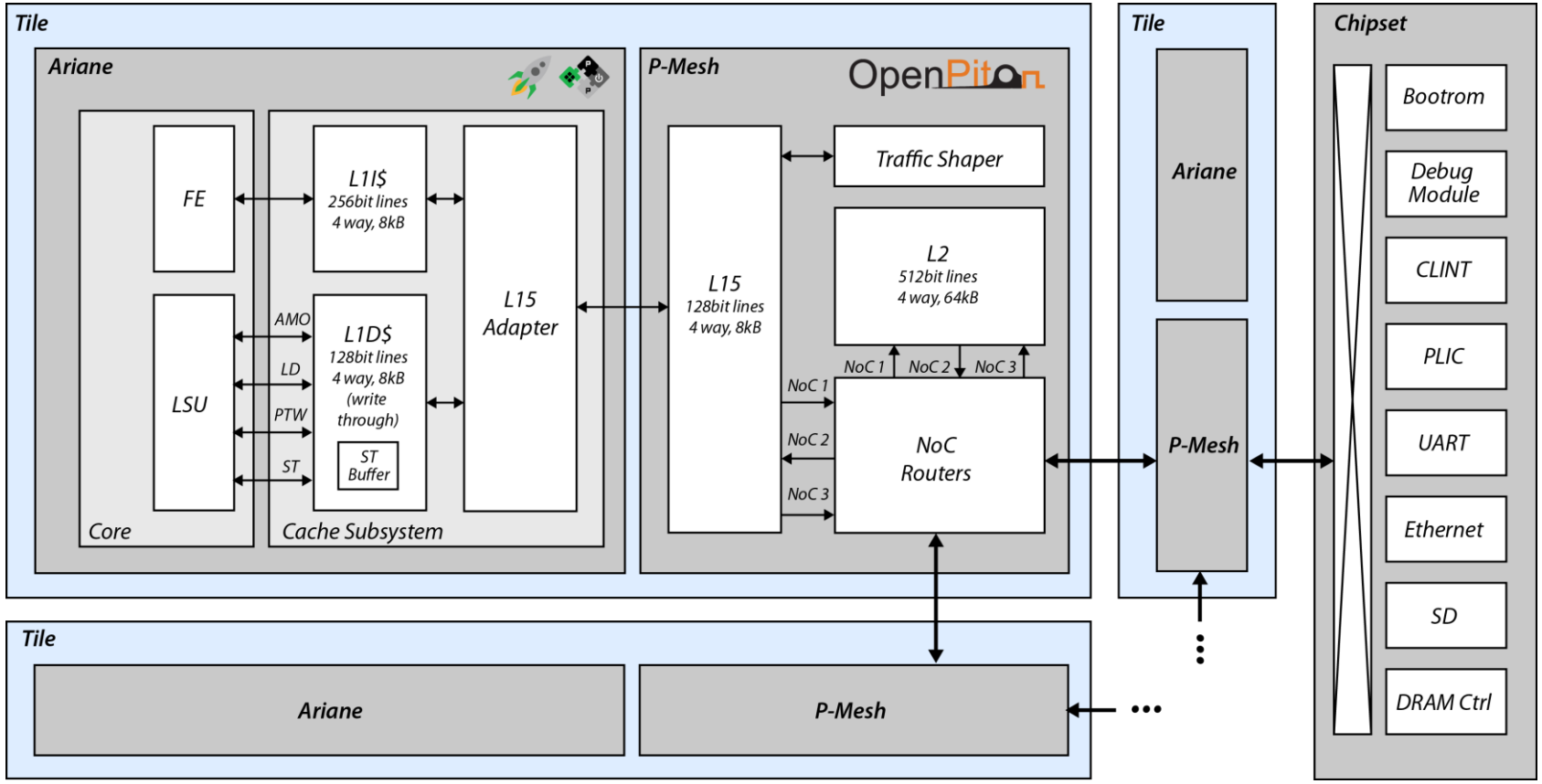


Silicon Proven Designs: Piton

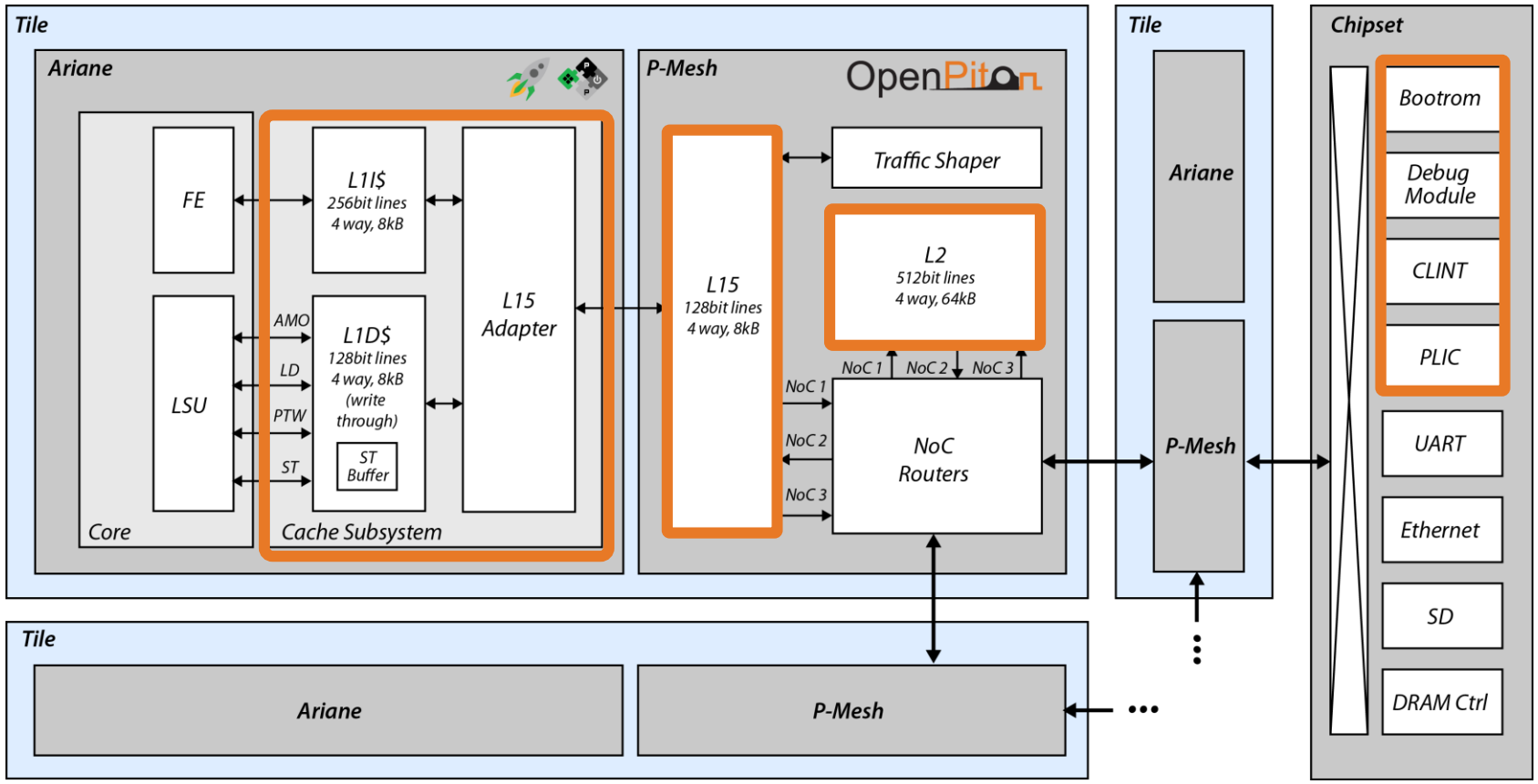
- 25-core
  - 2 Threads per core
  - Modified 64 bit OpenSPARC T1 Core
- 3 NoCs (P-Mesh)
  - 64 bit, 2D Mesh
  - Extend off-chip enabling multichip systems
- Directory-Based Cache System
  - 64kB L2 Cache per core (Shared)
  - 8kB L1.5 & L1 Data Caches
  - 16kB L1 Instruction Cache
- IBM 32nm SOI Process
  - 6mm x 6mm
  - 460 Million Transistors - Among largest chips built in academia
- Target: 1 GHz Clock @ 900 mV
- Received silicon and runs full-stack Debian in lab



OpenPiton+Ariane



OpenPiton+Ariane



- New write-through cache subsystem with invalidations and the TRI interface
- LR/SC in L1.5 cache
- Fetch-and-op in L2 cache
- RISC-V Debug
- RISC-V Peripherals

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Configurability Options

Component	Configurability Options	
Cores (per chip)	Up to 65,536	
Cores (per system)	Up to 500 million	
Core Type	OpenSPARC T1	**Ariane 64 bit RISC-V**
Threads per Core	1/2/4	**1**
Floating-Point Unit	FP64, FP32	**FP64, FP32**, FP16, FP8, BFLOAT16
TLBs	8/16/32/64 entries	Number of entries **(16 entries)**
L1 I-Cache	Number of Sets, Ways **(16kB, 4-way)**	
L1 D-Cache	Number of Sets, Ways **(8kB, 4-way)**	
L1.5 Cache	Number of Sets, Ways **(8kB, 4-way)**	
L2 Cache	Number of Sets, Ways **(64kB, 4-way)**	
Intra-chip Topologies	**2D Mesh**, Crossbar	
Inter-chip Topologies	2D Mesh, 3D Mesh, Crossbar, Butterfly Network	
Bootloading	SD/SDHC Card, UART, RISC-V JTAG Debug	

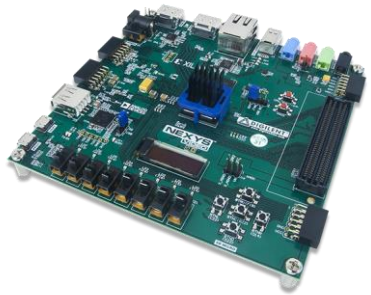
FPGA Prototyping Platforms

Available:

- Digilent Genesys2
  - $999 ($600 academic)
  - 1-2 cores at 66MHz
- Xilinx VC707
  - $3500
  - 1-4 cores at 60MHz
- Digilent Nexys Video
  - $500 ($250 academic)
  - 1 core at 30MHz

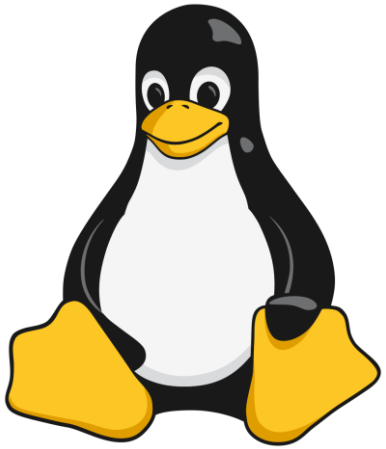
In progress:

- Xilinx VCU118, BittWare XUPP3R
  - $7000-8000
  - >100MHz
- Amazon AWS F1
  - Rent by the hour



Boot SMP Linux Today!

- Clone from:
  - https://github.com/PrincetonUniversity/openpiton
  - Simulation with Modelsim, VCS, Verilator
- Prebuilt bitfiles and Linux image available
  - Play Tetris, browse the web!



- Roadmap:
  - OpenSBI, U-Boot (?), Debian/Fedora distro
  - Simulation extensions (RV Torture, litmus, etc)
  - Performance enhancements (TLBs, mem. IF, multi-issue)
  - Tapeouts!

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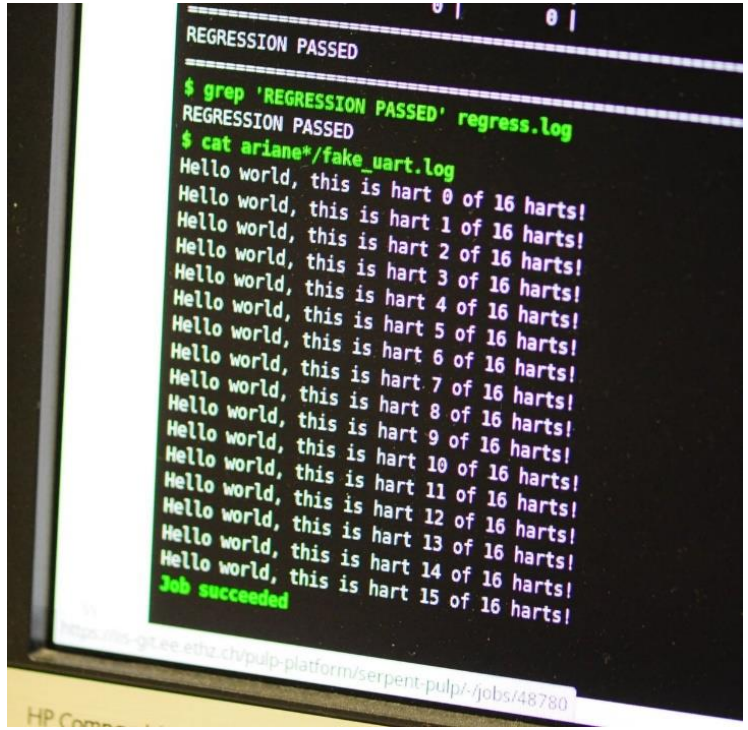
Upcoming Events / Papers

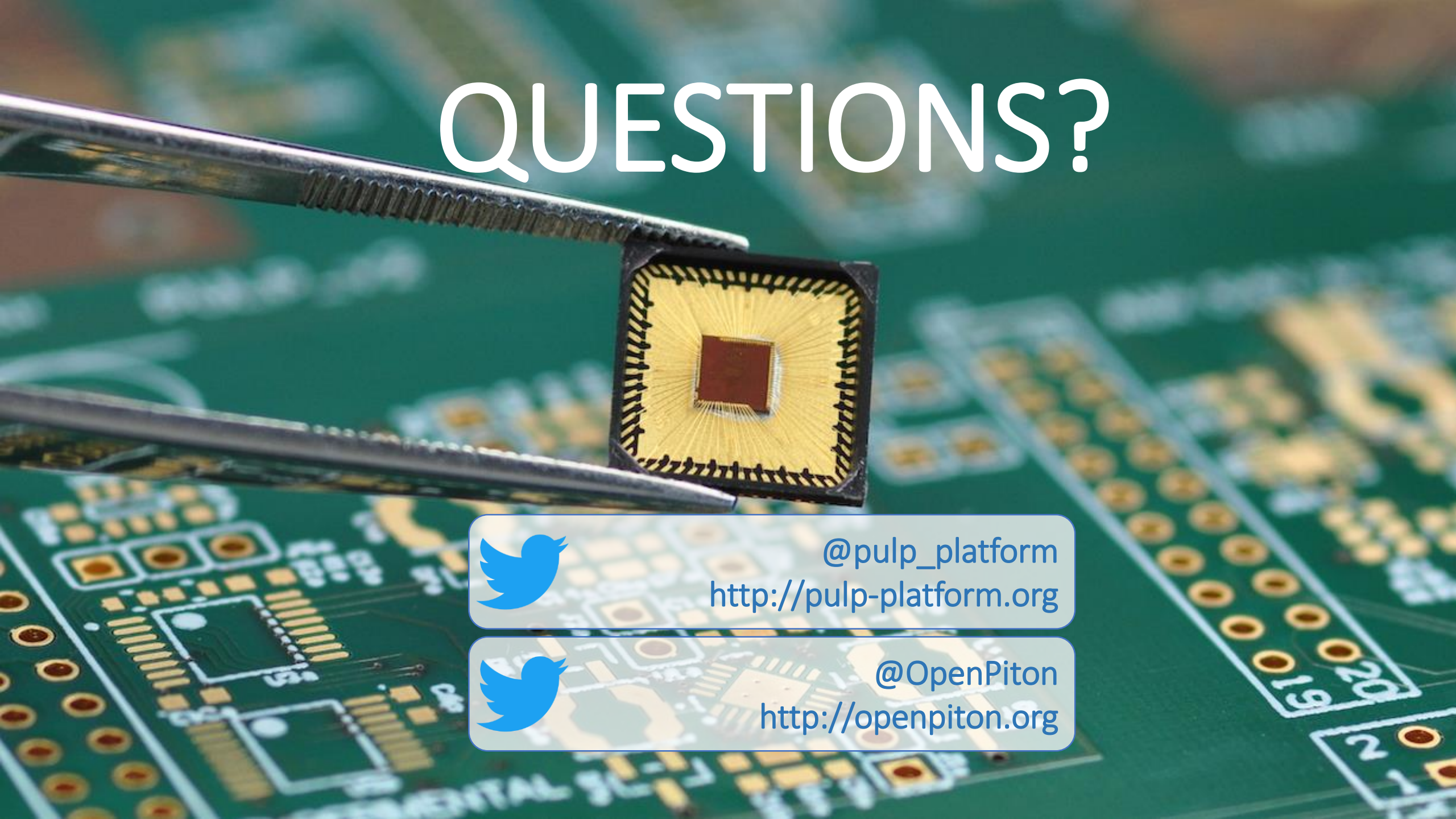
- Hands-on workshop @WOSH this Thursday afternoon (13:30 – 18:00, ETZ D61.1)
  http://openpiton.org/WOSH19_tutorial.html

- Hands-on workshop @ISCA on Sunday afternoon (June 23 14:00, Phoenix, Arizona, USA)
  http://openpiton.org/ISCA19_tutorial.html

- Talk @CARRV on Saturday morning (June 22 09:00, Phoenix, Arizona, USA)
  Paper with more details: https://carrv.github.io



QUESTIONS?



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Board Name / FPGA Type	Clock [MHz]	Config X × Y	Core Type	FPU [y/n]	LUTs [k]	Registers [k]	RAM Tiles [#]	DSPs [#]
Digilent NexysVideo Artix 7 7a200tsbg484	30	1 × 1	Ariane	no	95 (71%)	72 (27%)	66 (18%)	16 (2%)
	30	1 × 1	Ariane	yes	110 (82%)	75 (28%)	66 (18%)	27 (4%)
	30	1 × 1	OpenSPARC T1	yes	115 (86%)	96 (36%)	59 (16%)	13 (2%)
Digilent Genesys2 Kintex 7 7k325tffg900-2	67	1 × 1	Ariane	no	86 (42%)	72 (17%)	66 (15%)	16 (2%)
	67	1 × 1	Ariane	yes	99 (49%)	75 (18%)	66 (15%)	27 (3%)
	67	1 × 1	OpenSPARC T1	yes	105 (52%)	91 (22%)	59 (13%)	16 (2%)
	67	2 × 1	Ariane	no	141 (69%)	113 (28%)	124 (28%)	16 (4%)
	67	2 × 1	Ariane	yes	167 (82%)	120 (30%)	124 (28%)	54 (6%)
	67	2 × 1	OpenSPARC T1†	yes	160 (79%)	137 (33%)	112 (25%)	32 (4%)
Xilinx VC707 Virtex 7 7vx485tffg1761-2	60	1 × 1	Ariane	no	99 (33%)	73 (12%)	63 (6%)	16 (<1%)
	60	1 × 1	Ariane	yes	114 (37%)	77 (13%)	63 (6%)	27 (1%)
	60	1 × 1	OpenSPARC T1	yes	119 (39%)	97 (16%)	53 (5%)	16 (<1%)
	60	2 × 2	Ariane	no	284.1 (94%)	202 (33%)	237 (23%)	64 (2%)
	60	3 × 1	Ariane	yes	268 (88%)	169 (28%)	179 (17%)	81 (3%)
	60	3 × 1	OpenSPARC T1†	yes	255 (84%)	208 (34%)	158 (15%)	48 (2%)
Xilinx VCU118 Virtex US+ xcvu9pflga2104-2L	100	1 × 1	Ariane	no	90 (8%)	81 (3%)	88 (4%)	19 (<1%)
	100	1 × 1	Ariane	yes	103 (9%)	84 (4%)	89 (4%)	30 (<1%)
	100	1 × 1	OpenSPARC T1	yes	108 (9%)	100 (4%)	79 (4%)	19 (<1%)
	100	4 × 4	Ariane	no	923 (78%)	704 (30%)	963 (45%)	259 (4%)
	100	4 × 2	Ariane	yes	583 (49%)	399 (17%)	495 (23%)	219 (3%)

† Without Coherence Domain Restriction [8] in caches.