How to tape-out a 64-core RISC-V SoC in under 60 days

Left empty for blind review

[1]First affiliation
[2]Second affiliation

Abstract

Open-source hardware has been instrumental in allowing the necessary experience and components that are needed for a complex System-on-Chip to be shared freely, greatly enhancing the productivity. As a concrete demonstration, in the PROJECT[1], a team of four Ph.D. students were able to take over a many-core design from open-source repositories, scale it out to 64 RISC-V cores, map it to a state-of-the-art FinFET technology in 12nm, fix issues, enhance capabilities and successfully submit the design to tape-out in 56 days from the day the idea was first brought up.

Introduction

An often-overlooked side effect of Moore's Law has been the design effort required to keep up with the increased integration density it provides. What used to be a complete integrated circuit (IC) only a decade ago, is today a smaller part of a System-on-Chip (SoC), yet the timeline for completing such a design is expected to remain the same. Part of this productivity increase is achieved through improvements in electronic design automation (EDA) tools, and a larger part is achieved by design re-use of trusted and verified components commonly referred to as intellectual property (IP) blocks in IC design.

For a long time, these IP blocks were proprietary and were either developed and maintained by internal design teams in large corporations, or were made commercially available through IP vendors. The same observation above also holds true for the IP blocks. IP that a decade ago was an important part of a design, is now a smaller part of a larger SoC and an ever-increasing number of such IP is needed to complete a relevant design. This has been an issue for academic and research community limiting their ability to demonstrate their research in industry relevant SoCs.

The recent success of open-source hardware has been a very welcome development and has closed the productivity gap for research institutions that did not have access to commercial IPs allowing them to continue their research activity on industry relevant complex SoC designs. In this paper, we highlight the timeline of a recent, fairly complex SoC design that our group was able to complete in less than 60 days from the date the first discussion started until its successful tape-out in a 12nm FinFET technology.

Background

The focus of our research group is the development of energy efficient computing architectures. We have followed the work done around the Mempool [1] architecture that is able to scale up to 256 RISC-V cores. The authors of Mempool have made the RTL code, testbenches and verification setup available on GitHub [2] allowing us to understand their work and contributions, and make our own experiments.

As part of a semester thesis within our group, a customized version of the Mempool architecture codenamed PROJECT was developed to add floating point support and introduce the capability to support systolic operations. Supervised by two Ph.D. students, a student enrolled in the Master's program worked on the design from September to December 2023. Part of the work also included surrounding the Mempool core by a set of peripherals (UART, GPIOs, clocking) that would allow it to be used independently, and could boot on its own. These components were taken from open-source repositories and were added to the system.

For the physical implementation, a mature 65nm process was chosen, and the student scaled the design to a total of 16 RISC-V cores organized in four groups to stay within a $10mm^2$ area budget imposed by funding restrictions. The design managed a respectable 180MHz clock frequency in post layout timing analyses using typical conditions. Towards the completion of the project, discussions started whether or not it would be possible to make an actual tape-out with the present design.

At this point, late December 2023, an opportunity presented itself through the University Partnership Program of Globalfoundries which were looking for design ideas that Globalfoundries would sponsor a $5mm^2$ die on its 12nm FinFET technology. The problem: the final design delivery for this IC would be the 14th of February which was less than 60 days away.

Timeline of PROJECT

In the following, we have re-created the timeline of the project with critical junctures and decisions, starting from the first day where the possibility to take part in the Globalfoundries sponsored run was considered, December 20th 2023, shortly before the holiday season. At this time, the

[1] Generic name used for blind review purposes

PROJECT was mapped to a mature 65nm technology, and still work was needed to for additional verification, fixes to the codebase to alleviate these issues, as well as completing the back-end flow for an actual tape-out.

December 20th (D-56 days): The team responsible for the supervision of PROJET is made aware of the possibility that we could move to GF12 and target a mid-February tape-out. Discussions start if it would be possible to finalize the design on time.

December 21st (D-55 days): The PROJECT team is assembled consisting of four Ph.D. students, two original supervisors, plus two additional Ph.D. students with experience in back-end design. Preparations for the design start.

January 3rd (D-42 days): The application to Globalfoundries University Program was submitted requesting the donation.

January 4th (D-41 days): The kick-off meeting for PROJECT was held, and the responsibilities in the team were discussed. As a new technology was being used questions about the design flow to be used were raised to the support team in charge of maintenance of the design flows.

January 8th (D-37 days): Confirmation that our PROJECT would receive sponsoring from Globalfoundries.

January 11th (D-34 days): Discussions start on parametrization of the project. Initial trials suggest that the available area would support a larger design. Exploration for different options (16, 32 or 64 cores) start.

January 20th (D-25 days): The complete design flow in GF12 is prepared and validated for the PROJECT. The 16-core version is able to close timing at 750MHz. The entire design flow takes around 3 days to complete, multiple versions are being evaluated in parallel.

January 29th (D-16 days): A dry-run version is submitted through Europractice IC service to Globalfoundries. This is a 32-core version running at 615MHz and still has some design rule violations.

February 4th (D-10 days): Layout vs Schematic (LVS) checks pass completing the final part of the complete design flow. Attention now turns into finalizing the design and parametrization, considering that the runtime for the design is between 3-5 days.

January 9th (D-5 days): Three candidates with different parametrization (32, 64 and 64 cores) have been presented. Team discusses to concentrate efforts on an ambitious parametrization, while keeping a simpler backup ready.

January 14th (D Day) Successful tape-out achieved with no issues reported due to any DRC errors, design accepted for fabrication.

Results

The resulting layout of the PROJECT can be seen in Figure 1. The final design has 64 RISC-V cores with FPUs that support 32- ,16- and 8-bit floating point numbers, configurations to support systolic operation and achieves a maximum clock frequency 720MHz in worst case conditions (WC, 0.72V, 125C°), and over 900MHz in typical conditions where it consumes 64mW.

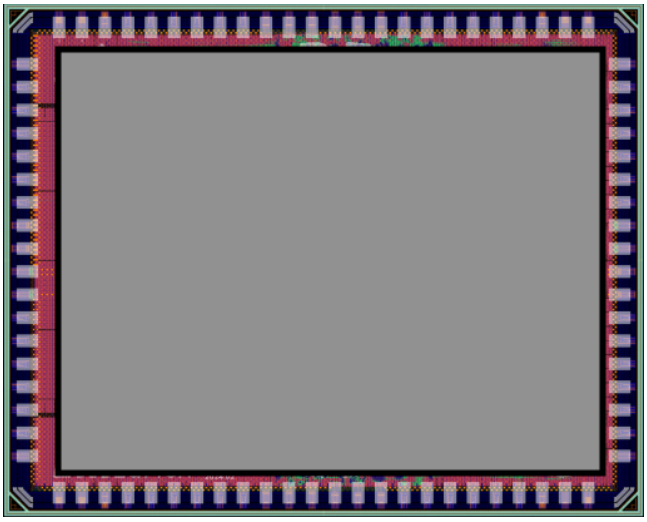

Figure 1 - Layout of PROJECT as submitted

Conclusion

The successful completion of PROJECT in less than 60 days is a vivid demonstrator of how much current open-source IP can help with the design of complex SoCs. Part of the rapid design cycle is undoubtedly also the experience of the designers working on the SoC. In our case, the availability of high-quality open-source IP also allows designers to get more experience in a shorter amount of time, which we believe is one of the most important hidden benefits that come through the wider adoption of open-source hardware.

In about a decade, open-source hardware has made significant progress and we believe that both the quantity and quality of available IP will continue to increase becoming an important part of SoC design both in academia and industry.

We strongly believe that the availability of open-source EDA tools coupled with open-source Process Design Kits (PDK) will close the ‘last-mile’ of the IC design cycle, bringing a similar productivity increase and more importantly will support the development of skilled workforce urgently needed to sustain the development of relevant SoC designs in industry and academia.

References

[1] S. Riedel et al., “MemPool: A Scalable Manycore Architecture with a Low-Latency Shared L1 Memory”, IEEE Tran. Computers, vol 72, no 12, pp 3561- 3575, 2023, doi: 10.1109/TC.2023.3307796

[2] Mempool online repository, https://github.com/pulp-platform/mempool, retrieved on March 2024