How to tape-out a 64-core RISC-V SoC in under 60 days

Frank K. Gürkaynak and the team ETH zürich

December 20th — 56 days to go
December 21st — 55 days to go
January 3rd — 42 days to go
January 4th — 41 days to go
January 8th — 37 days to go
January 11th — 34 days to go
January 20th — 25 days to go
January 29th — 16 days to go
February 4th — 10 days to go
February 9th — 5 days to go
February 14th — 0 days to go

Design

GlobalFoundries™ University Partnership Program

Team Setup

16 cores - TSMC65 - 200MHz

Heartstream
GF12nm
64 RISC-V cores
900MHz

Kick-off

Sponsorship

RTL

16 – 32 - 64 cores?

Synthesis

Floorplan

Design Flow

Placement and Routing

Dry-run

32 Core – 615 MHz

DRC clean

DRC LVS

Final Designs

32 – 64[a] - 64[b] cores?

Tape-out

64 cores – 900 MHz

SoA Research

https://pulp-platform.org/publications.html

Systolic | MemPool | Multi precision

Keys to our Success !!!

Silicon Proven IP

http://asic.ethz.ch

Occamy | Minpool

Open Source Releases

https://github.com/pulp-platform

Snitch | Serial Link | newFPU | AXI | RISC-V Debug | iDMA

About Heartstream

Heartstream is a 64-core RISC-V based building block for our **MemPool** and TeraPool based shared-memory architectures that can efficiently scale up to 256/1024 cores. Heartstream adds two important features to **MemPool**:

1. FPU with SIMD capability
2. Systolic Computation extension

Read more on **MemPool**:

S. Riedel, M. Cavalcante, R. Andri and L. Benini, "MemPool: A Scalable Manycore Architecture With a Low-Latency Shared L1 Memory," IEEE Transactions on Computers, vol. 72, no. 12, pp. 3561-3575, 2023, DOI: 10.1109/TC.2023.3307796

Watch this space, new publications coming soon

The Heartstream Team
Yichao, Samuel, Marco and Sergio

Visit our chip gallery

Useful Links

Our WWW page

Bianca the Bear

10 YEARS OF PULP +1 PULP

https://pulp-platform.org/
https://twitter.com/pulp_platform
https://github.com/pulp-platform