RISC-V Silicon at Scale in Academia: Designing "BIG" Open-Source Chips on PULP

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70 +	down to **7nm**	up to **432**	**1 Billion +**	**2.5D**
Chip Tapeouts	Advanced Node	RISC-V Cores	Transistors	Chiplet + HBM2E

PULP 14 Years

Parallel Ultra Low Power

The PULP Platform is an open-source ecosystem for energy-efficient RISC-V architecture research, developed by ETH Zürich and the Uni. Bologna.

- Reusable RISC-V IP cores & interconnects
- Scalable many-core clusters (Snitch RV32)
- SoC templates for rapid design bring-up
- 70+ tapeouts across 65 nm to 7 nm

pulp-platform.org GitHub

PULP Platform RISC-V Open-Source Ecosystem Stack

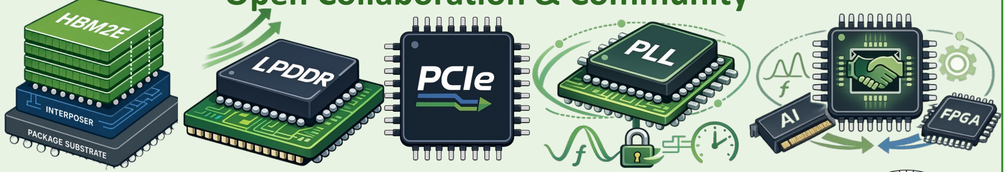
- Applications & Research
- Open Software Stack
- RISC-V ISA
- PULP IP Library (cores, interconnects, peripherals… …)

RISC-V Cores and Vector Units					
RI5CY CV32E	Zero R Ibex	Snitch	Spatz	Ariane CVA6	ARA
RV32	RV32	RV32	RVV	RV64	RVV

Peripherals	
JTAG	SPI
UART	I2S
DMA	GPIO

Interconnects	
LIC	HCI
APB	FlooNoC
AXI4	

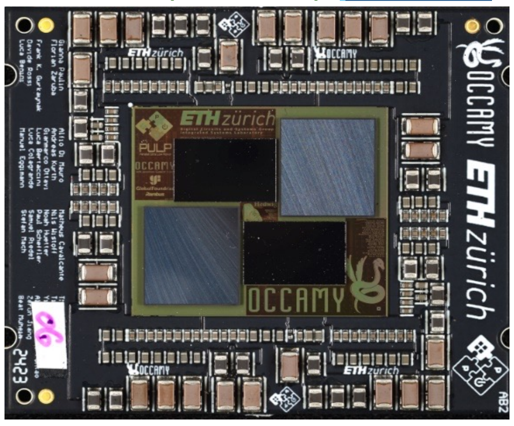
Open Collaboration & Community



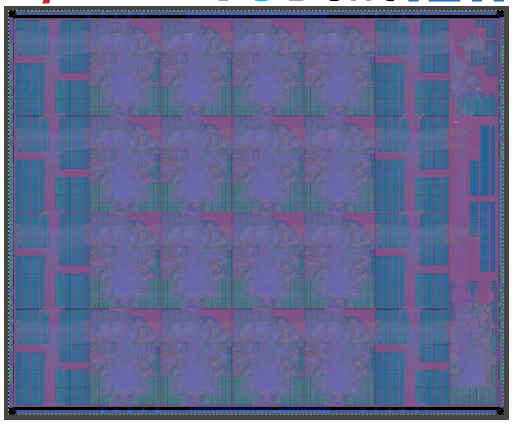
Rambus · SYNOPSYS · AVERY design systems · tsmc · intel · GlobalFoundries · Micron

Big PULP Chips

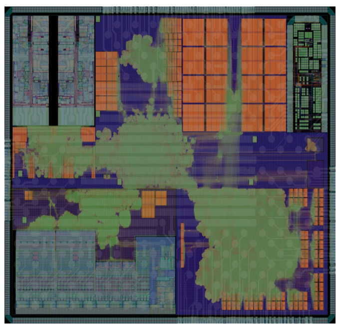
University Partners: (and more ...) KU LEUVEN · TU/e Eindhoven University of Technology · TU Delft · TUM



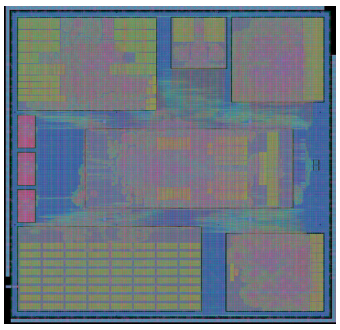
Occamy — 12 nm • 2.5D-IC • 432 cores
Dual-chiplet RISC-V + HBM2E, 768 DP-GFLOP/s



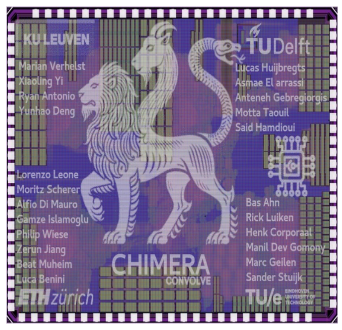
Picobello — 7 nm • 144 cores
NoC-based AI accelerator with tensor units



Flamingo — 22 nm • 9 cores
Robotics edge-AI, PCIe + LPDDR4



CARfield — 16 nm • 17 cores
Time-predictable automotive SoC



Chimera — 22 nm • 17 cores
Edge-AI with CIM acceleration

Chip	Node	Key Idea	# Cores	Team FTEs	Design Months
Occamy	12 nm	2.5D Chiplet HPC	432	25	15
Picobello	7 nm	Tensor + NoC AI Accel.	144	12	6
Flamingo	22 nm	Robotics Edge-AI	9	16	16
CARfield	16 nm	Automotive SoC	17	20	8
Chimera	22 nm	CIM AI Accelerator	17	4	3

Make Billion-Transistor Designs Possible for Academic Institutions

Design Reuse
- Open-source HW/SW ecosystem
- 3rd party IPs (HBM, PCIe, LPDDR4)
- Verification at scale
- Vendor support

Team Formation
- 20+ contributors per chip
- Student turnover & PhD timelines
- Cross-institution coordination
- Expertise alignment

Technology Access
- Advanced nodes are expensive
- Restricted NDA-based access
- EDA & IP dependence
- Funding from EU/Chips-JU

Assembly & Packaging
- MPW for advanced packaging
- Prototype-quantity challenges
- 2.5D/flip-chip difficulty
- Volume-business mismatch

Open Hardware Ecosystem: More Agility, More Collaboration, More Openness for More Design Complexity

References
[1] P. Scheffler et al., "Occamy: A 432-Core Dual-Chiplet Dual-HBM2E 768-DP-GFLOP/s RISC-V System," JSSC, 2025.
[2] A. Garofalo et al., "A Reliable, Time-Predictable Heterogeneous SoC for AI-Enhanced Mixed-Criticality Edge Applications," TCAS-II, 2025.
[3] F. Conti et al., "Open Source Heterogeneous SoCs for AI: The PULP Platform Experience," IEEE SSC Magazine, 2025.

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