Who Checks the Checker?

End-to-End Architectural SEU Tolerance for RISC-V Microcontroller Protection

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Motivation

- **Radiation-induced SEUs** corrupt data and computation **in space SoCs**, risking **mission failure**.
- Rad-Hard tech is costly and lags modern nodes.
- **New Space** demands modern, cost-effective, fault-tolerant SoCs on advanced nodes.
- Goal: comprehensive **soft-error tolerance** in RISC-V SoCs via **architectural** methods.

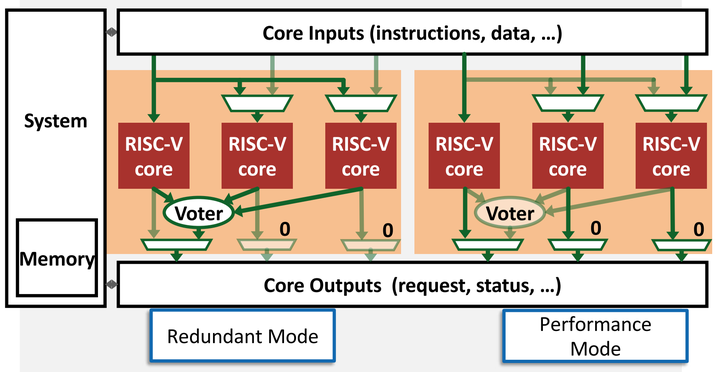
SotA Gaps

- Commercial space processors rely on **outdated and Rad-Hard** nodes, losing out on performance, efficiency, and capabilities.
- Standard lockstep permanently dedicates all cores to redundancy, **sacrificing performance** when fault tolerance is not needed.
- Other architectural schemes (e.g., fine-grained TMR) are expensive.
- **Voters** and **checkers** are often left **unprotected** or **requiring rad-hard** cells.

Building Blocks

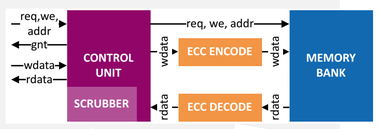
Processor Cores

- Hybrid Modular Redundancy
  - Runtime-switchable
  - Dual- & Triple-core Lockstep (DCLS/TCLS)
- Tested in a RISC-V multi-core cluster



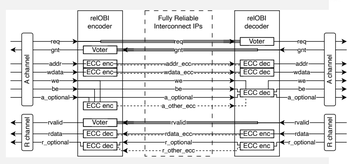
On-Chip Memory

- 32+7 Hsiao Single Error Correction, Double Error Detection ECC code
- Read-modify-write unit for minimal store overhead
- Scrubber to correct storage



On-Chip Interconnect

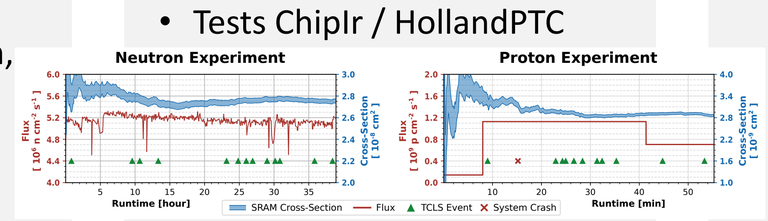
- High-activity SoC components can have an outsized impact on fault rate
- TMR Handshake & ECC Data to correct all faults



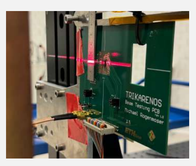
Trikarenos Test

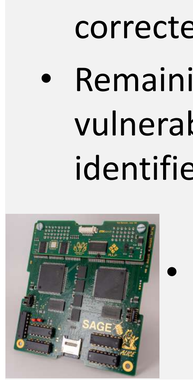
- Fault-tolerant RISC-V MCU in TSMC 28nm[3]
  - 3× Ibex with configurable TCLS
  - ECC SRAM + scrubber

- Tests ChipIr / HollandPTC

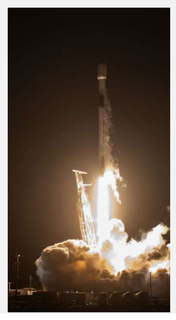


- All SRAM & core faults detected & corrected
- Remaining vulnerabilities identified!



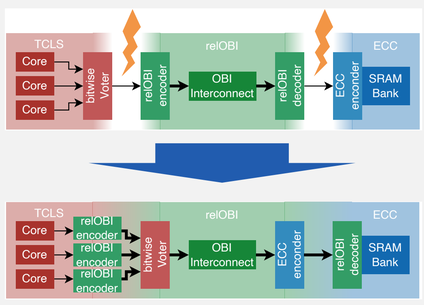


- Launched to space!



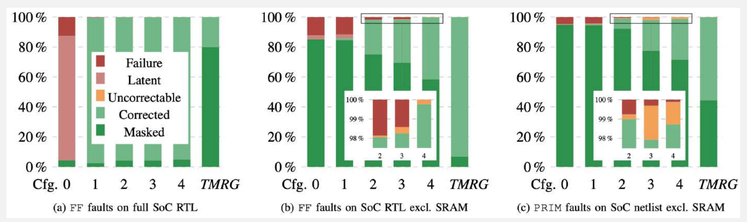
Address the Checkers!

Protection Overlap



- Regions between protected domains, e.g., checkers, remain vulnerable to faults
- Overlapping protections addresses this, ensuring checkers are protected by the other domain

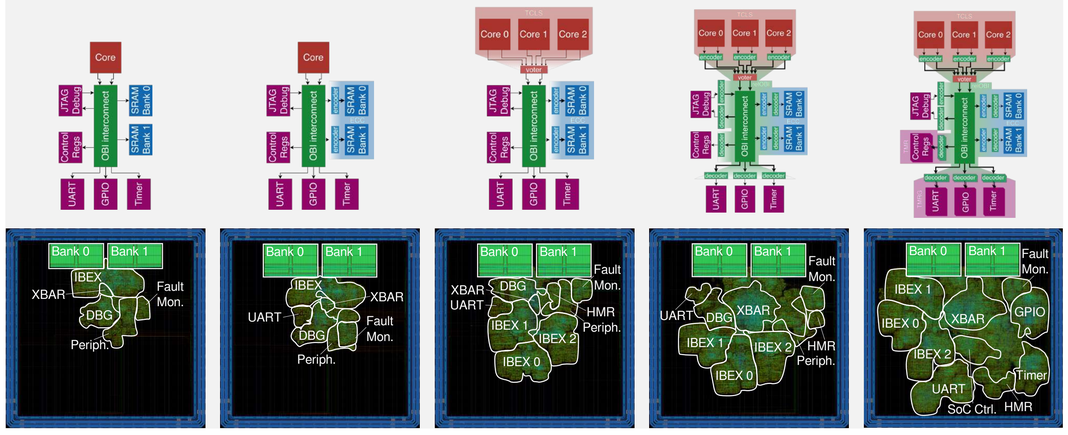
- Evaluated in a RISC-V MCU design (based on Trikarenos) with all developed protections:
  - TCLS-voter faults show up as relOBI errors, and vice versa
  - Iteratively add protections to evaluate impact & fault tolerance



- Physical implementation: 2.71× area vs. 3.48× for SotA full triplication

POST-LAYOUT IMPLEMENTATION RESULTS FOR CROC CFGS.

Cfg.	Used Core Area @ 60 MHz	Max. achieved Frequency	Registers	Area Overhead
0	1.057 mm² / 146 kGE	112 MHz	5113	1.00 ×
1	1.286 mm² / 177 kGE	108 MHz	5254	1.22 ×
2	1.758 mm² / 242 kGE	95 MHz	9358	1.66 ×
3	2.171 mm² / 299 kGE	65 MHz	10 175	2.05 ×
4	2.867 mm² / 395 kGE	62 MHz	13 799	2.71 ×
TMRG	3.676 mm² / 507 kGE	70 MHz	11 964	3.48 ×



Conclusion

- **Open-source**, end-to-end **fault-tolerant** RISC-V SoC leveraging **architectural** methods.
- Validated in 130 nm and transferrable — **node-agnostic** for **New Space** and safety-critical systems. Methodology **tested** under **radiation** and in **simulation-based fault injection**.
- Extends to particle-physics detectors, automotive, and high-radiation domains.

References

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