The Next Generation RISC-V SoCs for Space Communications

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Requirements of NTN gNB-Processors

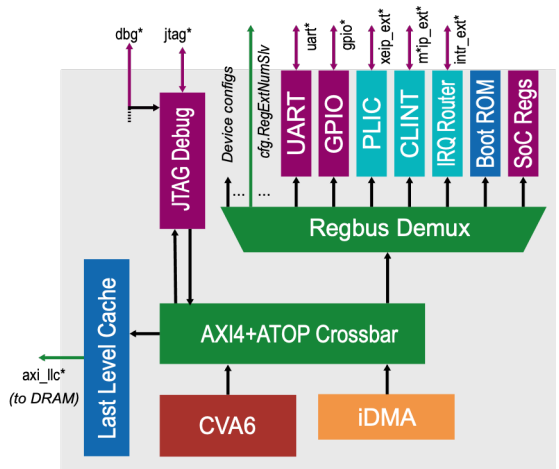
Long lifetime ➔ software defined
High performance (1ms latency @SCS=15kHz, 600Mbps)
Low power consumption

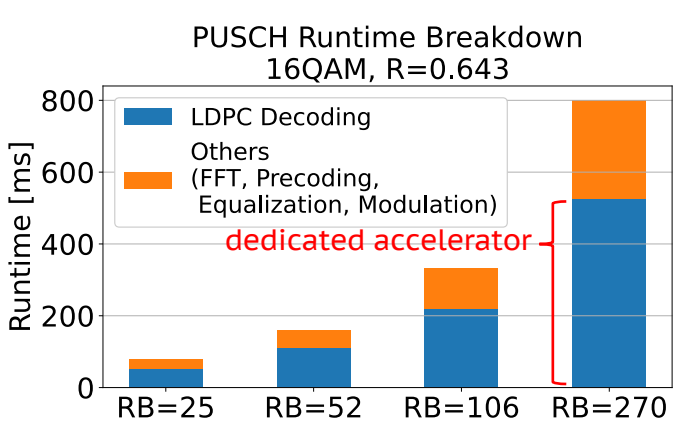
RISC-V® is the solution!

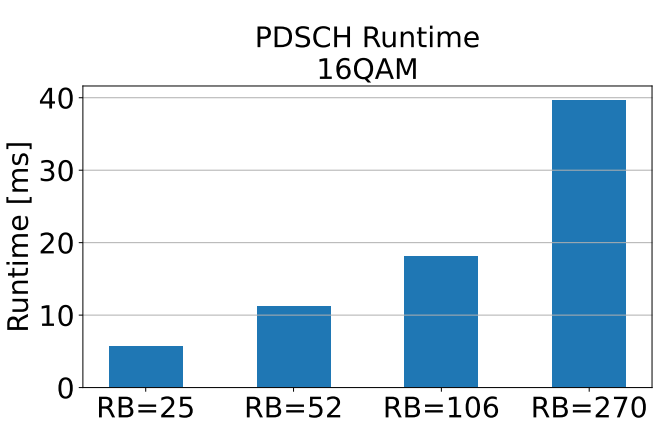
ISA-based acceleration
Performance and energy efficiency via ISA-specialization
Architectural transparency, full stack optimizations guided by hardware-software co-desing

Running Celeste's Smart-gNB (1TX-1RX) on the Cheshire SoC:

- ISA-specialization is mandatory (a single RV64GC core is **~270x** slower than real-time)
- Significant parallelism (resource-blocks, layers, code-block segments)

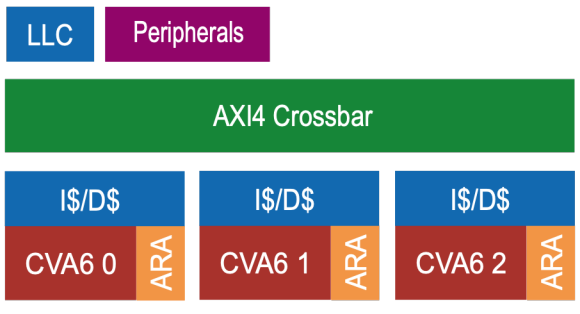






RVV + Scale-OUT!

Multi-core with large RVV co-processors

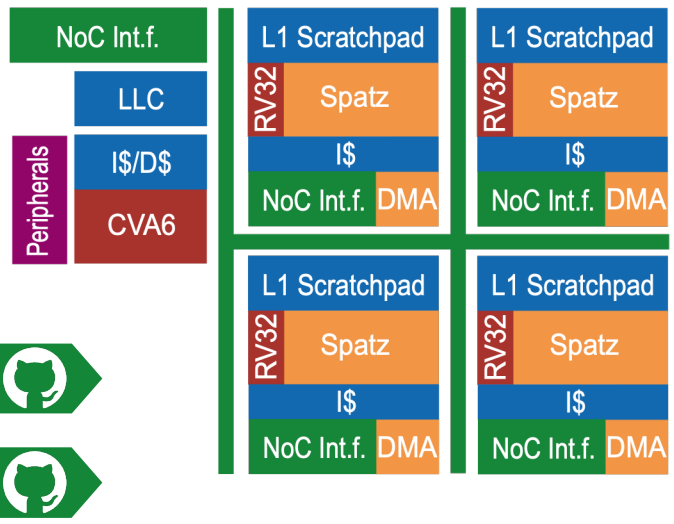


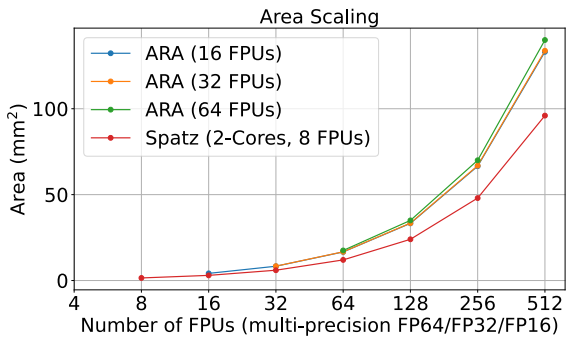
https://github.com/pulp-platform/cheshire

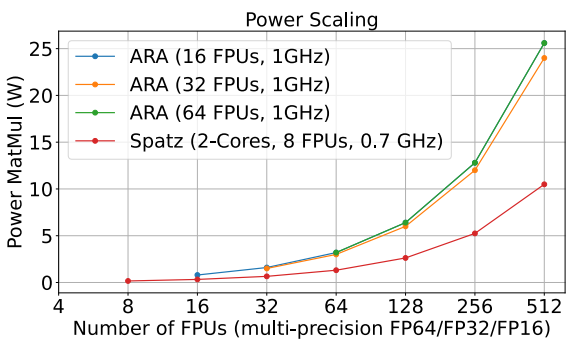
https://github.com/pulp-platform/spatz.git

https://github.com/pulp-platform/AraXL.git

Multi-cluster with ligthweight RV32+RVV complexes







RVV L1-Clusters provide better area and Power scaling compared to large RVV co-processors