ETH zürich

ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

PULP Parallel Ultra Low Power

From Components to Architecture: An End-to-End Approach to Soft-Error Tolerance

Michael Rogenmoser[1], Luca Benini[1,2]

[1]Integrated Systems Laboratory, ETH Zürich
[2]Department of Electrical, Electronic, and Information Engineering, University of Bologna

IEEE COMPUTER SOCIETY TTTC Test Technology Technical Community
E.J. McCluskey Best Doctoral Thesis 2026 Contestant

Motivation

- **Radiation-induced SEUs** corrupt data and computation **in space SoCs**, risking **mission failure**.
- Rad-Hard tech is costly and lags modern nodes.
- **New Space** demands modern, cost-effective, fault-tolerant SoCs on advanced nodes.
- Goal: comprehensive **soft-error tolerance** in RISC-V SoCs via **architectural** methods.

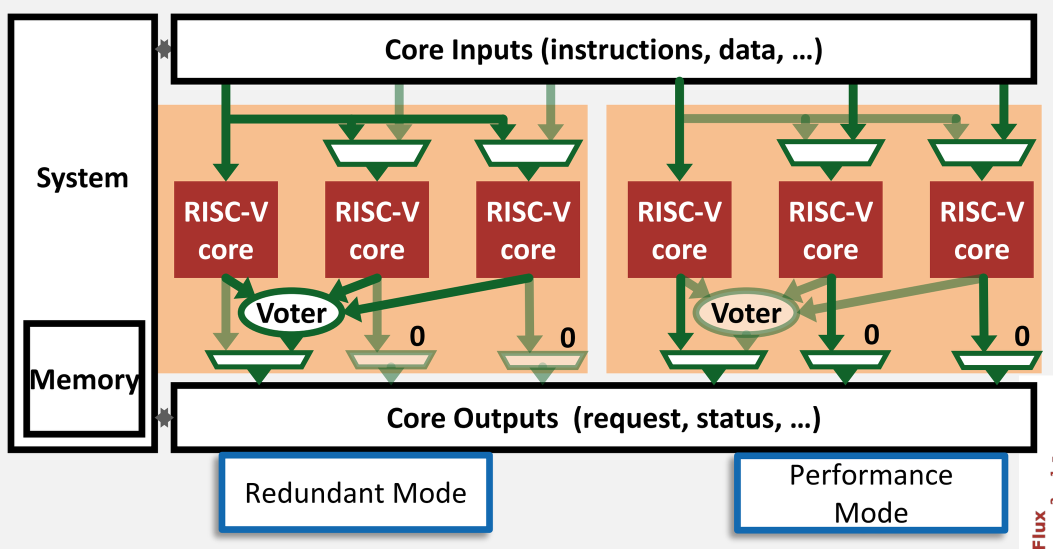
SotA Gaps

- Commercial space processors rely on **outdated and Rad-Hard** nodes, losing out on performance, efficiency, and capabilities.
- Standard lockstep permanently dedicates all cores to redundancy, **sacrificing performance** when fault tolerance is not needed.
- Other architectural schemes (e.g., fine-grained TMR) are expensive.
- No prior work validates a **complete end-to-end** open-source fault-tolerant RISC-V SoC leveraging **optimized tolerance mechanisms**.

Building Blocks

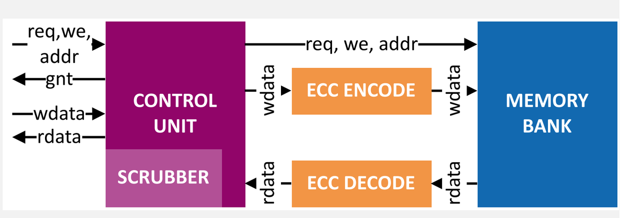
Processor Cores

- Hybrid Modular Redundancy
  - Runtime-switchable
  - Dual- & Triple-core Lockstep (DCLS/TCLS)
  - Tested in a RISC-V multi-core cluster
- Split-lock switching: <400 cycles
- SW recovery: ~700 cycles
  HW recovery: 24 cycles (15x faster)
- 12-core cluster @ 430 MHz, only 1.3–9.4% area overhead
  - 1,160 MOPS independent
  - 617 MOPS DCLS
  - 414 MOPS TCLS



On-Chip Memory

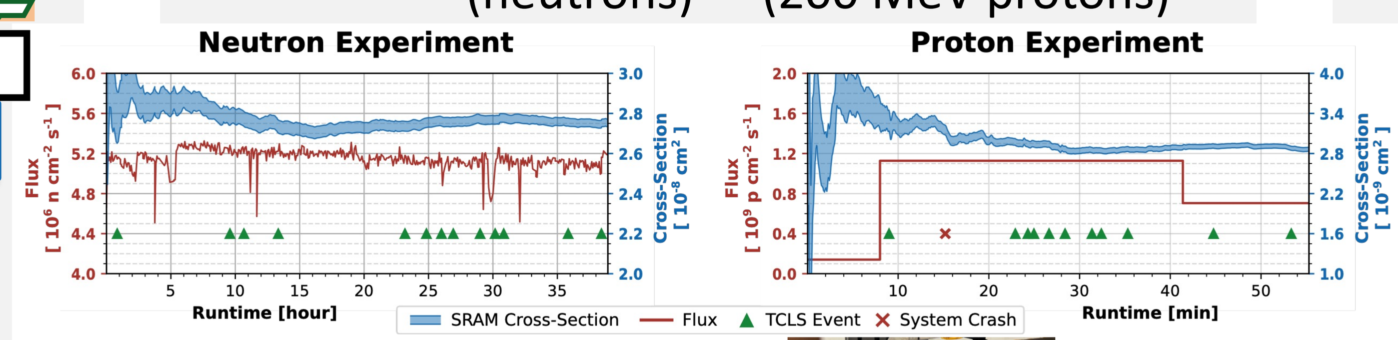
- 32+7 Hsiao Single Error Correction, Double Error Detection ECC code
- Read-modify-write unit for minimal store overhead
- Scrubber to correct storage



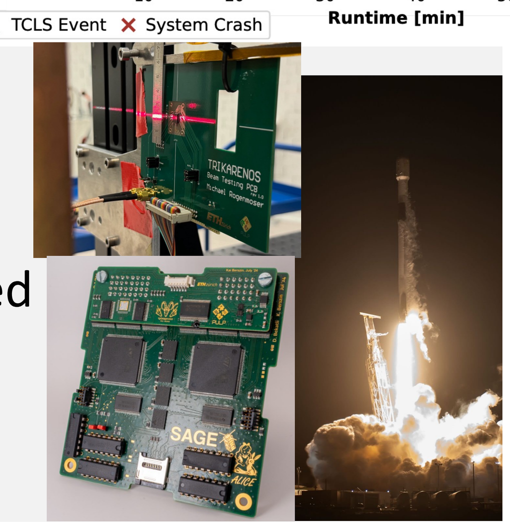
Trikarenos Test Article

- Fault-tolerant RISC-V MCU in TSMC 28nm[3]
  - 3× Ibex with configurable TCLS
  - ECC SRAM + scrubber

- Tested at ChipIr (neutrons) & HollandPTC (200 MeV protons)



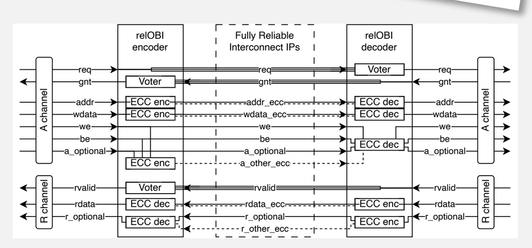
- All SRAM & core faults detected & corrected
- Remaining vulnerabilities identified
- Launched to space!



Lessons Learned

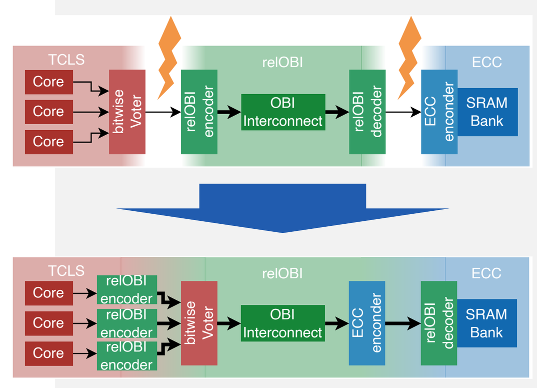
On-Chip Interconnect

- High-activity SoC components can have an outsized impact on fault rate
- TMR Handshake & ECC Data to correct all faults

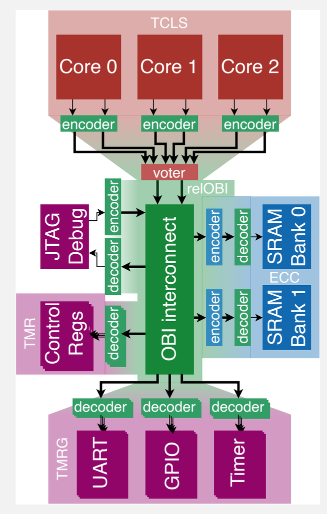


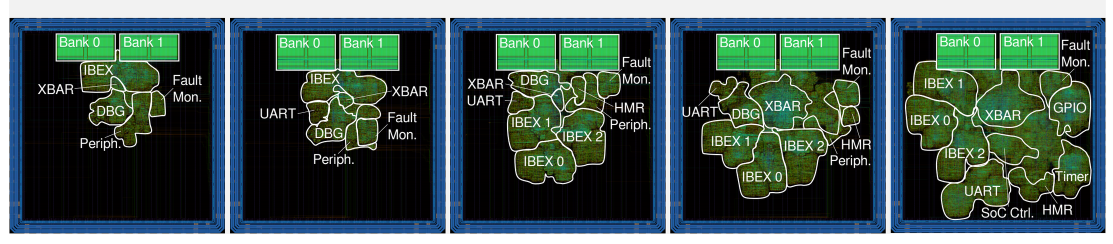
- 34.85% fault rate improved to 0%

Protection Overlap



- Regions between protected domains, e.g., checkers, remain vulnerable to faults
- Overlapping protections addresses this
- Evaluated in a RISC-V MCU design (based on Trikarenos) with all developed protections:
  - TCLS-voter faults show up as relOBI errors, and vice versa
  - Physical implementation: 2.71× area vs. 3.48× for SotA full triplication
  - >99.9% fault coverage





Conclusion

- First **open-source**, end-to-end **fault-tolerant** RISC-V SoC leveraging **architectural** methods.
- Validated in 130, 28, 22, and 7 nm — **node-agnostic** for **New Space** and safety-critical systems. Methodology **tested** under **radiation** and in **simulation-based fault injection**.
- Extends to particle-physics detectors, automotive, and high-radiation domains.

References

[1] M. Rogenmoser, N. Wistoff, P. Vogel, F. Gürkaynak, and L. Benini, "On-Demand Redundancy Grouping: Selectable Soft-Error Tolerance for a Multicore Cluster," in 2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Jul. 2022, pp. 398–401. [Online]. Available: https://ieeexplore.ieee.org/document/9912026

[2] M. Rogenmoser, Y. Tortorella, D. Rossi, F. Conti, and L. Benini, "Hybrid Modular Redundancy: Exploring Modular Redundancy Approaches in RISC-V Multi-core Computing Clusters for Reliable Processing in Space," ACM Trans. Cyber-Phys. Syst., vol. 9, no. 1, pp. 8:1–8:29, Jan. 2025. [Online]. Available: https://dl.acm.org/doi/10.1145/3635161

[3] M. Rogenmoser and L. Benini, "Trikarenos: A Fault-Tolerant RISC-V-based Microcontroller for CubeSats in 28nm," in IEEE International Conference on Electronics, Circuits and Systems (ICECS), Istanbul, Turkey, Dec. 2023, pp. 662–665. [Online]. Available: https://ieeexplore.ieee.org/document/10382727

[4] M. Rogenmoser, P. Wiese, B. E. Forlin, F. K. Gürkaynak, P. Rech, A. Menicucci, M. Ottavi, and L. Benini, "Trikarenos: Design and Experimental Characterization of a Fault-Tolerant 28-nm RISC-V-Based SoC," IEEE Transactions on Nuclear Science, vol. 72, no. 8, pp. 2783–2792, Aug. 2025. [Online]. Available: https://ieeexplore.ieee.org/document/10978878

[5] M. Rogenmoser, A. Garofalo, and L. Benini, "relOBI: A Reliable Low-latency Interconnect for Tightly-Coupled On-chip Communication," in International Integrated Reliability Workshop (IIRW). South Lake Tahoe, CA, USA: arXiv, Oct. 2025, arXiv:2508.05354 [cs]. [Online]. Available: http://arxiv.org/abs/2508.05354

[6] M. Rogenmoser, P. Sauter, C. Wu, A. Garofalo, and L. Benini, "Who Checks the Checker? Enhancing Component-level Architectural SEU Fault Tolerance for End-to-End SoC Protection," in 2026 IEEE 44th VLSI Test Symposium (VTS), Napa, CA, USA, Apr. 2026. [Online]. Available: https://arxiv.org/abs/2603.26637

pulp-platform.org pulp-platform @pulp_platform michaero@iis.ee.ethz.ch

IEEE COMPUTER SOCIETY TTTC Test Technology Technical Community

IEEE TEST SYMPOSIUM